physica status solidi rrl
www.pss-rapid.com

Vacuum-Deposited Inorganic Perovskite Memory Arrays with Long-Term Ambient Stability

*Chen Zou, Lijun He, and Lih Y. Lin**

Recently, metal halide perovskites have been widely used and considered as an alternative to oxides or chalcogenides in memory devices due to the high on–off ratio and low operating voltage, as well as ease of fabrication. However, most of the perovskite thin films in previous studies have been deposited by lab-scale solution-processed methods. They are not directly applicable to larger-scale and volume manufacturing, hindering the commercialization of this technology. Herein, the performance of memory devices based on vacuum-deposited inorganic perovskite (VDIP) is investigated for the first time. The optimized VDIP-based memory devices exhibit reliable and reproducible resistive switching (RS) behaviors with a high on–off ratio (>100), low set/reset voltage (<2 V), and reversible RS by fast pulse-voltage operations. Furthermore, the devices show an excellent ambient stability, and no obvious degradation is observed after storage in an ambient condition for 30 days. The memory devices on flexible substrates also show a good mechanical flexibility under a bending stress. In addition, a VDIP memory array with 16 × 16 memory cells on a large-scale substrate is demonstrated, suggesting the strong potential of the VDIP for high-density, large-area storage devices.

Among various memory technologies that have been developed, resistive switching random access memory (ReRAM) is considered as one of the most promising next-generation storage devices and targeted as a replacement technology for flash memory due to its low energy consumption, good cycle endurance, high switching speed, simple architecture, and good scaling behavior.[1] An external bias can switch the memory resistance between a high resistance state (HRS) and a low resistance state (LRS). As a result, ReRAM stores the information using these two nonvolatile switchable resistance states.[2]

Metal halide perovskite materials have attracted a lot of attention recently due to its excellent performance in solar cells.[3–5] The most widely studied methylammonium lead iodide ($MAPbI_3$)-based solar cell has achieved a power conversion efficiency above 22%,[6] which is much higher than that of polycrystalline silicon solar cells, and even comparable with single crystal silicon solar cells. It is observed that ion/defect mitigation and the resultant hysteresis in the current–voltage curves are usually inevitably present in solar cells.[7] The phenomenon is undesirable since it influences the stability and performance assessment of solar cells.[8] In contrast, this provides the required properties for applications of perovskite materials in high-performance memory devices.[9–15] In fact, many studies on organic–inorganic hybrid perovskites ($MAPbX_3$, X = Cl, Br, I)-based memory devices have exhibited a good performance including low switching voltage, high on–off ratio, good data retention, and endurance ability.[16–18] However, the performance of memory devices based on vapor-deposited all-inorganic metal halide perovskite is not systematically investigated. All-inorganic perovskite recently attracted the attention of the perovskite research community with its higher thermal stability.[19–21] Unlike methylammonium lead halide that decomposes into organic halide and lead halide at high temperatures, an inorganic cesium cation is more thermally stable and thus considered as a suitable substitute for organic cation (MA, FA).[22,23] In addition, the vacuum-deposition method provides advantages of good uniformity, precise thickness control, large-scale manufacturing, and good compatibility with flexible substrates compared with spin-coating processes.[24,25]

In this work, we studied the electrical properties of VDIP memory devices for the first time. We demonstrated VDIP-based ReRAM arrays with 16 × 16 memory cells on large-scale rigid and flexible substrates. The resistance ratios of memory cells between HRS and LRS are shown to stay around 100. The memory cells show repetitive current-switching behaviors during write-read-erase-read cycle tests, and no obvious degradation of the on–off current ratio is observed after storage in ambient conditions for 30 days. These results demonstrate good data retention and cycle endurance capability of VDIP-based memory cells. Furthermore, the VDIP-based ReRAM devices on flexible polyethylene terephthalate (PET) substrates exhibit an excellent bending capability. The devices can maintain their current–voltage (I–V) characteristics in different bending angles and after repetitive bending cycles. Finally, each memory cell in the memory array can be selected individually and applied an electrical pulse through a specific row and column. As a demonstration,

Dr. C. Zou, Prof. L. He, Prof. L. Y. Lin
Department of Electrical and Computer Engineering
University of Washington
Seattle, WA 98195, USA
E-mail: lylin@uw.edu

Prof. L. He
The School of Optoelectronic Engineering
Chongqing University of Posts and Telecommunications
Chongqing 400065, P. R. China

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/pssr.201900182.

DOI: 10.1002/pssr.201900182

16 memory cells on a diagonal line were addressed, and data were stored as a result. These characteristics suggest the great potential of VDIP for use in large-area, high-density memory devices.[26]

The fabrication process of the memory array is schematically shown in **Figure 1**a. Any desired substrate could be used, given the dexterity of the vacuum-deposited process for perovskite, which is especially favorable for fabricating flexible devices. In this work, we used large-scale rigid glass and flexible PET substrates for demonstrating the convenient and scalable fabrication process. The Ag nanoparticle ink was inkjet-printed onto the substrate to form the bottom electrode (BE) array. All-inorganic perovskite $CsPbBr_3$ was deposited through co-evaporating CsBr and $PbBr_2$ simultaneously with approximate rates. The top-view scanning electron microscopy (SEM) image (Figure S1a, Supporting Information) showed a continuous and good coverage perovskite film without obvious pinholes. The smooth surface of the perovskite layer was also confirmed by the atomic force microscopy (AFM) image (Figure S1b, Supporting Information). The average surface roughness is only 9.7 nm.

The MoO_3 layer was thermally evaporated onto the perovskite layer to protect perovskite from moisture and oxygen in an ambient environment, increasing the stability of perovskite memory devices.[16] The Ag top electrode (TE) array was vacuum-deposited onto the MoO_3 layer to form 16×16 intersections with the BE array, each intersection forming a memory cell.

The photograph of the as-fabricated device on the glass substrate is shown in Figure 1b. The magnified optical microscopy image in Figure 1c shows VDIP memory cells with a cell area of $200 \times 200\ \mu m^2$. Figure 1d schematically shows the single memory cell structure of $Ag/CsPbBr_3/MoO_3/Ag$, where the BE is grounded, and the voltage is applied to the TE for resistive switching (RS). The thickness for each layer is 100, 200, 20, and 100 nm in sequence.

The current–voltage (I–V) characteristics of the $Ag/CsPbBr_3/MoO_3/Ag$ memory cell are shown in **Figure 2**a. The I–V measurement was carried out by applying the bias voltage to the Ag TE with a sweep from $0\ V \rightarrow 2\ V \rightarrow 0\ V \rightarrow -2\ V \rightarrow 0\ V$ while grounding the Ag BE. During the application of a positive sweep from 0 to 2 V with a compliance current of 1 mA, the set process occurred from LRS to HRS at around 0.7 V. When a negative voltage sweep of 0 to −2 V was applied, the resistance of the perovskite layer changed from the LRS to HRS, confirming the occurrence of the reset process. The set and reset processes could only be performed in opposite bias polarities, demonstrating that perovskite memory devices exhibit a bipolar RS behavior.[27]

The write-read-erase-read sequence test was conducted to demonstrate the switching characteristic of the perovskite memory device.[28] The applied voltage pulse cycle was designed as shown in the top panel of Figure 2b: 2 V to write (Set), 0.2 V to read out the current (I_{LRS}), −2 V to erase (Reset), and 0.2 V to read out I_{HRS}; the duration of each pulse is 1 s. The current response for applied voltage pulse cycles is shown in the lower panel of Figure 2b. In each cycle, the write pulse triggered the memory switching from HRS to LRS; a stable high current of ≈0.3 mA was recorded in the following read period. Similarly, the erase pulse reset the memory and changed the resistance back to HRS, and thus a stable low current of ≈3 μA was measured in the subsequent period after the erase pulse.

The cycling endurance property of the perovskite memory device was measured using consecutive write-read-erase-read voltage pulses.[18] I_{LRS} and I_{HRS} were recorded after each set and reset cycle, as shown in Figure 2c. We noticed the apparent difference between I_{LRS} and I_{HRS}, resulting in an on–off ratio ≈100 at 0.2 V. During cycling tests, neither I_{LRS} nor I_{HRS} was observed to degrade obviously. The ambient stability of the VDIP memory devices was investigated in an air atmosphere at 20 °C and with 30–40% humidity. The I–V curves still exhibited bipolar RS properties after exposure to air for 30 days (Figure S2, Supporting Information). Figure 2d records the I_{LRS} and I_{HRS} of VDIP memory devices during storage in air for 30 days. Although there are some fluctuations, the on–off ratio remained >40, which should be sufficient to distinguish HRS from LRS. All these results demonstrate a great reproducibility of the RS behavior from cycle to cycle and a good electrical reliability of the VDIP memory devices, thus confirming the application feasibility of the VDIP memory as a rewritable storage device.

In previous reports on perovskite memory devices, RS behaviors were attributed to the conduction filament (CF) and

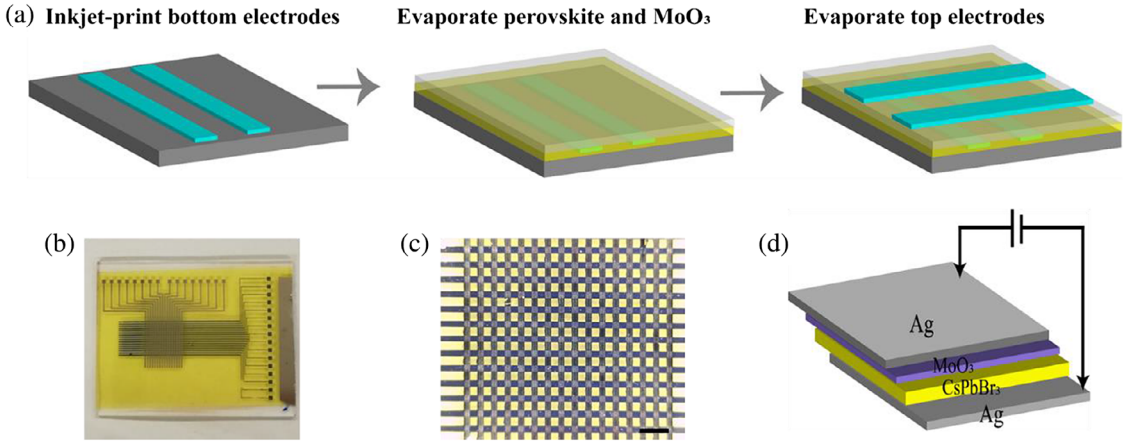

Figure 1. a) The schematic fabrication process of the inorganic perovskite memory array through all-vacuum-deposited processes. b) The photograph of the as-fabricated memory array on glass. c) The optical microcopy image of the memory cells (scale bar, 1 mm). d) The schematic structure of a single memory cell.

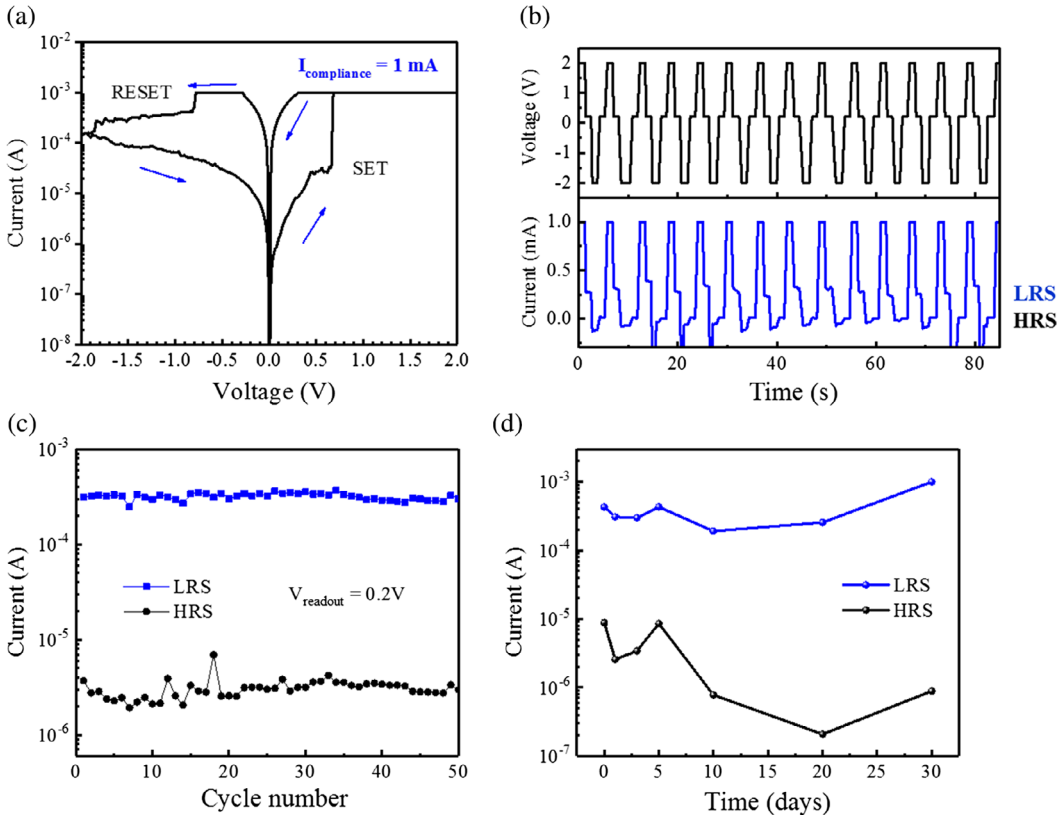

Figure 2. a) The current–voltage (*I–V*) curve of the perovskite memory devices. b) Current responses during write-read-erase pulse cycles (specifically, 2 V to write, 0.2 V to read, 2 V to erase, and 0.2 V to read). c) The cycle endurance test result. d) The stability of fabricated memory devices stored in an ambient condition.

interface-type switching mechanism.[29,30] We first investigated the effect of the device area on the I_{LRS} and I_{HRS} currents to determine which mechanism has the main contribution in our devices. We fabricated VDIP memory devices with different device areas (0.01, 0.04, 0.09, 0.16, 0.64, and 1 mm^2). The readout voltage is 0.2 V, and the current compliance is set as 1 mA. For each device area, the I_{LRS} and I_{HRS} were measured on six devices in the same batch. As shown in **Figure 3**a, both average values of I_{LRS} and I_{HRS} do not change obviously with an increasing device area, clearly opposite to the interface-based switching mechanism, where the current or resistance is dependent on the device area due to the interface modulation.[31,32] Therefore, we attributed the creation and annihilation of CF as the main mechanism contributing to the RS operations in this work. The thin perovskite layer (200 nm) in our case also facilitates the establishment of the ion migration path.[29]

We further proved the existence of charge trapping and CF in the RS behaviors by replotting the *I–V* curve in a log scale as shown in Figure 3b. The fitted results indicate that the *I–V* characteristics in HRS consists of ohmic and space-charge limited current (SCLC) conduction regions. In a region from 0 to 0.25 V (Figure 3c(i)), the relationship between current and voltage follows $I–V^{1.15}$, indicating that the ohmic conduction is dominant. In this region, the weak injection of charges cannot completely fill the traps, and thus the ohmic behavior is observed. In a region from 0.25 to 0.7 V, the electric field across the device is large enough to fill up all traps with charge carriers. The *I–V* characteristics follow the Child's law ($I–V^2$), indicating the transition from the ohmic to SCLC region (Figure 3c(ii)).[33] Continually increasing the voltage, the CF builds up and bridges the TE and BE. The injected carriers can move freely through the CF path, leading to the abrupt increase of the current to the compliance current of 1 mA; the resistance changes from HRS to LRS correspondingly (Figure 3c(iii)). In the region from 0.3 to 0 V, the *I–V* curve exhibits an exact linear relationship (slope of 1), obeying the ohmic conduction mechanism and suggesting the CF formed in the perovskite layer.[34] Then, the current is driven by the injected carriers and mainly dependent on the charge mobility through the CF path.

Sun et al. reported the competition of Ag CFs and iodine vacancy (V_I) CFs in $MAPbI_3$-based memory devices.[35] They found that both Ag ions and iodine ions can contribute to comparable ion migration when the perovskite layer thickness is reduced to 90 nm; however, iodine ion migration is the main CF when the thickness increases. In our case, we assumed that bromide vacancy (V_{Br}) CFs mainly contribute to the RS behavior, considering the thickness of the perovskite layer (200 nm). When a positive bias is applied to the Ag TE, negatively charged Br^- ions migrate toward the TE and form a thin AgBr layer near the TE.[36] Meanwhile, the bromide vacancies are created and accumulate from TE to BE until the V_{Br} CFs are throughout the perovskite layer, and then the memory cell is switched to

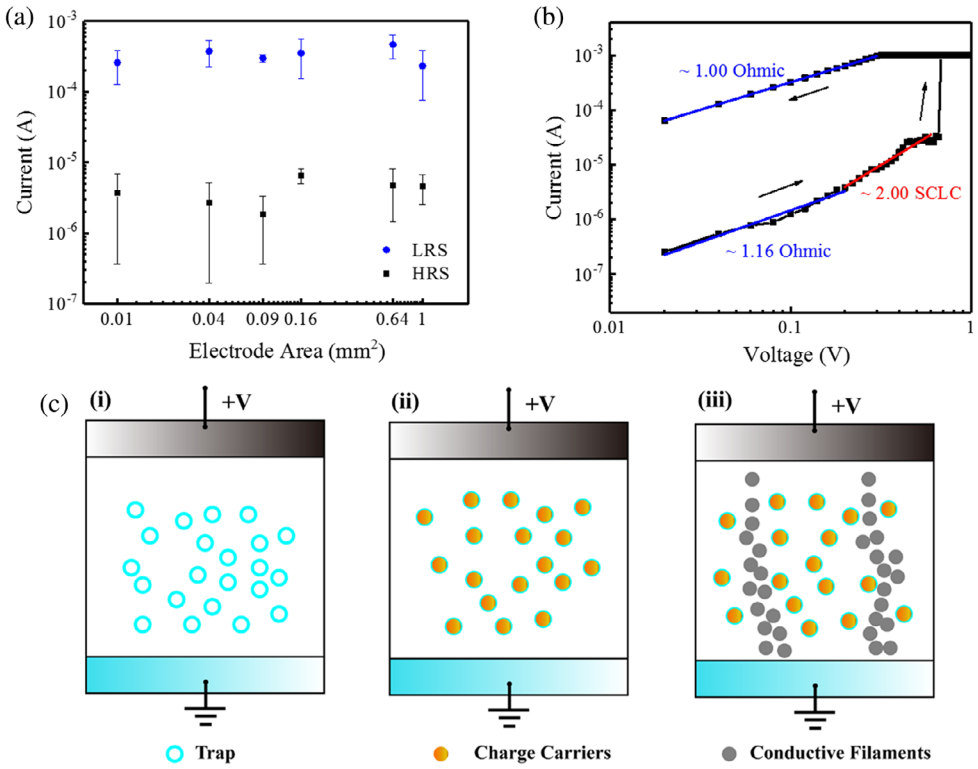

Figure 3. The investigation of the RS mechanism in VDIP memory devices. a) The currents in LRS and HRS (readout at 0.2 V) as a function of the device area, indicating the CF mechanism. b) The log–log scale plot of the *I–V* curve in the positive voltage sweep. c) The schematic illustration of the RS mechanism.

LRS.[37] When a negative voltage is applied to the BE, the Br^- ions stored near the Ag electrode migrate into the $CsPbBr_3$ film and recombine with V_{Br}, leading to the rupture of V_{Br} CFs, and the memory cell is switched back to HRS. The RS behavior can be well explained by the creation and dissolution of V_{Br} CFs.

To demonstrate the bending capability and application feasibility of the flexible VDIP memory array, the device was subjected to different bending states and number of bending cycles. First, the electrical characteristics were measured under different bending states (0° → 60° → 90° → 120° → 180°) with a compliance current of 1 mA. **Figure 4**a shows the *I–V* curves (0 V → 2 V → 0 V → −2 V → 0 V) of the flexible memory device under these four bending states; the inset photographs show the measurement setup and the schematic illustration of the central angle (θ) for the flexible device under bending status. The *I–V* curves measured at different bending angles all show bipolar RS behaviors, suggesting an application potential for flexible storage devices. Repetitive bending cycles test were also measured as

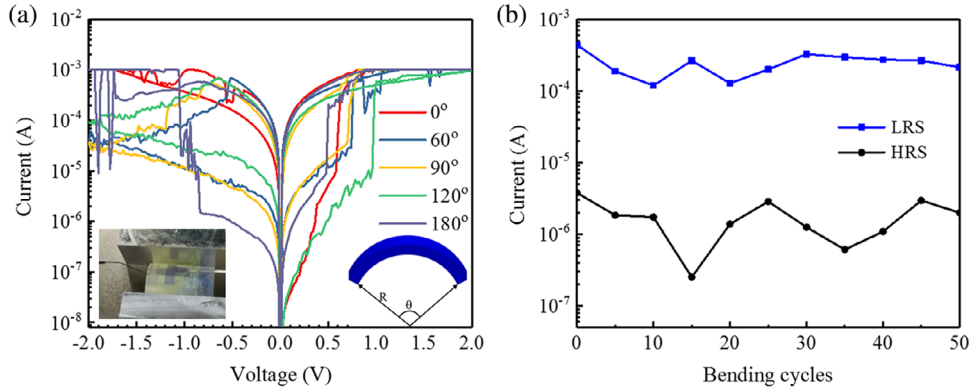

Figure 4. The bending performance of flexible perovskite memory devices. a) *I–V* curves measured at various bending angles. The inset photographs show the measurement setup and the schematic illustration of the central angle (θ) for the flexible device under bending. b) The currents of flexible devices in LRS and HRS after different bending cycles.

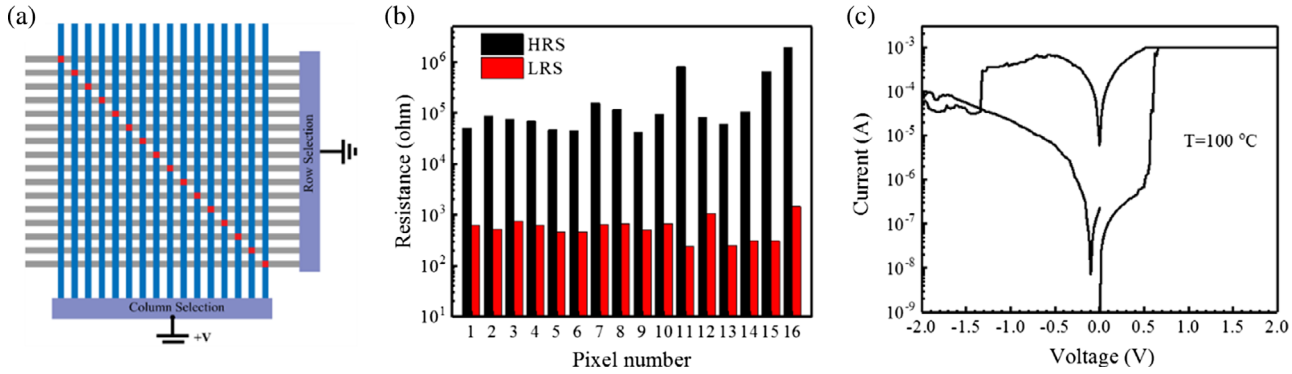

Figure 5. Reliable RS properties of the perovskite memory array. a) The schematic illustration of testing 16 memory cells on the diagonal line. b) The resistances of 16 memory cells in HRS and LRS. c) The *I–V* curve of one memory cell measured at an elevated temperature of 100 °C.

shown in Figure 4b. Although the I_{LRS} and I_{HRS} currents fluctuated a little bit, the on–off current ratio retained around 100 robustly over 50 bending cycles. Overall, these results demonstrate that VDIP memory devices have good electrical properties and bending stability, indicating the promising application in flexible data storage devices.

To check the feasibility of storing data in the VDIP memory array, we applied "set" electrical pulses (2 V) to memory cells along the diagonal line through corresponding TEs and BEs (**Figure 5**a). The currents of 16 memory cells on the diagonal line before and after electrical pulses were read out at 0.2 V as shown in Figure 5b. Before electrical pulses, 16 memory cells were all in HRS, and the readout currents were in the range of 10^{-7}–10^{-5} A. After electrical pulses, the memory cells were switched to LRS, and the currents were in the range of 10^{-4}–10^{-3} A. The reliable switching behaviors suggest the feasibility of the VDIP for high-density and large-area memory devices. In addition, the memory array device still showed the bipolar RS behavior at an elevated temperature of 100 °C (Figure 5c), which demonstrates the good thermal stability of VDIP films.

In summary, we demonstrated a memory array based on the VDIP. The VDIP films exhibit a uniform surface morphology and better adaptability in large-scale and flexible devices. The 16×16 memory cells can be individually addressed and tested, and they show reliable RS behaviors with a high on–off ratio around 100 and a great ambient stability. These results demonstrate the great potential of the VDIP material for high-density storage devices. In addition, the flexible memory array on the PET substrate shows a good mechanical bending capability, suggesting great potential for integrating storage devices on flexible substrates.

Experimental Section

Perovskite Deposition: The all-inorganic perovskite $CsPbBr_3$ was deposited through a dual-source thermal evaporation method. The CsBr and $PbBr_2$ were placed into two crucibles separately and heated to sublime temperatures. Two quartz crystal monitors (QCMs) were used to measure the evaporation rates of two sources. The evaporation rates of CsBr and $PbBr_2$ were 0.8 and 0.5 Å s^{-1}, respectively, based on their molar mass and density. The tool factors of QCMs were calibrated by comparing the actual deposited thickness (measured by a profilometer) and the expected thickness.

Device Fabrication: The rigid glass and flexible PET substrates were ultrasonic-cleaned in acetone, 2-propanol, and DI water in sequence. The Ag nanoparticle ink was loaded into the cartridge of an inkjet printer (Diamatrix), and the cartridge was ultrasonicated briefly to reduce the aggregation of Ag nanoparticles. The voltage of printing nozzle was set at 23 V, and the waveform frequency was set at 5 kHz. The cleaned substrates were well adhered to the printing platform using vacuum, and the platform temperature was set at room temperature. The printing nozzle was controlled by the computer to drop the Ag ink with the designed pattern. The substrates were then heated in an oven at 110 °C for 10 min to sinter the Ag electrodes. The perovskite layer was deposited as mentioned earlier. The MoO_3 layer (20 nm) was deposited atop the perovskite layer to protect it from moisture ingest. Finally, the top Ag electrode rows were evaporated through another shadow mask.

Characterization: The crystal grain morphology of perovskite films and the cross-sectional view of the memory cell were characterized by SEM (FEI, Sirion). The surface roughness of perovskite films was measured by AFM (Bruker). The *I–V* curves of perovskite memory cells were measured by a source meter (Keithley 6430) with the applied voltage sweeping in $0\,V \rightarrow 2\,V \rightarrow 0\,V \rightarrow -2\,V \rightarrow 0\,V$. The write-read-erase-read cycles were conducted by setting the applied voltage at 2, 0.2, −2, and 0.2 V for 1 s.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported in part by the National Science Foundation (grant ECCS-1807397). Part of the work was conducted at the Molecular Analysis Facility and Washington Nanofabrication Facility, a National Nanotechnology Coordinated Infrastructure site at the University of Washington, which is supported in part by the National Science Foundation (grant NNCI-1542101), the University of Washington, the Molecular Engineering & Sciences Institute, the Clean Energy Institute, and the National Institutes of Health.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

inorganic perovskites, memory arrays, resistive switching, device stability, vacuum deposition

Received: March 26, 2019
Revised: April 25, 2019
Published online: May 24, 2019

[1] T.-C. Chang, K.-C. Chang, T.-M. Tsai, T.-J. Chu, S. M. Sze, *Mater. Today* **2016**, *19*, 254.
[2] B. Hwang, J. S. Lee, *Adv. Electron. Mater.* **2019**, *5*, 1800519.
[3] M. Liu, M. B. Johnston, H. J. Snaith, *Nature* **2013**, *501*, 395.
[4] A. Swarnkar, A. R. Marshall, E. M. Sanehira, B. D. Chernomordik, D. T. Moore, J. A. Christians, T. Chakrabarti, J. M. Luther, *Science* **2016**, *354*, 92.
[5] M. A. Green, A. Ho-Baillie, H. J. Snaith, *Nat. Photonics* **2014**, *8*, 506.
[6] W. S. Yang, B. W. Park, E. H. Jung, N. J. Jeon, Y. C. Kim, D. U. Lee, S. S. Shin, J. Seo, E. K. Kim, J. H. Noh, S. I. Seok, *Science* **2017**, *356*, 1376.
[7] B. Chen, M. Yang, S. Priya, K. Zhu, *J. Phys. Chem. Lett.* **2016**, *7*, 905.
[8] A. Rizzo, F. Lamberti, M. Buonomo, N. Wrachien, L. Torto, N. Lago, S. Sansoni, R. Pilot, M. Prato, N. Michieli, *Sol. Energy Mater. Sol. Cells* **2019**, *189*, 43.
[9] C. Gu, J. S. Lee, *ACS Nano* **2016**, *10*, 5413.
[10] J. Choi, J. S. Han, K. Hong, S. Y. Kim, H. W. Jang, *Adv. Mater.* **2018**, 1704002.
[11] J. H. Heo, D. H. Shin, S. H. Moon, M. H. Lee, D. H. Kim, S. H. Oh, W. Jo, S. H. Im, *Sci. Rep.* **2017**, *7*, 16586.
[12] K. Yang, F. Li, C. P. Veeramalai, T. Guo, *Appl. Phys. Lett.* **2017**, *110*, 083102.
[13] J. Zhao, S. Li, W. Tong, G. Chen, Y. Xiao, S. Lei, B. Cheng, *Adv. Electron. Mater.* **2018**, *4*, 1800206.
[14] H. Kim, J. S. Han, S. G. Kim, S. Y. Kim, H. W. Jang, *J. Mater. Chem. C* **2019**, *7*, 5226.
[15] R. A. John, N. Yantara, Y. F. Ng, G. Narasimman, E. Mosconi, D. Meggiolaro, M. R. Kulkarni, P. K. Gopalakrishnan, C. A. Nguyen, F. De Angelis, *Adv. Mater.* **2018**, *30*, 1805454.
[16] B. Hwang, J. S. Lee, *Sci. Rep.* **2017**, *7*, 673.
[17] Y. Liu, F. Li, Z. Chen, T. Guo, C. Wu, T. W. Kim, *Vacuum* **2016**, *130*, 109.
[18] J. Choi, Q. V. Le, K. Hong, C. W. Moon, J. S. Han, K. C. Kwon, P. R. Cha, Y. Kwon, S. Y. Kim, H. W. Jang, *ACS Appl. Mater. Interfaces* **2017**, *9*, 30764.
[19] R. J. Sutton, G. E. Eperon, L. Miranda, E. S. Parrott, B. A. Kamino, J. B. Patel, M. T. Hörantner, M. B. Johnston, A. A. Haghighirad, D. T. Moore, *Adv. Energy Mater.* **2016**, *6*, 1502458.
[20] M. Saliba, T. Matsui, J.-Y. Seo, K. Domanski, J.-P. Correa-Baena, M. K. Nazeeruddin, S. M. Zakeeruddin, W. Tress, A. Abate, A. Hagfeldt, *Energy Environ. Sci.* **2016**, *9*, 1989.
[21] J. S. Han, Q. V. Le, J. Choi, H. Kim, S. G. Kim, K. T. Hong, C. W. Moon, T. L. Kim, S. Y. Kim, H. W. Jang, *ACS Appl. Mater. Interfaces* **2019**, *11*, 8155.
[22] J. Liang, C. Wang, Y. Wang, Z. Xu, Z. Lu, Y. Ma, H. Zhu, Y. Hu, C. Xiao, X. Yi, *J. Am. Chem. Soc.* **2016**, *138*, 15829.
[23] B. W. Park, S. I. Seok, *Adv. Mater.* **2019**, *31*, 1805337.
[24] J. Ávila, C. Momblona, P. P. Boix, M. Sessolo, H. J. Bolink, *Joule* **2017**, *1*, 431.
[25] G. Tong, H. Li, D. Li, Z. Zhu, E. Xu, G. Li, L. Yu, J. Xu, Y. Jiang, *Small* **2018**, *14*, 1702523.
[26] B. Hwang, J. S. Lee, *Adv. Mater.* **2017**, *29*, 1701048.
[27] E. J. Yoo, M. Lyu, J. H. Yun, C. J. Kang, Y. J. Choi, L. Wang, *Adv. Mater.* **2015**, *27*, 6170.
[28] Y. Ren, H. Ma, W. Wang, Z. Wang, H. Xu, X. Zhao, W. Liu, J. Ma, Y. Liu, *Adv. Mater. Technol.* **2019**, *4*, 1800238.
[29] X. Guan, W. Hu, M. A. Haque, N. Wei, Z. Liu, A. Chen, T. Wu, *Adv. Funct. Mater.* **2018**, *28*, 1704665.
[30] Y. Wang, Z. Lv, Q. Liao, H. Shan, J. Chen, Y. Zhou, L. Zhou, X. Chen, V. A. L. Roy, Z. Wang, Z. Xu, Y. J. Zeng, S. T. Han, *Adv. Mater.* **2018**, *30*, 1800327.
[31] X. F. Cheng, X. Hou, J. Zhou, B. J. Gao, J. H. He, H. Li, Q. F. Xu, N. J. Li, D. Y. Chen, J. M. Lu, *Small* **2018**, *14*, 1703667.
[32] F. Zhou, Y. Liu, X. Shen, M. Wang, F. Yuan, Y. Chai, *Adv. Funct. Mater.* **2018**, *28*, 1800080.
[33] Z. Xu, Z. Liu, Y. Huang, G. Zheng, Q. Chen, H. Zhou, *J. Mater. Chem. C* **2017**, *5*, 5810.
[34] D. Liu, Q. Lin, Z. Zang, M. Wang, P. Wangyang, X. Tang, M. Zhou, W. Hu, *ACS Appl. Mater. Interfaces* **2017**, *9*, 6171.
[35] Y. Sun, M. Tai, C. Song, Z. Wang, J. Yin, F. Li, H. Wu, F. Zeng, H. Lin, F. Pan, *J. Phys. Chem. C* **2018**, *122*, 6431.
[36] X. Zhu, J. Lee, W. D. Lu, *Adv. Mater.* **2017**, *29*, 1700527.
[37] B. Hwang, C. Gu, D. Lee, J. S. Lee, *Sci. Rep.* **2017**, *7*, 43794.

