

# P160 Module Specification



**Version 1.3**  
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PN# DS-MANUAL-P160-SPEC



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## Table of Contents

<b>1</b>	<b>OVERVIEW .....</b>	<b>1</b>
1.1	MECHANICAL DIMENSIONS .....	2
1.2	CONNECTORS .....	2
1.3	SIGNAL DESCRIPTIONS .....	3
1.4	POWER BUDGET .....	5
<b>2</b>	<b>REVISIONS .....</b>	<b>6</b>
	<b>APPENDIX A - HIROSE DATA SHEET .....</b>	<b>7</b>

## Figures

FIGURE 1 – EXAMPLE P160 SYSTEM BOARD .....	1
FIGURE 2 – P160 PHYSICAL DIMENSIONS .....	2

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## Tables

TABLE 1 – JX1 LEFT USER I/O CONNECTOR .....	3
TABLE 2 – JX2 RIGHT USER I/O CONNECTOR.....	4
TABLE 3 – P160 POWER BUDGETS .....	5

## 1 Overview

The P160 module specification defines an open standard for connecting expansion modules or add-on cards to existing circuit boards. Although originally defined for use on generic FPGA development boards, there are only limited FPGA specific signals and functions included in the standard. The P160 module defines two 80-pin, low insertion force connectors that connect the daughter card to the main system board. Each connector has a defined signal name and voltage level. This specification provides the information needed to interface to any P160 slot and to allow development of custom P160 modules. The figure below shows an example P160 implementation on the Memec Design Virtex-II MB1000 Development board.

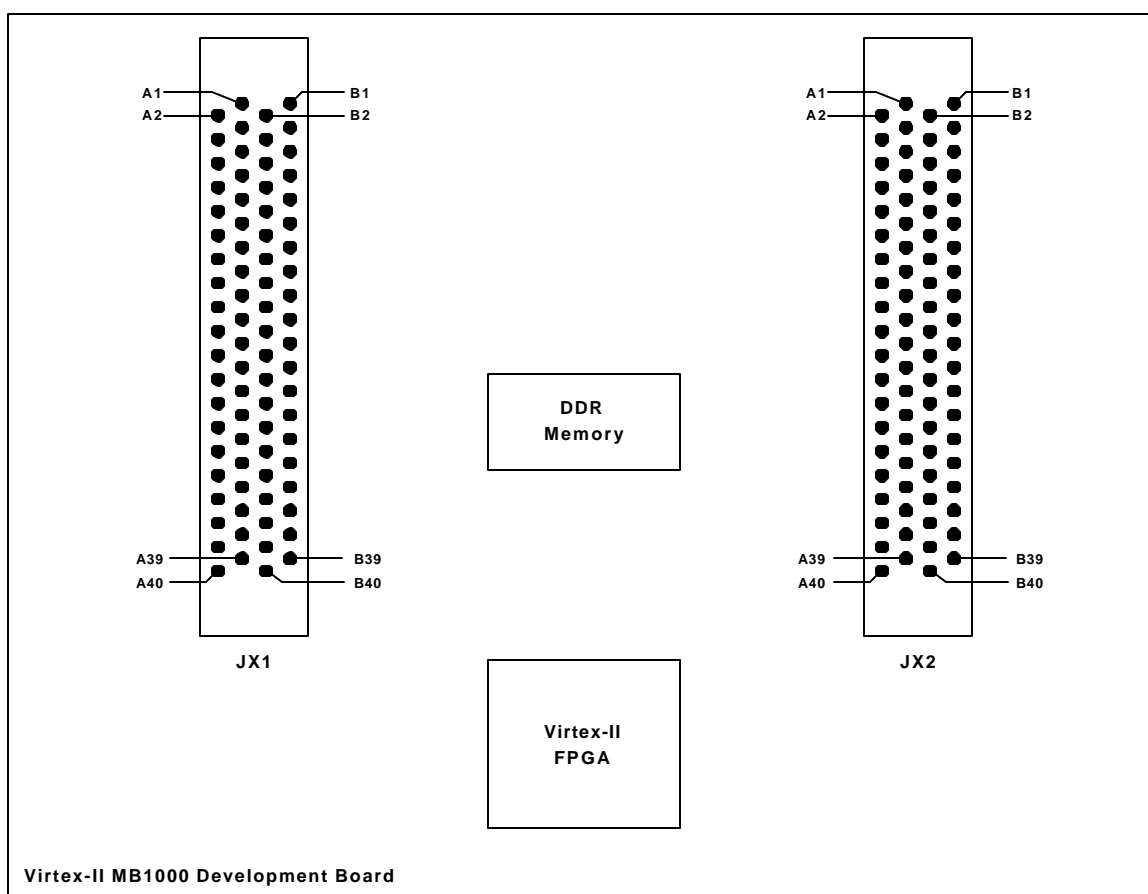
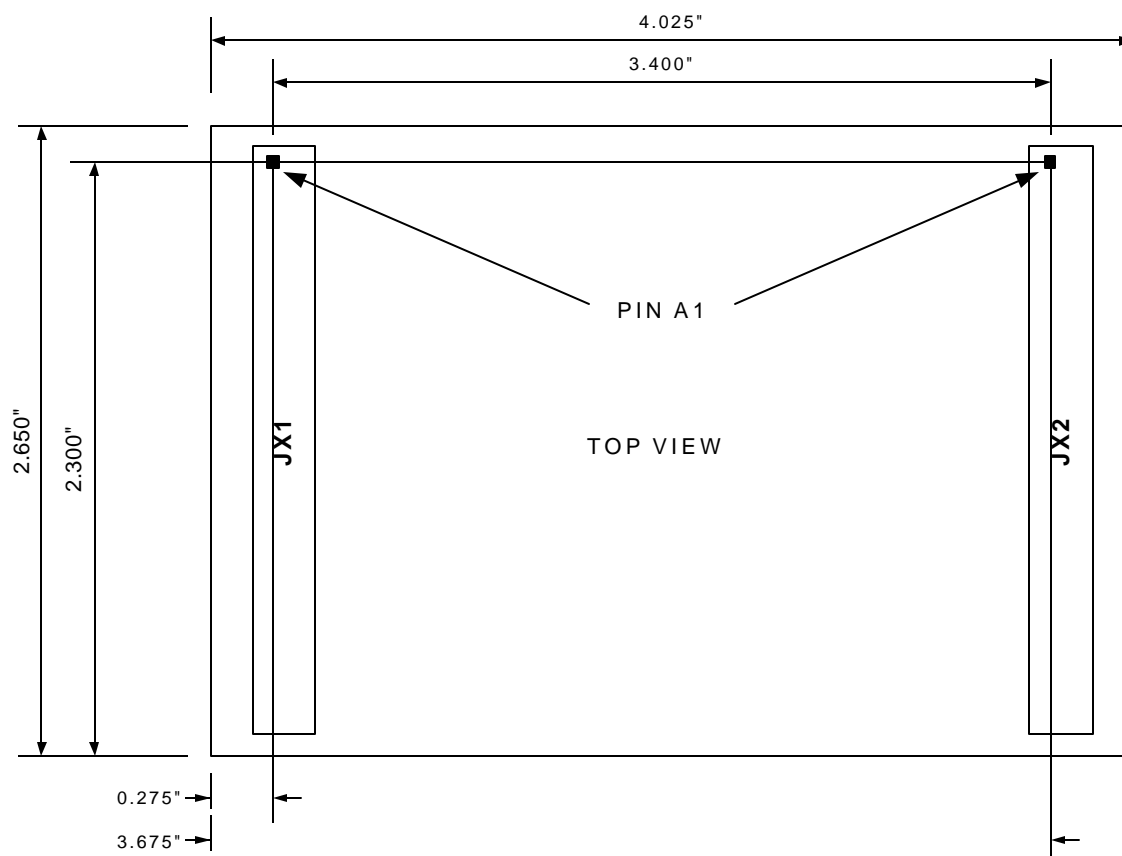


Figure 1 – Example P160 System Board

## 1.1 Mechanical Dimensions

The mechanical dimensions of the P160 I/O connectors along with the dimensions of the custom designed option module are shown in the following figure.



**Figure 2 – P160 Physical Dimensions**

The physical dimensions of the P160 board, shown above, guarantee inter-operability with all existing P160 slots. Some system boards may allow larger size modules to be created.

## 1.2 Connectors

The P160 module uses two 80-pin, low insertion force connectors to connect the P160 expansion module to the main system board. The connectors are relatively inexpensive (~\$3.00) and can support operating frequencies in excess of 100MHz. The details of this connector are provided below:

Part Number  
FX2C-80S-1.27DSAL

Manufacturer  
Hirose

The part listed above is a thru hole style which offers maximum reliability. SMT versions of this connector are also available. The mating connector that resides on the system board is the FX2C-80P-1.27DSAL. For additional information on this connector see Appendix A for the complete data sheet or visit:

[http://www.hirose.com/Products/Product\\_Cat\\_PDF/PDF%20files/FX2%20Cat\\_1001.pdf](http://www.hirose.com/Products/Product_Cat_PDF/PDF%20files/FX2%20Cat_1001.pdf)

### 1.3 Signal Descriptions

The following two tables provide a brief description of the I/O connector signals connected to each of the P160 connectors.

**Table 1 – JX1 Left User I/O Connector**

Type	Signal Name	JX1 Pin #		Signal Name	Type
RESERVED	RESERVED	A1	B1	FPGA.BITSTREAM	INPUT
	<b>GND</b>	A2	B2	SM.DOUT/BUSY	I/O
RESERVED	RESERVED	A3	B3	FPGA.CCLK	INPUT
	<b>Vin</b>	A4	B4	DONE	INPUT
RESERVED	RESERVED	A5	B5	INITn	I/O
	<b>GND</b>	A6	B6	PROGRAMn	INPUT
RESERVED	RESERVED	A7	B7	NC	NC
	<b>3.3V</b>	A8	B8	LIOB8	I/O
I/O	LIOA9	A9	B9	LIOB9	I/O
	<b>GND</b>	A10	B10	LIOB10	I/O
I/O	LIOA11	A11	B11	LIOB11	I/O
	<b>2.5V</b>	A12	B12	LIOB12	I/O
I/O	LIOA13	A13	B13	LIOB13	I/O
	<b>GND</b>	A14	B14	LIOB14	I/O
I/O	LIOA15	A15	B15	LIOB15	I/O
	<b>Vin</b>	A16	B16	LIOB16	I/O
I/O	LIOA17	A17	B17	LIOB17	I/O
	<b>GND</b>	A18	B18	LIOB18	I/O
I/O	LIOA19	A19	B19	LIOB19	I/O
	<b>3.3V</b>	A20	B20	LIOB20	I/O
I/O	LIOA21	A21	B21	LIOB21	I/O
	<b>GND</b>	A22	B22	LIOB22	I/O
I/O	LIOA23	A23	B23	LIOB23	I/O
	<b>2.5V</b>	A24	B24	LIOB24	I/O
I/O	LIOA25	A25	B25	LIOB25	I/O
	<b>GND</b>	A26	B26	LIOB26	I/O
I/O	LIOA27	A27	B27	LIOB27	I/O
	<b>Vin</b>	A28	B28	LIOB28	I/O
I/O	LIOA29	A29	B29	LIOB29	I/O
	<b>GND</b>	A30	B30	LIOB30	I/O
I/O	LIOA31	A31	B31	LIOB31	I/O
	<b>3.3V</b>	A32	B32	LIOB32	I/O
I/O	LIOA33	A33	B33	LIOB33	I/O
	<b>GND</b>	A34	B34	LIOB34	I/O
I/O	LIOA35	A35	B35	LIOB35	I/O
	<b>2.5V</b>	A36	B36	LIOB36	I/O
I/O	LIOA37	A37	B37	LIOB37	I/O
	<b>GND</b>	A38	B38	LIOB38	I/O
I/O	LIOA39	A39	B39	LIOB39	I/O
	<b>Vin</b>	A40	B40	LIOB40	I/O

**Table 2 – JX2 Right User I/O Connector**

Type	Signal Name	JX2 Pin #		Signal Name	Type
I/O	RIOA1	A1	B1	<b>GND</b>	
I/O	RIOA2	A2	B2	RIOB2	I/O
I/O	RIOA3	A3	B3	<b>Vin</b>	
I/O	RIOA4	A4	B4	RIOB4	I/O
I/O	RIOA5	A5	B5	<b>GND</b>	
I/O	RIOA6	A6	B6	RIOB6	I/O
I/O	RIOA7	A7	B7	<b>3.3V</b>	
I/O	RIOA8	A8	B8	RIOB8	I/O
I/O	RIOA9	A9	B9	<b>GND</b>	
I/O	RIOA10	A10	B10	RIOB10	I/O
I/O	RIOA11	A11	B11	<b>2.5V</b>	
I/O	RIOA12	A12	B12	RIOB12	I/O
I/O	RIOA13	A13	B13	<b>GND</b>	
I/O	RIOA14	A14	B14	RIOB14	I/O
I/O	RIOA15	A15	B15	<b>Vin</b>	
I/O	RIOA16	A16	B16	RIOB16	I/O
I/O	RIOA17	A17	B17	<b>GND</b>	
I/O	RIOA18	A18	B18	RIOB18	I/O
I/O	RIOA19	A19	B19	<b>3.3V</b>	
I/O	RIOA20	A20	B20	RIOB20	I/O
I/O	RIOA21	A21	B21	<b>GND</b>	
I/O	RIOA22	A22	B22	RIOB22	I/O
I/O	RIOA23	A23	B23	<b>2.5V</b>	
I/O	RIOA24	A24	B24	RIOB24	I/O
I/O	RIOA25	A25	B25	<b>GND</b>	
I/O	RIOA26	A26	B26	RIOB26	I/O
I/O	RIOA27	A27	B27	<b>Vin</b>	
I/O	RIOA28	A28	B28	RIOB28	I/O
I/O	RIOA29	A29	B29	<b>GND</b>	
I/O	RIOA30	A30	B30	RIOB30	I/O
I/O	RIOA31	A31	B31	<b>3.3V</b>	
I/O	RIOA32	A32	B32	RIOB32	I/O
I/O	RIOA33	A33	B33	<b>GND</b>	
I/O	RIOA34	A34	B34	RIOB34	I/O
I/O	RIOA35	A35	B35	<b>2.5V</b>	
I/O	RIOA36	A36	B36	RIOB36	I/O
I/O	RIOA37	A37	B37	<b>GND</b>	
I/O	RIOA38	A38	B38	RIOB38	I/O
I/O	RIOA39	A39	B39	<b>Vin</b>	
I/O	RIOA40	A40	B40	RIOB40	I/O



#### 1.4 Power Budget

The P160 derives its voltages and current from the system board that it plugs into. Because of this, the P160 specification does not set a standard for the maximum current draw allowed for each voltage supply. It is up to the P160 module designer to guarantee that a P160 module will not over-load the main system board supplies. This is further complicated by the fact that many of the FPGA based system boards draw current that is design dependent. For this reason, each P160 module should clearly define the current requirement for each of the supplies required. An example guideline for this is shown in Table 3 below.

**Table 3 – P160 Power Budgets**

Supply	Comments
5.0V	The 5V supply is often used to generate the 2.5V and 3.3V supplies on the main system board. Therefore, when looking at the 5V power budget, be sure to include the other supply requirements in this calculation. Keeping the P160 5V supply to less than 500 mA is recommended.
2.5V	Keeping the P160 2.5V supply to less than 500 mA is recommended.
3.3V	Keeping the P160 3.3V supply to less than 1 A is recommended.

## 2 Revisions

Version 1.0	Initial Release	12/5/01
Version 1.1	Updated with connector part number information	6/2/02
Version 1.2	Modified Table 1 to change JTAG connections to Reserved	10/16/02
Version 1.3	Updated Figure 2 with additional dimensions	11/18/02

## **Appendix A - Hirose Data Sheet**