

P160 Analog Module User Guide



**Version 1.0
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PN# DS-MANUAL-ANALOG1



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1 About this Kit

The Memec Design P160 Analog Module provides an advanced analog interface to existing P160 compatible FPGA platforms. The module enables designers to easily implement dual channel analog input and output functions, targeting communications, video and general-purpose mixed-signal applications. With two 12-bit analog-to-digital (A/D) converters capable of sample speeds up to 53MSPs and two digital-to-analog (D/A) converters capable of 165MSPs conversions, the module offers flexibility and ease of use to FPGA-based DSP applications and prototyping. The P160 Analog Module is ideally suited as an add-on for the Memec Design MB1000 Virtex-II Development Kit and the 2VP4/7 Virtex-II Pro Development Kit. The module will also work with the Spartan-II 200PCI and Spartan-II E 300 platforms from Memec Design.

The Memec Design P160 Analog Module kit includes the following:

- MBEXP3 P160 Analog Module
 - o 2 12-bit 53-MSPs A/D converters
 - o AC coupled, single-ended, 1 to 1.5 V_{p-p} analog input
 - o Low pass input filter with $f_c = 19.4$ MHz
 - o 2 12-bit 165 MSPs D/A converters
 - o Single-ended, 2 V_{p-p} analog output
 - o AC coupled output optional
 - o Low pass output filter with $f_c = 28.4$ MHz
- Documentation CD

2 The P160 Analog Module

The P160 Analog Module is comprised of four independent analog channels, two supporting analog inputs and two supporting analog outputs. The analog input channels are identical in design and include signal conditioning analog front ends. The Texas Instruments ADS807 12-bit, 53MSPs A/D converters are used to convert incoming analog signals into 12-bit data for the FPGA located on the baseboard. Analog outputs can be generated using the two DAC902 12-bit, 165MSPs D/A converters from Texas Instruments. Gain and filtering is provided on the D/A outputs.

Control of the A/Ds and D/As is handled by the FPGA through the P160 digital interface. Sample clocks, data, reference voltage settings, and power down control are examples of some of the control signals available. Two external clock inputs are provided on the P160 Analog Module, allowing clock inputs to be routed down to the FPGA and then back up to the D/As or A/Ds.

The analog front-ends to both the D/A channels and A/D channels are designed to accommodate a wide variety of applications. Customization of the front-end gain and frequency response characteristics is possible through the change of certain resistor and capacitor values. If electing to make such changes, care must be taken to ensure circuit stability. Read the device data sheets thoroughly to understand the recommended design parameters.

Figure 1 shows the P160 Analog Module.

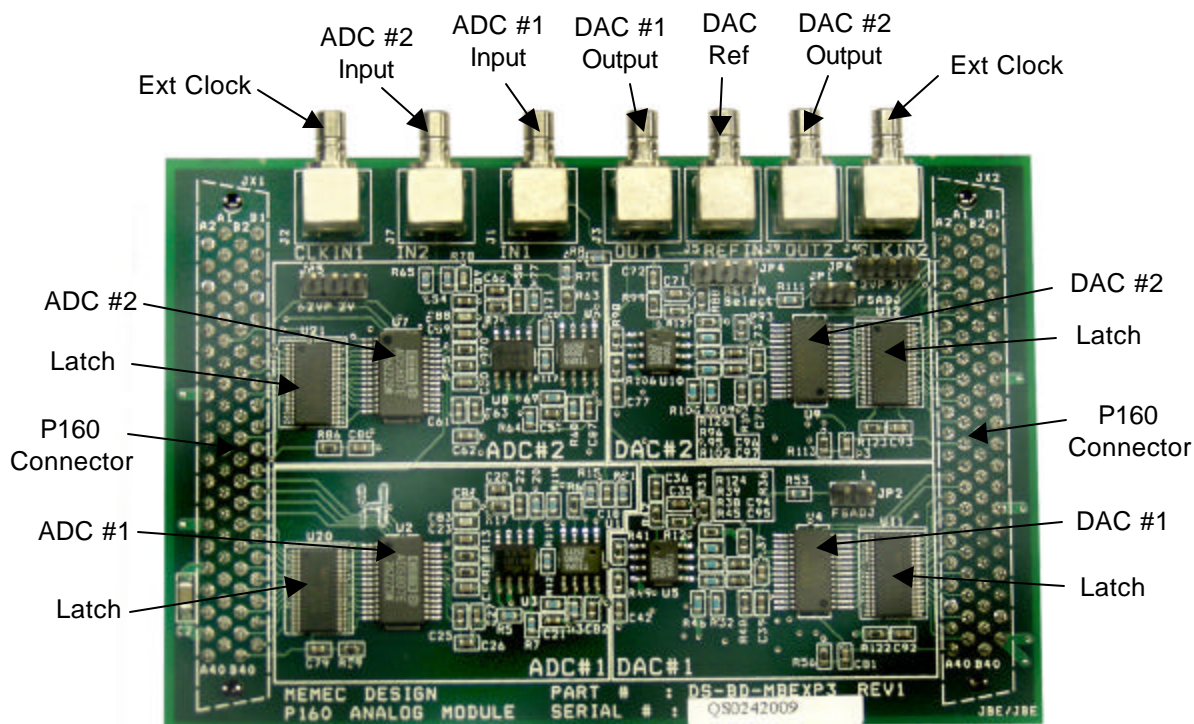


Figure 1 – P160 Analog Module

All the analog inputs and outputs are available along the topside of the module through the SMB type connectors. The P160 connections along the left and right sides of the board connect the digital signals between the FPGA based board and the register and control pins on the Analog Module. A high-level block diagram of the P160 Analog Module is shown in Figure 2, followed by a brief description of each board function.

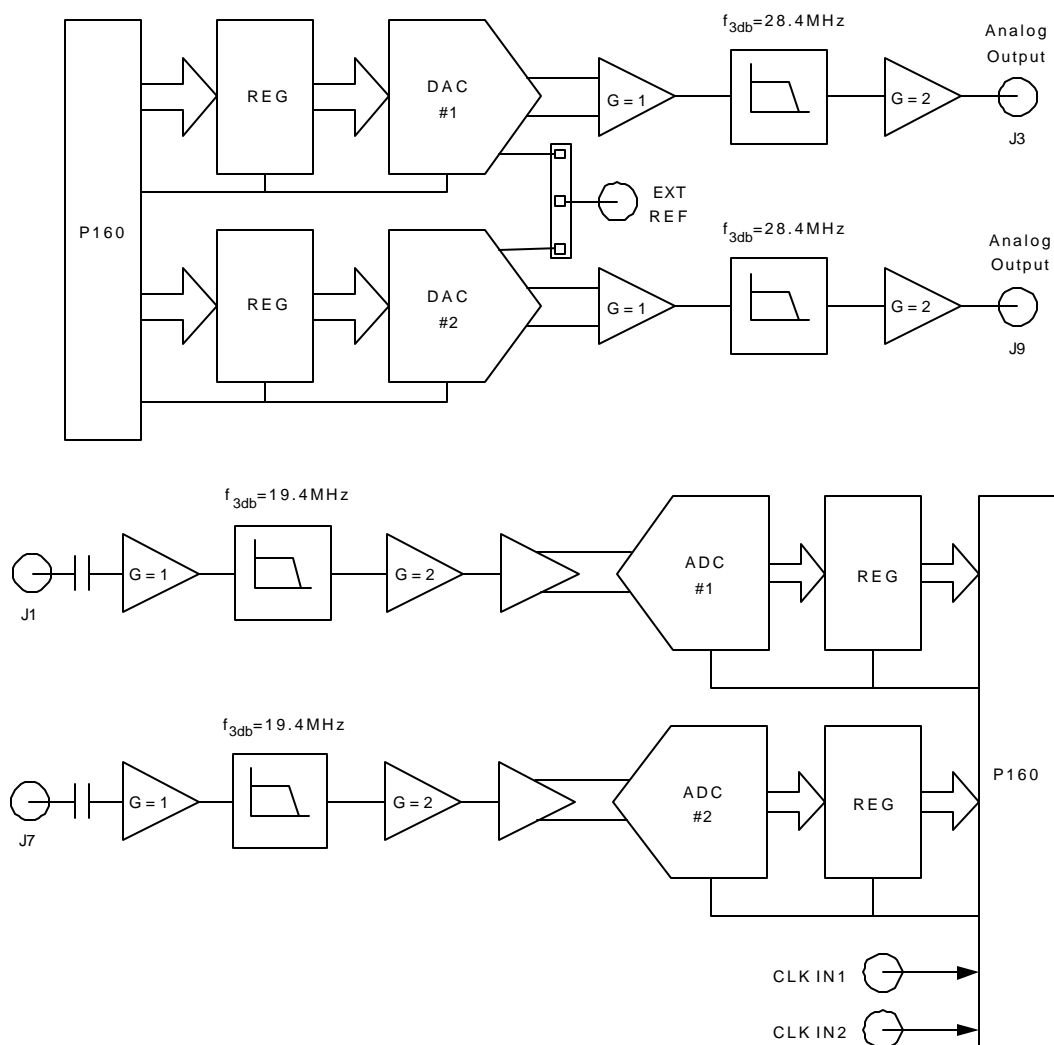


Figure 2 – P160 Analog Module Block Diagram

2.1 D/A Converters

Two digital-to-analog converters provide single-ended analog outputs from the P160 Analog Module. The Texas Instruments DAC902 delivers 12-bit resolution at 165Mps with differential outputs for improved dynamic performance. The FPGA interfaces to the D/As through 12-bit registers, which add a clock cycle delay between data out from the FPGA and the D/A analog outputs. Two independent data channels, one channel for each DAC, are driven from the FPGA to the P160 connector and into the register.

Table 1 shows the P160 interface signals for DAC #1 and Table 2 shows the interface signals for DAC #2.

Table 1 – DAC #1 P160 Interface

Signal	JX2 P160 Connector	Description
DB1	A39	DAC input data bit 11 (MSB)
DB2	A38	DAC input data bit 10
DB3	A37	DAC input data bit 9
DB4	A36	DAC input data bit 8
DB5	A35	DAC input data bit 7
DB6	A34	DAC input data bit 6
DB7	A33	DAC input data bit 5
DB8	A32	DAC input data bit 4
DB9	A31	DAC input data bit 3
DB10	A30	DAC input data bit 2
DB11	A29	DAC input data bit 1
DB12	A28	DAC input data bit 0 (LSB)
DB13	A27	(Unused)
DB14	A26	(Unused)
CLK	A40	DAC Clock (rising edge active)
CLK2	A23	Register Clock
REFSELECT	A25	Reference Select (Low = Internal, High = External)
PD	A24	Power Down (Low = Normal, High = Power Down)

Table 2 – DAC #2 P160 Interface

Signal	JX2 P160 Connector	Description
DB1	A19	DAC input data bit 11 (MSB)
DB2	A18	DAC input data bit 10
DB3	A17	DAC input data bit 9
DB4	A16	DAC input data bit 8
DB5	A15	DAC input data bit 7
DB6	A14	DAC input data bit 6
DB7	A13	DAC input data bit 5
DB8	A12	DAC input data bit 4
DB9	A11	DAC input data bit 3
DB10	A10	DAC input data bit 2
DB11	A9	DAC input data bit 1
DB12	A8	DAC input data bit 0 (LSB)
DB13	A7	(Unused)
DB14	A6	(Unused)
CLK	A21	DAC Clock (rising edge active)
CLK2	A3	Register Clock
REFSELECT	A5	Reference Select (Low = Internal, High = External)
PD	A4	Power Down (Low = Normal, High = Power Down)

2.1.1 DAC Signal Flow

The DAC input data is defined such that DB1 is the MSB data and DB12 is the LSB data. Two additional data bits are included in the FPGA interface for possible expansion to 14-bit offerings in the DAC900 family. Data values and corresponding output values are shown below.

Table 3 – DAC Input Data

Input Code DB1 <-> DB12	DAC Output (J3/J9)
1111 1111 1111	3.5V
1000 0000 0000	2.5V
0000 0000 0000	1.5V

The DAC output seen at J3 and J9 is normally DC coupled for a 2 V peak-to-peak (Vp-p) signal centered at 2.5 V. Current to voltage conversion, gain, and filtering is provided at the output of the DAC chip as shown in the following figures. The diagrams presented reflect the component designators for the DAC#1 channel.

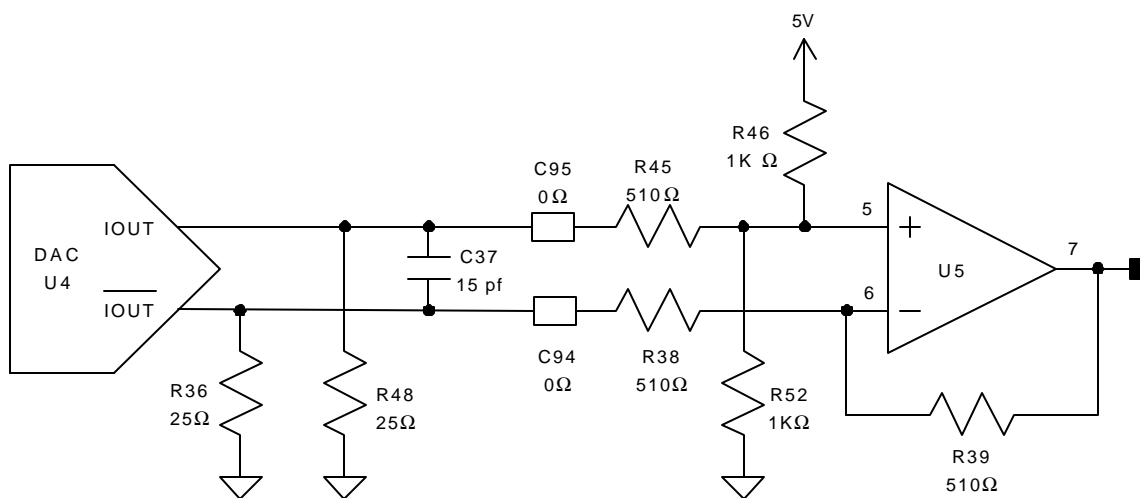


Figure 3 – DAC #1 Difference Amplifier Configuration

The DAC has two complementary current outputs with a nominal current range of 0 mA to 20 mA. As shown, the DAC generates a differential output signal of .5 Vp-p at the load resistors, R36 and R48. The difference amplifier stage level shifts the .5 Vp-p DAC outputs to a 2.5 V bias and provides a unipolar, single-ended output with a 1 Vp-p swing.

The capacitor locations C94 and C95 can be populated with .1 uf devices for improved AC performance. The default setting has C94 and C95 set with 0 ohm jumpers, providing enhanced DC performance.

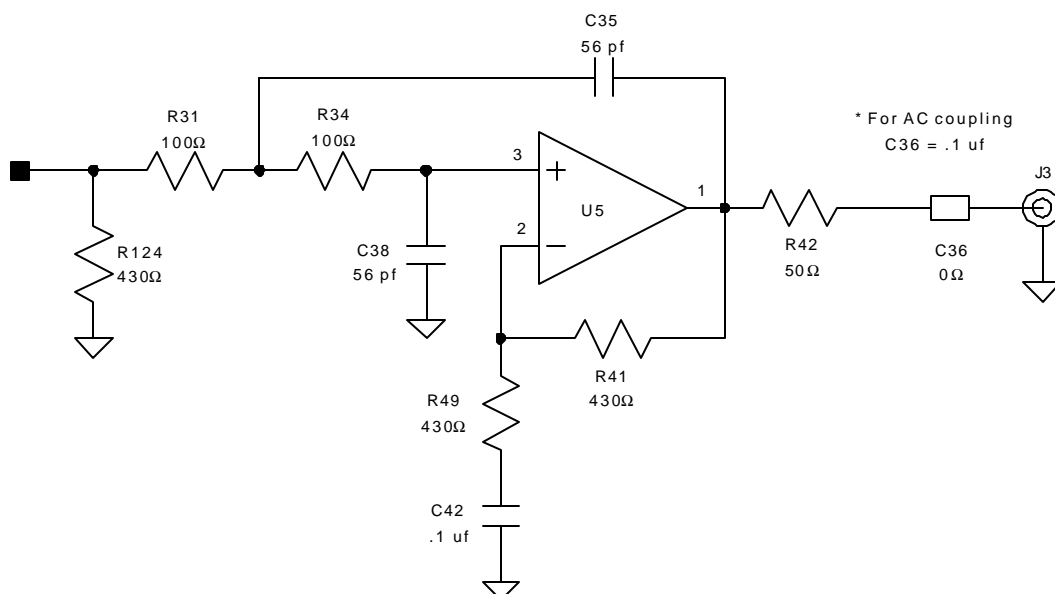


Figure 4 – DAC #1 Filter and Gain Output Stage

The final output stage incorporates an active two-pole Sallen-Key low pass filter set for a 3-db frequency of 28.4MHz. (Additional filter design theory can be found in the Sallen-Key application note included on the CD). The gain of the circuit is set at $G = 2$, resulting in a 2 Vpp output signal centered at 2.5 V. It is possible to modify this circuit to adjust the gain and the 3-db frequency as shown below.

$$G = \frac{R49 + R41}{R49} = 2$$

Figure 5 – DAC Low Pass Filter Gain

Table 4 – DAC Gain Adjust Values

DAC #1			DAC #2		
R41	R49	Gain	R98	R106	Gain
430 Ω	430 Ω	2	430 Ω	430 Ω	2
403 Ω	806 Ω	1.5	403 Ω	806 Ω	1.5
510 Ω	340 Ω	2.5	510 Ω	340 Ω	2.5

$$f_c = \frac{1}{2\pi(R31R34C35C38)^{1/2}} = 28.4 \text{ MHz}$$

Figure 6 – DAC Low Pass Filter 3-db Frequency

Table 5 – DAC Low Pass Filter Adjust Values

DAC #1				
R31	R34	C35	C38	f_c
100 Ω	100 Ω	56 pf	56 pf	28.4 MHz
28.9 Ω	120 Ω	100 pf	56 pf	36 MHz
33.7 Ω	150 Ω	100 pf	56 pf	30 MHz

DAC #2				
R88	R91	C71	C74	f_c
100 Ω	100 Ω	56 pf	56 pf	28.4 MHz
28.9 Ω	120 Ω	100 pf	56 pf	36 MHz
33.7 Ω	150 Ω	100 pf	56 pf	30 MHz

By default, the analog outputs are DC coupled through 0 ohm jumpers in locations C36 on DAC #1 channel and C72 on DAC #2 channel. Replacing these jumpers with .1 uf capacitors will result in an AC coupled output.

2.1.2 Full Scale Adjust Jumpers JP1 and JP2

The Full Scale Adjust jumpers (JP1 and JP2) are normally closed when using the internal 1.24 V bandgap reference. Connecting an external reference voltage to the D/A via the REF Input connector and setting jumper JP4 to select one of the DACs, may require jumper JP1 or JP2 to be removed. See the “Internal Reference Operation” section of the DAC902 Data Sheet for further details on configuring the full scale adjust.

2.1.3 DAC External Reference

The DAC902 has an on-chip reference circuit that is normally enabled through low inputs on the DAC1.REFSELECT and DAC2.REFSELECT. The internal reference can be disabled by driving one of these inputs high and applying an external reference voltage at J5. Jumper JP4 must also be set with a jumper to connect the external reference to the desired DAC REF pin. The table below explains the jumper settings.

Table 6 – DAC REF Select Jumper (JP4)

JP4	Description
OPEN	Internal REF active
1 - 2	External REF connected to DAC #1
2 - 3	External REF connected to DAC #2

2.1.4 DAC Clocking

Each DAC channel requires 2 clock signals to latch digital data into the DAC. DAC1.CLK/DAC2.CLK and DAC1.CLK2/DAC2.CLK2 come from the FPGA and are rising-edge triggered. The *.CLK2 signals latch the digital DAC data from the FPGA into the P160 register. The *.CLK signals latch the output data from the register into the DAC. On the falling edge of the *.CLK signal, the DAC output changes to the newly latched value.

2.2 A/D Converters

Two analog-to-digital converters are included on the P160 Analog Module. These Texas Instruments ADS807 converters provide 12-bit resolution at up to 53 Msps. The digital data out of the A/Ds is latched into external buffers and then passed to the FPGA through the P160 interface. The tables below show the P160 interface between the P160 registers and the FPGA.

Table 7 – ADC #1 P160 Interface

Signal	JX1 P160 Connector	Description
DB1	B28	ADC output data bit 0 (MSB)
DB2	B29	ADC output data bit 1
DB3	B30	ADC output data bit 2
DB4	B31	ADC output data bit 3
DB5	B32	ADC output data bit 4
DB6	B33	ADC output data bit 5
DB7	B34	ADC output data bit 6
DB8	B35	ADC output data bit 7
DB9	B36	ADC output data bit 8
DB10	B37	ADC output data bit 9
DB11	B38	ADC output data bit 10
DB12	B39	ADC output data bit 11 (LSB)
FSSEL	B27	Full Scale Select (Low = 2Vpp, High = 3Vpp)
REFSEL	B25	Reference Select (Low = Internal, High = External)
OEn	B24	Output Enable (Low = Enabled, High = Tri-Stated)
CLK	B40	Convert Clock (rising edge active)

Table 8 – ADC #2 P160 Interface

Signal	JX1 P160 Connector	Description
DB1	B10	ADC output data bit 0 (MSB)
DB2	B11	ADC output data bit 1
DB3	B12	ADC output data bit 2
DB4	B13	ADC output data bit 3
DB5	B14	ADC output data bit 4
DB6	A25	ADC output data bit 5
DB7	B16	ADC output data bit 6
DB8	B17	ADC output data bit 7
DB9	A27	ADC output data bit 8
DB10	B19	ADC output data bit 9
DB11	B20	ADC output data bit 10
DB12	B21	ADC output data bit 11 (LSB)
FSSEL	B9	Full Scale Select (Low = 2Vpp, High = 3Vpp)
REFSEL	B23	Reference Select (Low = Internal, High = External)
OEn	A11	Output Enable (Low = Enabled, High = Tri-Stated)
CLK	B22	Convert Clock (rising edge active)

2.2.1 A/D Signal Flow

Figure 7 shows the first stage of the analog input channel.

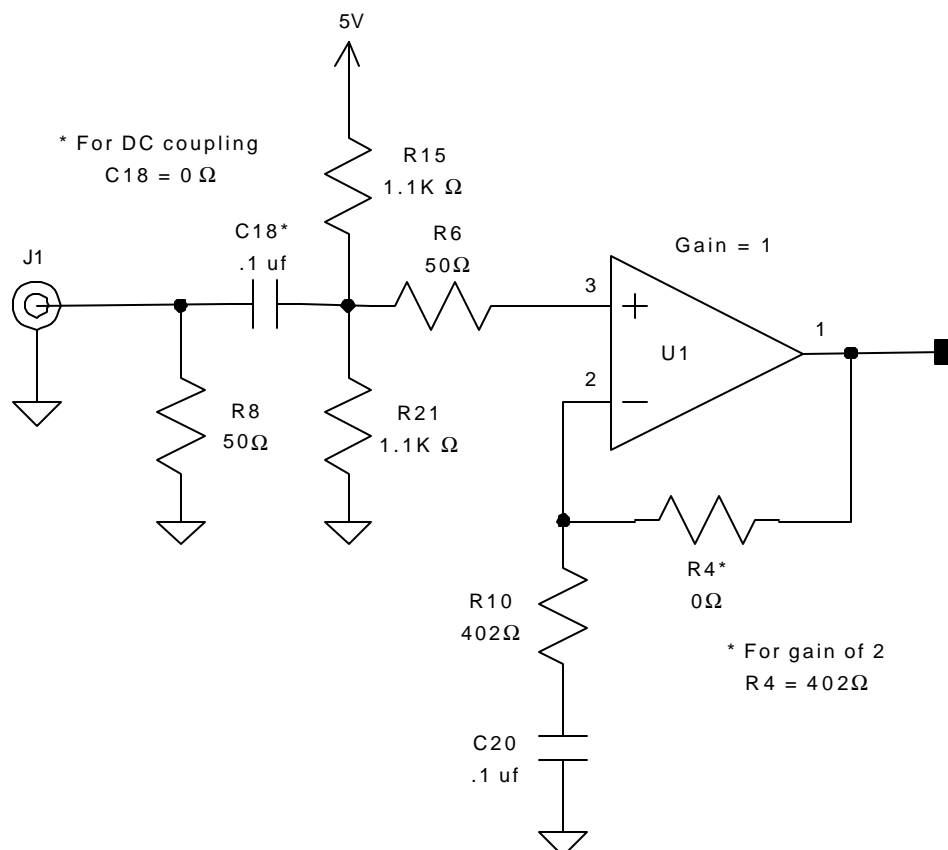


Figure 7 – Analog Input Stage

An analog signal with amplitude 1 Vp-p or 1.5 Vp-p is applied to J1 for ADC #1 or to J7 for ADC #2. The input has a 50 ohm termination through R8 and R65. The input signal is AC coupled, biased to 2.5 volts for unipolar operation, and buffered through the op amp. Low-level analog inputs can be amplified by adjusting the gain setting of this front-end op amp circuit. As shown, the gain is defined as:

$$G = \frac{R10 + R4}{R10} = 1$$

Changing R4 (ADC #1) and R61 (ADC #2) to 402 ohms would result in a gain = 2. This would limit the analog input to a .5 Vp-p range. The range of the input signal is dependant on the Full Scale Select control signal to the A/D. Setting this signal to a logic high, enables 3 Vp-p inputs to the A/D, which corresponds to a 1.5 Vp-p input to the board. Setting the Full Scale Select to low, selects a 2 Vp-p range into the A/D and a 1 Vp-p input range to the board.

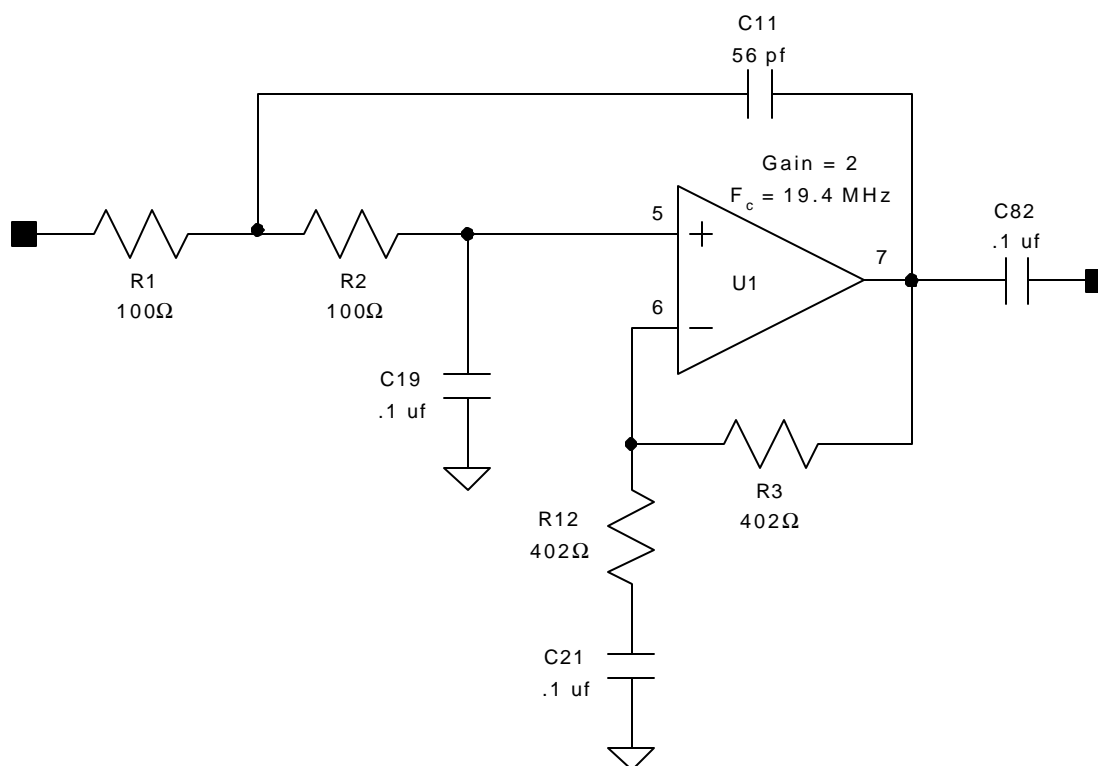


Figure 8 – Analog Filter Stage

The second op-amp stage incorporates an active two-pole Sallen-Key low pass filter set for a 3-db frequency of 19.4MHz. The gain of the circuit is set at $G = 2$, resulting in a 2 Vpp output signal centered at 2.5 V. It is possible to modify this circuit to adjust the gain and the 3-db frequency as shown below.

$$G = \frac{R12 + R3}{R12} = 2$$

Figure 9 – ADC Low Pass Filter Gain

Table 9 – ADC Gain Adjust Values

ADC #1			ADC #2		
R3	R12	Gain	R60	R69	Gain
402 Ω	402 Ω	2	402 Ω	402 Ω	2
402 Ω	804 Ω	1.5	402 Ω	804 Ω	1.5
510 Ω	340 Ω	2.5	510 Ω	340 Ω	2.5

$$f_c = \frac{1}{2\pi(R_1R_2C_{11}C_{19})^{1/2}} = 19.4 \text{ MHz}$$

Figure 10 – ADC Low Pass Filter 3-db Frequency

Table 10 – ADC Low Pass Filter Adjust Values

ADC #1				
R1	R2	C11	C19	f_c
100 Ω	100 Ω	56 pf	120 pf	19.4 MHz
120 Ω	100 Ω	56 pf	56 pf	26 MHz
120 Ω	100 Ω	120 pf	120 pf	12.1 MHz

ADC #2				
R58	R59	C47	C55	f_c
100 Ω	100 Ω	56 pf	56 pf	28.4 MHz
28.9 Ω	120 Ω	100 pf	56 pf	36 MHz
33.7 Ω	150 Ω	100 pf	56 pf	30 MHz

The Texas Instruments THS4150 Differential Amplifier is used to convert the intermediate single-ended analog input signal into a differential signal for final input into the A/D. Figure 11 shows the circuit used.

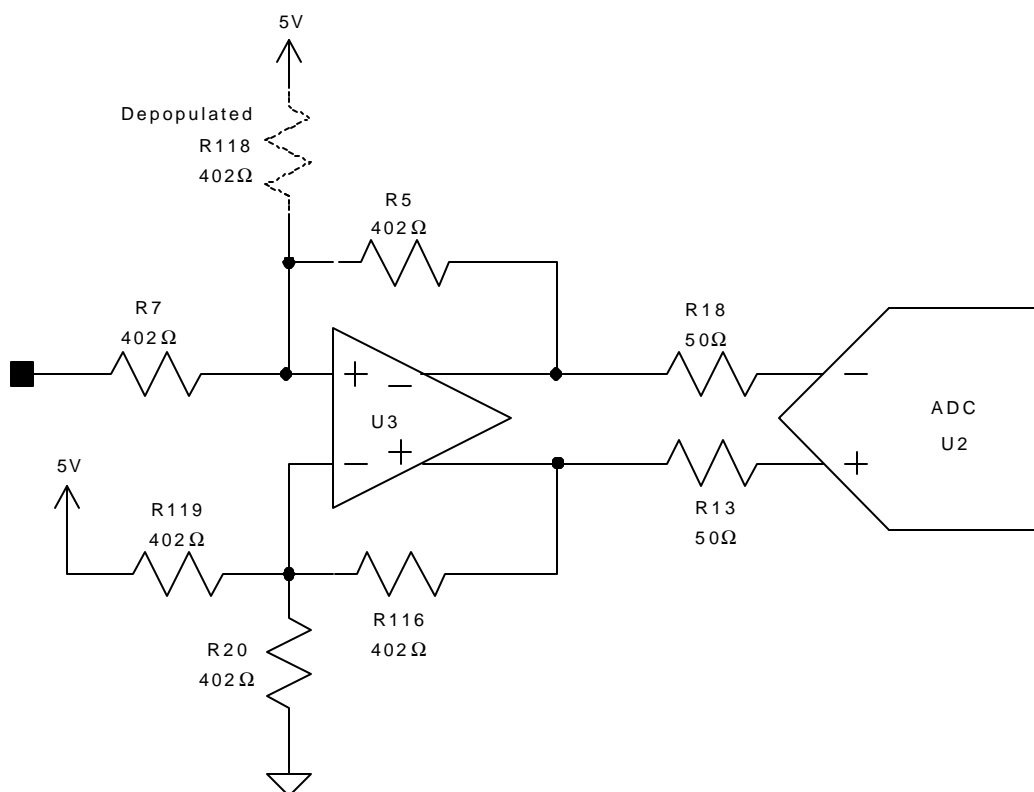


Figure 11 – ADC Differential Amplifier

2.2.2 A/D Data Format

The 12-bit digital data output from the ADS807 is a positive straight offset binary code as shown in the table below.

Table 11 – ADC Output Values

ADC Input	Offset Binary Output
+5V	1111 1111 1111
0V	1000 0000 0000
-5V	0000 0000 0000

2.2.3 A/D Clocking

The ADS807 samples the input signal on the rising edge of the CLK input. Output data values are valid at the A/D outputs 6 clock cycles later, after the rising edge of the clock. It is important that this clock have minimal jitter, close to a 50% duty cycle and fast rise and fall times of 2ns or less.

2.2.4 A/D Full Scale Select

The ADS807 can be configured for a differential full-scale input range of either 2 Vp-p or 3 Vp-p. The **ADC1.FSSEL** and **ADC2.FSSEL** control signals from the FPGA control the setting of this input range.

Table 12 – ADCx.FSSEL Control

FSSEL	Description
LOW	2 Vp-p input range
HIGH	3 Vp-p input range

2.2.5 A/D Internal Reference

The ADS807 has an internal reference source that can be enabled or disabled through the FPGA control signal **ADC1.REFSEL** and **ADC2.REFSEL**.

Table 13 – ADCx.REFSEL Control

REFSEL	Description
LOW	Internal reference selected
HIGH	External reference selected

2.2.6 A/D Over-Range Indicator

If the analog input voltage exceeds the full-scale range of the A/D, the **ADC1.OTR** and **ADC2.OTR** signal will go high. OTR is updated along with the output data that corresponds to the sampled analog input voltage. Therefore, the OTR data is subject to the same 6-clock cycle pipeline delay as the digital data.

2.3 External Clock Inputs

The P160 Analog Module includes two external clock input connectors, J2 and J4. These clock inputs are 50 ohm terminated and can be used to drive the clock inputs to the baseboard FPGA. Two jumpers, JP5 and JP6 are used to jumper the corresponding clock inputs to one of two FPGA pins. To achieve optimum performance, the clock input signals should connect to global clock input pins on the FPGA. Jumpers JP5 and JP6 allow for selection of global clock input pins to either the Virtex-II MB1000 baseboard or the Virtex-II Pro P4/P7 baseboard. Table 14 and 15 shows the jumper settings.

Table 14 – JP5 External Clock Settings

J2 External Clock Input			
JP5 Pins	Description	P160 Pin	FPGA Pin
2-3 closed	J2 Clock input set for MB1000 platform	JX2-A20	AB12
1-2 closed	J2 Clock input set for Virtex-II Pro platform	JX1-A39	E12

Table 15 – JP6 External Clock Settings

J4 External Clock Input			
JP6 Pins	Description	P160 Pin	FPGA Pin
2-3 closed	J2 Clock input set for MB1000 platform	JX2-B14	Y12
1-2 closed	J2 Clock input set for Virtex-II Pro platform	JX1-B15	F12

When connecting to the Spartan-II 200 PCI or Spartan-II E platforms, regular I/O pins must be used for these clock inputs since global clock inputs are not available. The jumper settings for either of these baseboards are arbitrary.

2.4 P160 Connectors

A P160 format of the Analog Module allows the board to be interchanged with any of the P160 compatible baseboards from Memec Design. However, due to the external global clock input routing, the Memec Design Virtex-II MB1000 and Virtex-II Pro P4/P7 platforms are the ideal choices.

The P160 interface used on the Analog Module is 3.3 V compatible, so the 3.3 V bank setting should be chosen on the baseboard when connecting to the Analog Module. The following tables show the pin assignments to the P160 Analog Module connectors (JX1 and JX2).

Table 16 – P160 Connector – JX1

P160 CONNECTOR	BOARD NAME --> REVISION -->	MB1000 REV1	2S200PCI REV2	S2E REV1	2VPx REV2
JX1 PIN	SIGNAL NAME	FPGA PIN NUMBER			
A9	NC	K22	E16	D16	F18
A11	ADC2.OEn	J21	E15	C16	H20
A13	NC	G22	E14	D15	E11-GCLK*
A15	NC	F21	F12	C15	F11-GCLK*
A17	NC	D22	C10	D14	F10*
A19	NC	C21	D10	B16	D9*
A21	NC	L20	B8	E14	B11*
A23	NC	K19	A7	B15	E10*
A25	ADC2.DB6	H20	B7	AA20	G19
A27	ADC2.DB9	G19	B6	C13	F20
A29	NC	F20	A5	E13	F19
A31	NC	F19	B5	C12	E20
A33	NC	D11-GCLK	A4	V17	C10*
A35	NC	C11-GCLK	B4	Y18	D10*
A37	NC	C8	A3	W18	E19
A39	CLKIN1.2VP	D8	B3	B12	E12-GCLK
B8	ADC2.OTR	L22	B19	D17	G18
B9	ADC2.FSSEL	L21	A19	C17	E17
B10	ADC2.DB1	K21	B18	C18	E16
B11	ADC2.DB2	J22	A18	D18	E15
B12	ADC2.DB3	H22	B17	B19	E14
B13	ADC2.DB4	H21	A17	A19	F14
B14	ADC2.DB5	G21	A16	B18	F13
B15	CLKIN2.2VP	F22	B15	A18	F12-GCLK
B16	ADC2.DB7	E22	A15	B17	H22
B17	ADC2.DB8	E21	B14	A17	H21
B18	NC	D21	A14	AB20	G22
B19	ADC2.DB10	C22	B13	A16	G21
B20	ADC2.DB11	L18	A13	AB21	F22
B21	ADC2.DB12	L19	B12	A15	F21
B22	ADC2.CLK	K18	C18	B14	E22
B23	ADC2.REFSEL	K20	D17	A14	E21
B24	ADC1.OEn	J20	C17	B13	D22
B25	ADC1.REFSEL	J19	D16	A13	D21
B26	ADC1.OTR	H19	C16	C14	C22
B27	ADC1.FSSEL	G20	D15	D13	C21
B28	ADC1.DB1	E19	C15	E12	D18
B29	ADC1.DB2	E20	D14	D12	D17
B30	ADC1.DB3	L17	C14	A12	D16
B31	ADC1.DB4	K17	D13	E17	C16
B32	ADC1.DB5	J17	C13	E16	D15
B33	ADC1.DB6	J18	E13	E15	C15
B34	ADC1.DB7	H18	C12	AA18	D14
B35	ADC1.DB8	G18	D12	F14	D13
B36	ADC1.DB9	F18	E12	F13	C13
B37	ADC1.DB10	E18	C9	F12	E13
B38	ADC1.DB11	E11	D9	Y19	B12
B39	ADC1.DB12	A10	C8	AB19	G20
B40	ADC1.CLK	B10	D8	AA19	H19

* FPGA pins are dedicated to 2.5 V signal levels

Table 17 – P160 Connector – JX2

P160 CONNECTOR	BOARD NAME --> REVISION -->	MB1000 REV1	2S200PCI REV2	S2E REV1	2VPx REV2
JX2 PIN	SIGNAL NAME	FPGA PIN NUMBER			
A1	NC	AB18	V14	AB18	J21
A2	NC	AA16	Y14	AA16	J22
A3	DAC2.CLK2	AA17	W13	AA17	K21
A4	DAC2.PD	AB16	Y18	AB16	K22
A5	DAC2.REFSELECT	AB17	Y13	AB17	L21
A6	DAC2.DB14	AA15	Y17	AA15	M21
A7	DAC2.DB13	W17	V13	W17	N22
A8	DAC2.DB12	AB15	Y16	AB15	P22
A9	DAC2.DB11	Y17	Y12	Y17	P21
A10	DAC2.DB10	AA14	Y15	AA14	R22
A11	DAC2.DB9	W16	V12	W16	R21
A12	DAC2.DB8	AB14	AB20	AB14	T22
A13	DAC2.DB7	Y16	V11	Y16	T21
A14	DAC2.DB6	AA13	AA19	AA13	U22
A15	DAC2.DB5	V16	W11	V16	U21
A16	DAC2.DB4	AB13	AB18	AB13	V22
A17	DAC2.DB3	W15	V10	W15	V21
A18	DAC2.DB2	AA12-GCLK	AB17	AB11	W22
A19	DAC2.DB1	V14	Y10	V14	W21
A20	CLKIN1.2V	AB12-GCLK	AA15	AA11	Y22
A21	DAC2.CLK2	U14	W10	U14	Y21
A22	NC	AB9	AA14	AB9	AA22
A23	DAC1.CLK2	U13	Y9	U13	R20
A24	DAC1.PD	AA9	AA13	AA9	R19
A25	DAC1.REFSELECT	U12	W9	U12	T20
A26	DAC1.DB14	AB8	AA12	AB8	T19
A27	DAC1.DB13	U11	Y8	U11	U20
A28	DAC1.DB12	AA8	AB10	AA8	U19
A29	DAC1.DB11	U10	W8	U10	V20
A30	DAC1.DB10	AB7	AB9	AB7	V19
A31	DAC1.DB9	U9	Y7	U9	M17
A32	DAC1.DB8	AA7	AB8	AA7	N17
A33	DAC1.DB7	V9	W7	V9	P17
A34	DAC1.DB6	AB6	AA7	AB6	P18
A35	DAC1.DB5	V8	Y6	V8	R18
A36	DAC1.DB4	AA6	AA6	AA6	T18
A37	DAC1.DB3	V7	W6	V7	U18
A38	DAC1.DB2	AB5	AA5	AB5	AB21
A39	DAC1.DB1	V6	W5	V6	N21
A40	DAC1.CLK	AA5	AA4	AA5	H18
B2	NC	Y15	W18	Y15	J18
B4	NC	W14	W17	W14	J17
B6	NC	Y14	W16	Y14	K17
B8	NC	W13	W15	W13	L17
B10	NC	Y13	W14	Y13	J19
B12	NC	V13	AA20	V13	J20
B14	CLKIN2.2V	Y12-GCLK	AA18	Y12	K19
B16	NC	W12-GCLK	AA17	W12	K20
B18	NC	V12	AB16	V12	K18
B20	NC	V10	AB15	V10	L20
B22	NC	Y10	AB14	Y10	L19
B24	NC	W10	AB13	W10	L18
B26	NC	Y9	AB11	Y9	M18
B28	NC	W9	AA10	W9	M19

P160 CONNECTOR	BOARD NAME --> REVISION -->	MB1000 REV1	2S200PCI REV2	S2E REV1	2VPx REV2
JX2 PIN	SIGNAL NAME	FPGA PIN NUMBER			
B30	NC	Y8	AA9	Y8	M20
B32	NC	W8	AA8	W8	N18
B34	NC	Y7	AB6	Y7	N20
B36	NC	W7	AB5	W7	N19
B38	NC	Y6	AB4	Y6	P20
B40	NC	W6	AB3	W6	P19

3 Revisions

V1.0 Initial release for Rev 1 board

October 31, 2002