A Prototype System and Circuits for the Development of an Implantable H-bridge Stimulator ASIC in a Bulk CMOS Process

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Abstract

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The opportunity to introduce nanometer sized circuits and systems into the body to treat or cure mental disorders, physical injuries, and genetic disabilities has put us at the forefront of a burgeoning industry. Implantable stimulators have the potential to save the lives, or drastically improve the quality of life, of millions of patients that currently are subject to disorders for which there are few, insufficient, or ineffective treatment options. However, much work must be done to reduce the size, cost, and power demands of stimulator SoCs, whilst also extending the voltage range over which the stimulator regulates the flow of charge through the body. Stimulators today are often manufactured in a costly, specialized process, which precludes the addition of the supporting and control circuitry onto just a single chip. This work seeks to develop an implantable stimulator ASIC that is manufactured in a standard, low voltage, bulk CMOS process, which achieves a voltage compliance of approximately ±12 V.

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Acknowledgements

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1.0 Introduction

The explosive growth in the field of biomedical engineering over the past several decades is a trend that will undoubtedly continue into the future. The rapid technological advances that have occurred in the fields of electrical engineering, materials science, microelectromechanical systems (MEMs), and semiconductor physics have allowed for the creation of ultra-small form factor, low power, robust, and cost effective application specific integrated circuits (ASICs, or in general, ICs) that can perform complex operations. The understanding of the brain and nervous system by neurologists and medical researchers has advanced to the point where we can envision, and have already begun to implement, medical devices that aid or replace a biological modality that may have been damaged by an injury or disease. Neuroprosthetics and brain computer interfaces (BCIs) hold promise in dramatically altering the lives of millions of individuals affected by a wide range of disorders by marrying engineering with human anatomy, but this task is extremely complex for a variety of reasons, and there are a large number of challenges that must be addressed and solved before widespread adoption of BCIs becomes a reality. However, the results of well designed neuroprosthetics are far too great to ignore the challenges, and could open the door to a new era of "bioengineering".

A neural prosthesis, or neuroprosthetic, can be defined as a device designed to augment a motor, cognitive, or sensory ability that is damaged due to birth defect, injury, disease, or age. A brain computer interface is similar to a neuroprosthetic, but differs in that a BCI often connects the nervous system to another device, instead of the device connecting to the nervous system. The two terms are often used interchangeably, and for the sake of this thesis, will be functionally equivalent. At the core of a neuroprothesis is a stimulation system, designed to invoke a

response in the subject by electrically stimulating nerve tissue, and/or a recording system, which records neural activity to be analyzed, and is often used as a trigger mechanism for electrical stimulation in closed loop systems. This thesis focuses solely on the relevant topics of electrical stimulation of the nervous system, and will not focus on any technical aspects of neural recording, although it may be mentioned in the context of a complete neural system.

The applications of neural stimulation are so numerous, and the technology to perform that stimulation is in such a stage of infancy, that it is difficult to identify which holds the most potential. However, at a cursory glance, there appear to be upwards of tens of millions of people in the United States alone that could see a benefit from one form or another of electrical stimulation.

An often examined application of electrical stimulation is to persons that have suffered a head trauma, stroke, neurological disorder, or spinal cord injury that has induced a form of paralysis. The ideal stimulation system for these patients would be able to reanimate the movement of paralyzed limbs, as well as restore the somatosensory system feedback to and from those limbs, to return the patient to a normal state, which would have dramatic individual benefits in future employment opportunities, general mood and disposition, and life expectancy, and also societal benefits due to decreased long term hospitalization costs. The Christopher and Dana Reeve Foundation performed a comprehensive, randomly sampled telephone survey across the nation in 2008 that found that approximately 5.6 million people, or approximately 2% of the United States' population, reported that they were living with some form of paralysis (see Figure 1)[1].

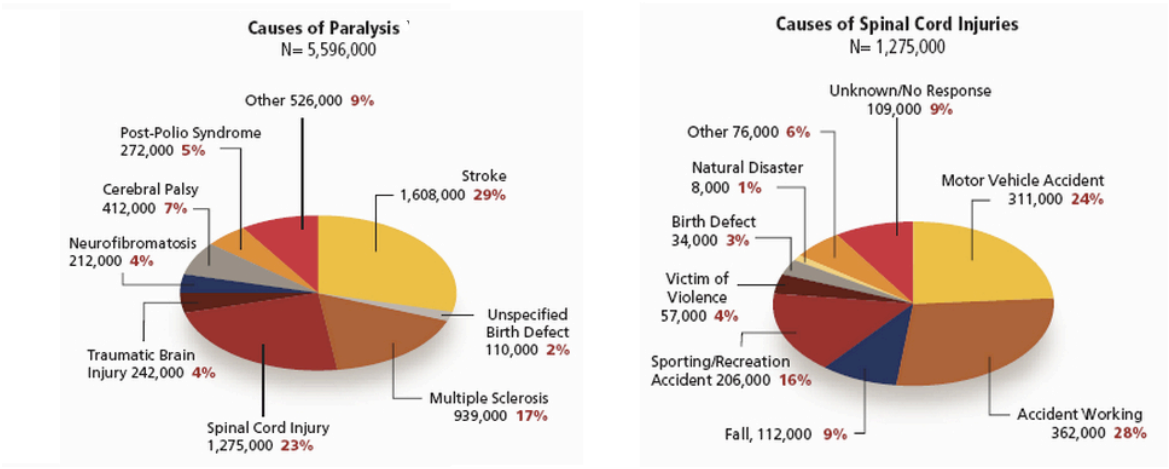
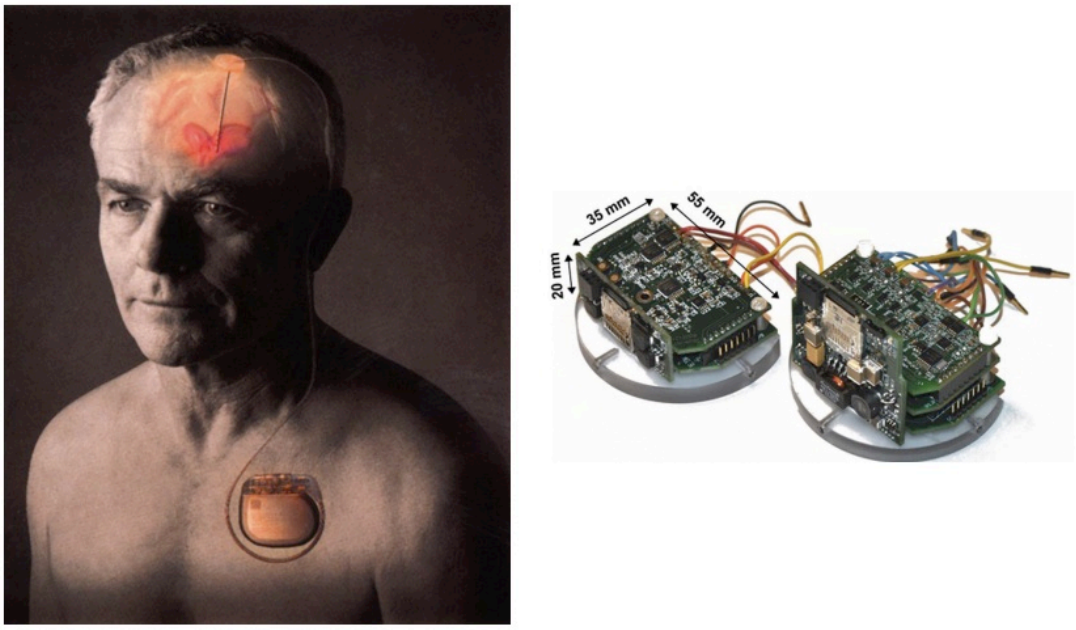


Figure 1: Causes of paralysis and SCI in the United States (Source: Christopher and Dana Reeves Foundation)

Deep brain stimulation (DBS) is another emerging technology that holds significant promise for the treatment of a large number of neurological disorders. In deep brain stimulation, a long electrode is placed into the structure of the brain responsible for the disorder, and a programmable current is used to modulate neural activity. Although its effects are not well understood, DBS has already been approved by the FDA for the treatment of Parkinson's disease, essential tremor, and dystonia. There are also ongoing studies for various neural diseases and disorders to determine if DBS is a valid treatment option, not limited to just those that incur motor dysfunction, such as depression, obesity, obsessive compulsive disorder, epilepsy, addictive behavior, and Tourette's syndrome.

Robust neural stimulator devices today are often comprised of a multitude of discrete components, configured to work together to achieve stimulation. This dramatically increases the size of the system, precluding its implantation at the stimulation site (or at all), and requiring long wires to reach the stimulation electrodes (see Figure 2). The drawbacks of such a system are obvious; additional trauma to the body, more potential points of failure from increased component count, power inefficiency from the increased component biases, and possibly the

exclusion of desired features due to size constraints. Thus, there is a clear push for a better solution.



(a) (b)

Figure 2: (a) Illustrated DBS system with electrode implanted in a subcortical target and connected to a subclavicular pulse generator (Source: Medtronic Inc.) (b) Two versions of the Neurochip-2, a stimulation and recording system designed for primate testing at the Univ. of Washington; the system sits in a can on top of the primate's skull (Source: [2])

Designing all of the circuits onto just a single chip appears to be a pathway to a better stimulation system. However, the high stimulation voltages generated in biphasic, constant current stimulators due to large, complex, and non-linear impedances[3,4,5] often limit the application of the stimulation system greatly, or require that the chip be fabricated in a high voltage tolerant process, like a silicon-on-insulator (SOI) technology or high voltage CMOS. The fabrication of the stimulation system in a high voltage process increases cost and makes the integration of low voltage digital control circuits with the high voltage analog circuits difficult, with designers often electing to put other circuit blocks, like the digital signal processing (DSP), wireless interfaces, power management, and neural recording on a separate, low voltage process

chip. Again, this increases neuroprosthesis system size, and is a multi-component solution. If high voltage tolerant circuits could be designed in a low voltage process, it would allow the integration of all circuits, digital and analog, onto just a single substrate. This is the primary challenge in designing a stimulation chip today, and the focus of this thesis is the design of a complete stimulation system that achieves that goal, which also includes a unique method to tolerate charge storage by the capacitance of the electrode-tissue interface.

Fundamentally, electrical stimulation works by injecting extracellular charge to a neuron to evoke an action potential. It is also important that there is zero net charge delivered into the body, as this can create a DC voltage that degrades the electrode and causes tissue damage due to redox reactions. Typically, there are three methods used to achieve this goal. Current mode stimulators actively regulate the charge delivered to the body through constant sink/source current sources. Biphasic current stimulators provide a regulated, anodic and cathodic current pulse to the body to accurately control the charge delivered. Monophasic current stimulators often provide a regulated sinking (or sourcing) current source and short the electrodes together to let the charge delivered passively dissipate. Voltage mode stimulators use a constant voltage source to push and pull current into and from the body. Lastly, charge mode stimulators charge and discharge capacitors to deliver and receive charge from the body. For an in depth comparison between the three types of stimulators, see [6].

Voltage mode stimulators are not often used due to the fact that electrode impedances are not well defined, and often change from electrode and electrode and over time, making it difficult to predict what the stimulation currents will be and the total charge delivered, rendering it unsafe for patients. Charge mode stimulators set an accurate amount of charge to deliver but often require large, off chip capacitors, rendering them too large. Current mode stimulators

(CMS) offer high safety and are more amenable to circuit design, making them the best option for a stimulation system. However, the main drawback of a CMS is its voltage compliance, which can be defined as the maximum voltage across the active and return electrode in which the current is regulated. The "current source" used in CMS is one or more transistors, which must be kept in saturation for the current to be regulated. As was discussed previously, the high electrode impedances present lead to large stimulation voltages, meaning extending the voltage compliance as much as possible is necessary.

As an example of a monophasic current stimulator with passive discharge, see the representative schematic in Figure 3(a) and [7], which is able to achieve a voltage compliance of just under 6 V. They do not specify the power supply voltage, but use an old process technology; 0.6 μm CMOS. By using a source regulated topology, the voltage compliance is limited to a maximum of approximately V_{device_max}. There is no solution to make this topology work in a low voltage process (i.e. sub-100 nm technology), where V_{device_max} is on the order of 1 to 2 V. A biphasic current stimulator is presented in [8] and its representative schematic shown in Figure 3(b). It was fabricated in a 0.6 μm BiCMOS process, and uses a supply voltage of 5 V. It is only able to reach a compliance voltage of ±2 V. Again, the transistor breakdown voltage of V_{device_max} limits the voltage compliance and makes this topology unusable for many applications and it cannot be extended to a process with smaller feature sizes. If the supply voltages were increased using charge pump techniques, the device breakdown limits would be exceeded on the sourcing current sources. With sourcing current sources, these approaches cannot be extended to achieve improved voltage compliance.

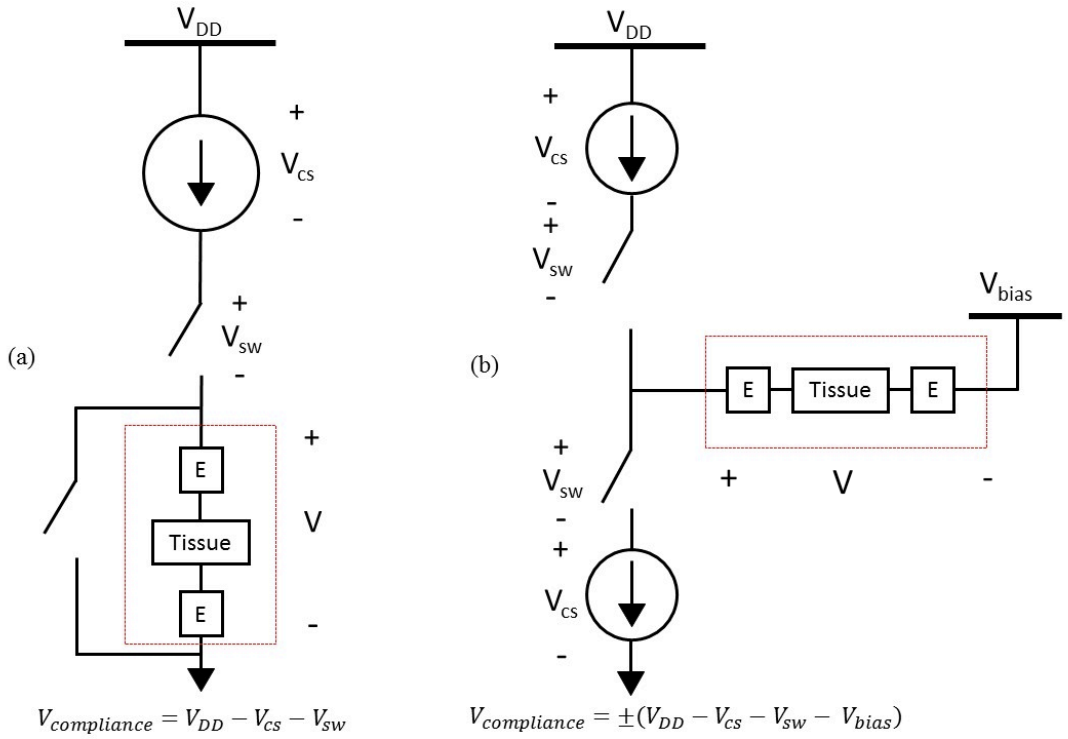


Figure 3: (a) A monophasic current mode stimulator with source regulation (b) A biphasic current mode stimulator with sink/source regulation

By using charge pump techniques to generate an elevated supply voltage greater than the chip V_{DD} and using only sinking current sources, improved voltage compliances can be realized when device stacking is employed and neither electrode is held to a fixed potential. This stimulator technique can be utilized to deliver biphasic stimulus currents through an H-bridge topology. Wren et. al. fabricated an integrated SoC in 0.18 μm CMOS that makes use of this stimulator topology (simplified schematic of the stimulator portion seen in Figure 4), which was able to achieve approximately ±9 V voltage compliance with a chip V_{DD} of just 1.8 V[9]. They used 3.3 V devices, but maximum stimulus current was just 30 μA. The voltage compliance is limited to non-arbitrary high voltages by the p-n junction breakdown limits of triple well NMOS transistors that are used to generate the high voltage rail (denoted in Figure 4 as HVDD). The system works by using feedback to increase HVDD when the current source is about to leave the

saturation region, keeping the current regulated and increasing the voltage compliance. An unaddressed issue of this design relates to the fact that there exists a capacitance between the electrode-tissue interface that often stores charge. When the stimulator switches from the cathodic to the anodic current pulse, charge stored across that capacitance will "lift" the voltage on the return electrode above HVDD, possibly causing unregulated (high) currents to run through the body and damaging the devices in the design. This is illustrated in Figure 5. The stimulation chip in this thesis was designed to solve that concern, which will be covered more in depth in later chapters.

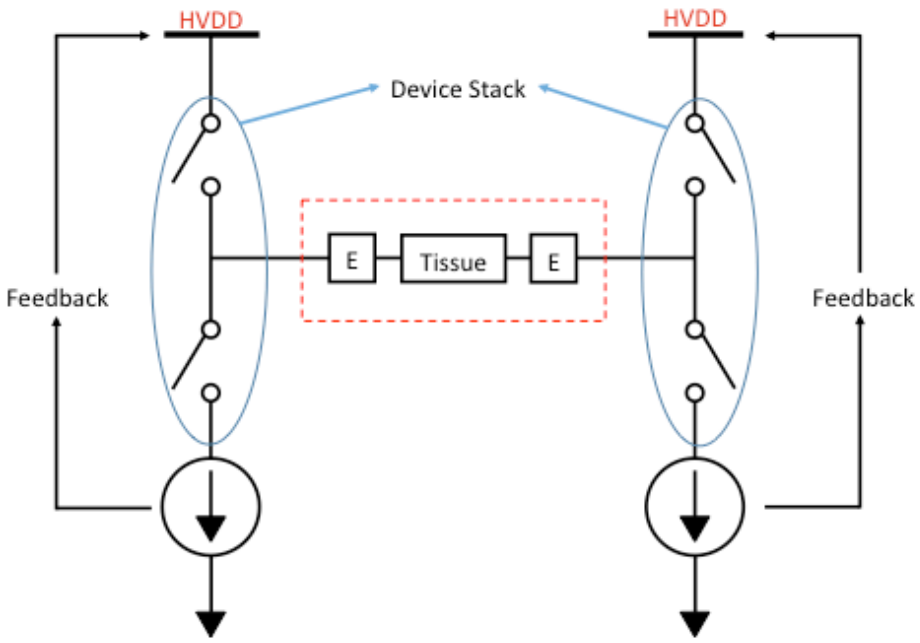


Figure 4: Schematic representation of the H-bridge stimulator topology used in [9]

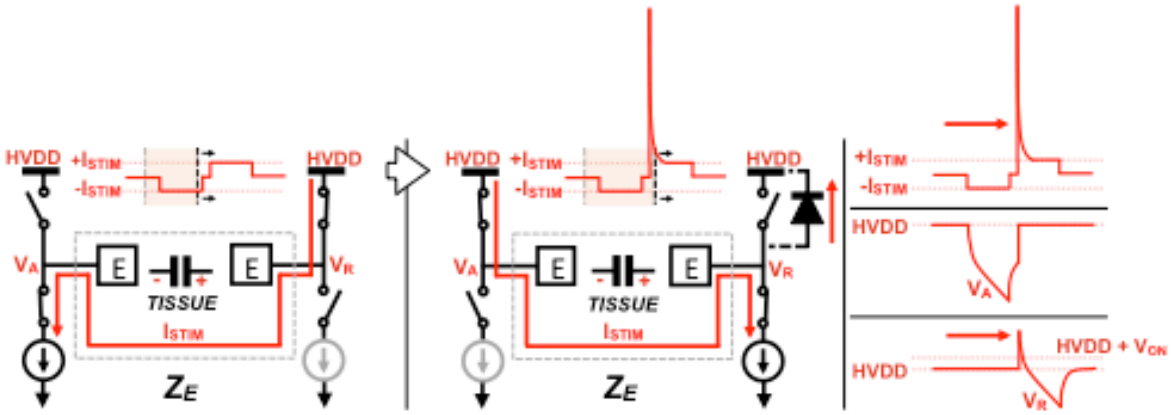


Figure 5: Illustration of a design concern in the H-bridge stimulation topology; unregulated current flows when switching from the cathodic to anodic current pulse

The subsequent chapters of this thesis will familiarize the reader with stimulation on a lower level and supply insight into the design process of circuits for a fabricated stimulation system chip. Chapter 2 will give context for the specific circuits developed, by describing the top level system and its functionality. Chapter 3 will cover the design and testing of a PCB that was made to emulate the stimulator system to verify proof of concept before proceeding with the chip design. Chapters 4 and 5 will cover the design, verification, and simulation results of circuit blocks that were used in the tapeout of the stimulator chip. Chapter 6 will summarize the findings and a discussion on the scope of future work.

2.0 Top Level System Description

The design of this neural stimulator was based around the goal of being able to drive a large range of biphasic, constant current waveforms through nearly any type of electrode impedances; from purely resistive to purely capacitive. It is difficult to predict electrode impedances (form this point on denoted as Z_E), which vary greatly depending on the type of electrodes used (i.e. the geometry of the electrode), the composition and surface material of the electrode, and the time after implantation[10]. Because of these reasons, it is necessary to design stimulator electronics that do not rely on any assumptions of the electrode impedances presented. The design, based around an H-bridge topology, utilizes a regulated discharge phase to account for "capacitive-looking" electrodes to ensure safe and predictable stimulation currents at all points in the stimulation waveform. The stimulation ASIC was designed in a low voltage, 65 nm bulk-CMOS technology, with the addition of 2.5 V I/O devices. It achieves a voltage compliance of approximately ±11 V through the use of two, integrated, switched-capacitor, dynamic voltage supplies (0-12 V), and a low voltage, programmable, eight bit current digital-to-analog-converter (DAC) with a LSB step size of 10 μA. A general overview of a stimulus event will be described in the proceeding section.

2.1 Stimulation Overview

This section is written to give the reader a conceptual understanding of the "states" that the stimulator goes through and the mechanisms it uses to achieve biphasic, constant current stimulation. It uses symbols to represent some components of the design for the sake of simplicity. The two stimulation electrodes in the body will henceforth be denoted as the "active" and "return" electrode, sometimes seen in figures as E_{ACTIVE} or E_A and E_{RETURN} or E_R, with

voltages at those nodes following the same naming convention. The active electrode is recognized by the fact that during a cathodal current pulse, the direction of electron flow is from electrode to tissue[10]. As mentioned earlier, a stimulation event typically occurs first with a cathodal current pulse that is realized as a negative current to the active electrode, followed by an anodal current pulse that is realized as a positive current.

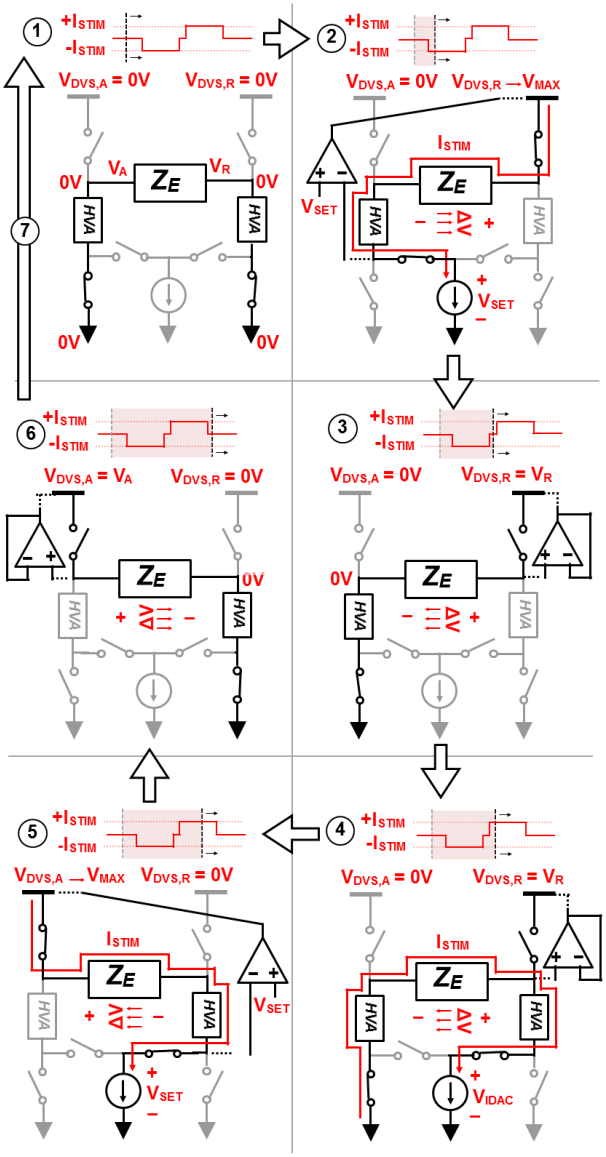


Figure 6: Biphasic constant-current driver state cycle (1-7) during a stimulus event

At the beginning of State 1, both electrodes are shorted to chip ground, and both dynamic voltage supplies (DVS) are at 0 V. There is zero net charge across the body from previous stimulus events, and zero current is being delivered. The stimulator spends most of its time in this state, and can be understood as a low-power, idle state. For the stimulus event shown in Figure 6, the active electrode is on the left, and the return electrode is on the right. This configuration is user selectable, so that either electrode can be "active".

At the onset of State 2, the cathodic current starts to be delivered to the body. The stimulus event could potentially be set by the user at specified intervals, or generated by an algorithm that is meant to detect a specified signal(s) through recording amplifiers. For testing purposes of this chip, no recording amplifiers are built onto it, although a stimulus event could be triggered by off-chip recording circuitry. The current amplitude is regulated by the low voltage current DAC (IDAC), and feedback ensures that the return DVS voltage is high enough to keep the IDAC in saturation. The feedback is modeled by an open loop op amp, i.e. a comparator, which generates a one bit error signal that is sent to the return DVS control logic. There are no instability concerns with this feedback because the DVS control logic only receives a signal that tells it to raise the voltage or keep it constant. Since the feedback is unidirectional and not bidirectional, this removes any potential for system oscillation. The non-inverting input of the comparator is biased at V_{SET}, which is the minimum output voltage of the IDAC required for high output impedance current regulation. The maximum voltage that the DVS can reach is approximately 12 V, which is limited to that value by the breakdown voltage of the p-n junction of a triple well NMOS device.

In the third state, a short period of time between the cathodic and anodic current pulses, known as the interphase delay, is used to ensure that the nerve membrane has ample time to

depolarize from the cathodic current pulse and reach the action potential threshold[11]. Z_E may have capacitive properties that allows for significant charge to be stored from the previous state, which could begin to self discharge in this state, so the return DVS is set to "track" the voltage on the return electrode through feedback. This is modeled by a voltage follower op amp configuration, although in reality it is implemented with a one bit signal from a comparator to the return DVS control logic. It is necessary for the return DVS to track the voltage on the return electrode because the DVS biases the devices in the return high voltage adapter (HVA), which ideally acts as a zero resistance switch while protecting the low voltage IDAC devices from the high voltages seen at the electrodes. The time constant associated with the discharge rate is often quite long, and the interphase delay is short, so the amount of self discharge is usually small.

State 4 is what makes this stimulator design unique in comparison to other H-bridge stimulator topologies[9]. In this state, the anodic current pulse begins, seen as a positive current to the active electrode. However, in contrast to State 2, in which the current was supplied from the return DVS, the flow of charge in this state is wholly from the discharge of Z_E, which may have charge stored across it from the capacitive looking electrodes. The current is regulated through the IDAC, and the return DVS voltage tracks the falling electrode voltage to keep the return HVA properly biased. V_R will eventually fall beyond the minimum output voltage required by the IDAC to keep the current regulated, at which point the control logic will force the system to proceed to the next state.

State 5 is nearly identical to State 2, with the only difference being that current flows in the opposite direction. The anodic current pulse is continued, whilst feedback from a one bit comparator to the active DVS control logic ensures that the IDAC is kept in saturation. The charge in this state is supplied by the active DVS.

Nearing the end of a stimulus event, State 6 is analogous to State 3, in which one electrode is shorted to chip ground, and the other electrode is allowed to passively self discharge, while feedback is employed to ensure that the active DVS voltage tracks the active electrode voltage. State 7 is left as a blank state for which the designer can choose a method to ensure charge is properly balanced. This may be performed by shorting of the electrodes after a specified number of stimuli, or through the use of additional (small) stimulus pulses. The intention of this design was to test the stimulation architecture, so proper testing will most likely utilize off chip electrode shorting, in conjunction with a DC blocking capacitor for safety, which is a common method used in stimulation applications.

2.2 General System Overview

The delivery of the biphasic current through the state cycle relies on the coordinated operation of both the active and return DVSs working in conjunction with feedback and control circuits to deliver positive current through tissue. The collection of feedback, control circuits, and a DVS will be defined as a positive-current driver (PCD). Each PCD has three operating modes; IDLE, TRACK, and SUPPLY, with feedback being used in the latter two modes. To minimize the number of charge pump stages and maximize efficiency, all of the circuits in the stimulus current path utilize the process I/O devices, which allow the use of a boosted V_{DD}, up to 2.5 V. The block diagram of the active PCD can be seen in Figure 7, and the following sections will describe key blocks.

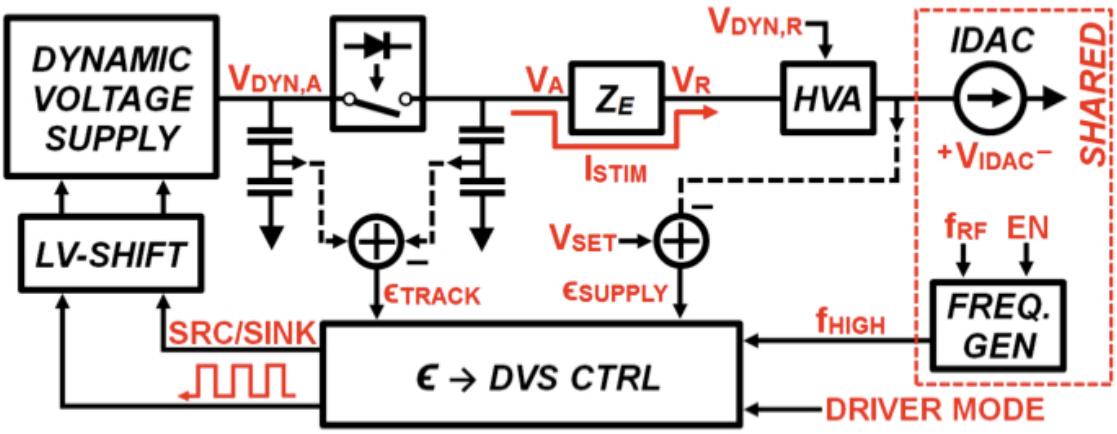


Figure 7: Active positive-current driver (PCD); return PCD is identical, but with complementary active/return connections

The DVS is a cascade of switched capacitor blocks which can source current up to a V_{MAX} of approximately 12 V when the PCD is in SUPPLY mode, and sink current down to 0 V when unloaded and in TRACK mode. The magnitude of the current flowing in/out of the DVS to a large, output storage capacitor (internal to the DVS block in Figure 7) is controlled by the pulse signal frequency and the direction is controlled by the SRC/SINK signal. The charge flowing through the DVS to the storage capacitor results in the DVS acting as a variable voltage source.

The HVA is required to protect the low voltage IDAC from the high voltages seen at the electrode. It is designed to operate as a closed or open switch, depending on the state of the stimulus event. It is comprised of stacked, triple-well NMOS devices, which are biased by the DVS on the same side of the H-bridge. A series capacitor string, with each capacitor having a voltage-locking diode in parallel, safely distributes the bias voltage across the NMOS gates. When the DVS voltage is too low to bias the devices in the HVA, chip V_{DD} takes over that operation to enforce the high conduction required of the HVA.

The IDAC can be realized with low voltage devices and topologies because of the HVAs. The magnitude of the current is programmable, which is necessary because of the large variance in stimulus currents required for different applications. It needs a high output impedance to ensure that the current during the entire cathodic and anodic pulses is constant. Another important specification is that the IDAC possesses a small minimum output voltage, as it directly reduces the voltage compliance of the stimulator.

There exists a direct trade off in the number of charge pump stages required in the DVS and the pulse frequency necessary to supply high stimulus currents at high voltages. The number of charge pump stages in the DVS necessitates relatively high pulse frequencies (>100 MHz), which are generated on-chip via an integer PLL. This frequency synthesizer also generates the clocks for the feedback comparators. Due to the fact that the PCDs will primarily be in IDLE mode, this PLL can often be put to sleep to conserve power.

There are two feedback loops within the stimulator system, which send information to the DVS control logic to control the direction and number of pulses passed (i.e. average pulse period) to the DVS in different states. Each pulse passed to the DVS results in a ΔV at $V_{DYN,A}$; by knowing where in the state cycle the PCD is, the SRC/SINK supply control (which determines the ΔV sign) can be reliably set. Referring to Figure 7, error signals ε_{TRACK} and ε_{SUPPLY} are generated by comparators, which act as one-bit A/D converters. In SUPPLY mode, the high side switch is closed, and $\varepsilon_{SUPPLY} = V_{IDAC} - V_{SET}$. The DVS must source current in this mode, which requires pulses passed to it to increase the DVS output voltage ($+\Delta V$), with the number of pulses passed to it being controlled by the feedback loop to produce a $V_{DYN,A}$ which maintains V_{IDAC} at V_{SET} (which is slightly above the minimum output voltage of the IDAC). In TRACK mode, the high side switch is open, and $\varepsilon_{TRACK} = (V_{DYN,A} - V_A)/K$, where K is a

constant set by the capacitive divider ratio. The feedback is applied to make $V_{DYN,A}$ track V_A, which is falling in this mode, so the DVS must sink current ($-\Delta V$); why this is necessary will be apparent after the next section.

The high side switches in Figures 5 and 6 are implemented with a diode. Knowledge of the stimulus current direction and the described feedback scheme adequately ensures that the diode models a switch. To force the "switch" to be "open", feedback enforces an (ideal) zero voltage across the diode such that no current will flow. When the "switch" is "closed", feedback ensures that the DVS voltage is high enough to sink the current demanded by the IDAC. The primary drawback with using a diode as a switch is that when it is "closed", its resistance is nearly zero, but there exists a small voltage drop across it that is subtracted from the voltage compliance. However, the diode is an elegant solution to the problem of how to create a high side HVA, as there is no equivalent for PMOS devices to a triple well NMOS device.

The circuits I designed for the stimulator chip were the eight-bit IDAC, the integer-divider PLL for frequency synthesis, and the feedback comparators. The design, testing, and simulation results of these circuits will come in later chapters. Another graduate student was in control of top-level system design, the HVAs, and the DVSs. For more information on those circuits, see [12].

3.0 Board Level Design and In-Vivo Testing

The end goal of this stimulator chip is for it to be used for medical research purposes by research scientists at the University of Washington and its collaborators; to further the field of electrical stimulation and recording and the understanding of the neurobiology of humans and animals as a whole. A unique benefit of working at the University of Washington is the close proximity to the research scientists that this project is designed to aid, such as neurophysiologists and neurosurgeons. They are often well versed in using benchtop stimulators and provide concise design specifications and what their needs are in a stimulation device. Before proceeding with a long design cycle and costly chip tapeout, it was identified that it would be prudent to verify that the H-bridge stimulator topology could work in stimulating tissue, the voltage compliances reached by the stimulator chip (~11 V) would be sufficient, and also what the desired range of stimulation currents would need to be for various stimulation applications. This is possible given the low frequency operation of any neural interface system, thus allowing a board implementation that would emulate the proposed chip-level architecture. A prototype H-bridge stimulator was designed using high voltage tolerant discrete components and implemented on a printed circuit board (PCB) to answer the preceding questions about the feasibility of the stimulator topology. The design concerns were addressed by performing in-vivo tests for several stimulation applications and verifying functional stimulation.

3.1 Functions of the Prototype System

After consulting with a research group that often performs controlled animal testing using electrical stimulation with implanted electrodes, several design specifications were identified that allow the prototype stimulator to achieve functional stimulation. The amplitude and duration of

the cathodic and anodic current pulses was required to be easily programmable, as they may vary by orders of magnitude for different applications (e.g. spinal versus muscle stimulation). The number of pulses and the pulse period was also required to be easily programmable, in addition to several other variables. Research scientists often achieve stimulation by performing quick "bursts" of stimulation, where there are several small stimulus events in a short period of time, followed by a long period of time that allows the tissue to "rest". All of the stimulation variables, with their relative names, can be summarized in Figure 8. All of the stimulation variables are easily edited by either changing variable values in C code or on supporting benchtop equipment.

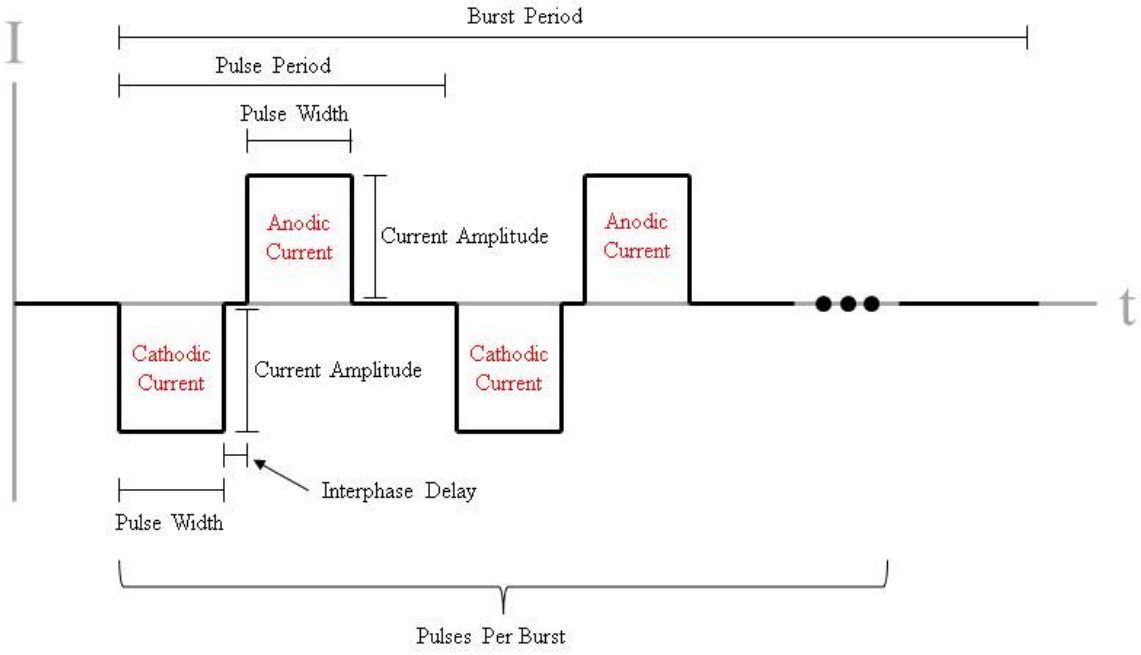


Figure 8: Programmable stimulus current waveform and corresponding variables

3.2 Top Level Block Diagram

A block diagram of the prototype H-bridge stimulator system as a whole, including supporting benchtop equipment, can be seen in Figure 9. At a high level, it uses a microcontroller to oversee the timing of control signals that are sent from the microcontroller to the H-bridge stimulator PCB (henceforth known as the HB-PCB). The HB-PCB is composed of low resistivity, high voltage tolerant analog switches that can be opened and closed from CMOS logic level voltages. The analog switches are employed to steer current through the body in a cathodic first, anodic second fashion. The current is regulated from a benchtop current source unit with a large, programmable current range and a low minimum voltage. The laptop is used to program the microcontroller and provide power for it. Lastly, the voltage supplies provide bias points and are the power rails that source and sink the stimulus currents.

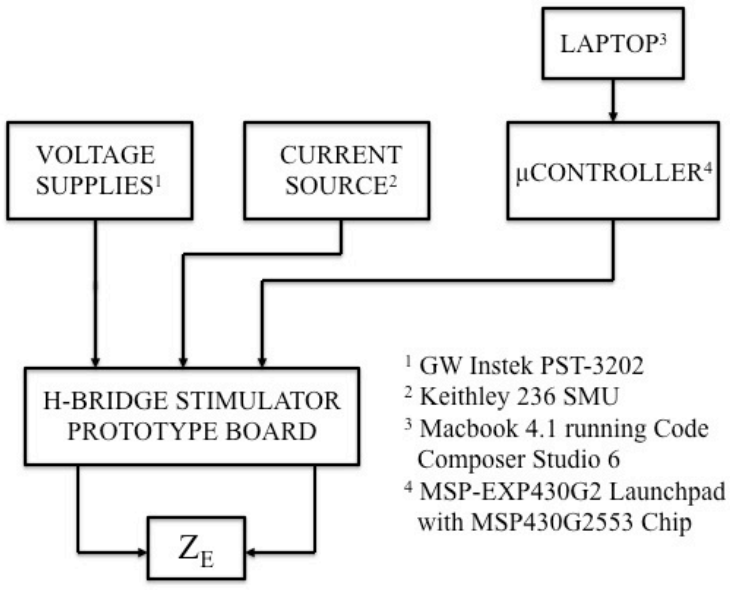


Figure 9: Prototype H-bridge stimulator system block diagram

3.3 Prototype H-Bridge Stimulator Schematic and Operation

The prototype H-bridge stimulator, although similar to the design implemented in the stimulator ASIC, does not accurately model the entire system of the chip. However, the primary features implemented in the stimulator ASIC are still present, and the functionality should be equivalent. The V_{DD} of the prototype system could be set arbitrarily high by the benchtop equipment (as opposed to the upper limit of 12 V on the chip), and the discrete switches were able to withstand high voltages across them without breaking down. The system schematic and its respective state cycle for operation will be presented in the following paragraphs.

The prototype H-bridge stimulator schematic can be seen in Figure 10. As alluded to, current is simply steered through the body in a controller manner to achieve functional stimulation; there are five switches to do so. The switches are controlled by the microcontroller's digital outputs (P2.x; shorthand notation for Port 2, bit x), which are set high and low at specific time intervals dictated by which "state" the microcontroller is in. The microcontroller moves through the state cycle by "waiting" a specific number of cycles predetermined at compile time. R_1 and R_2 are 1 kΩ resistors that can be used to verify the stimulation current by measuring the voltage across them with oscilloscope probes. They detract from the voltage compliance, so when that measurement is not desired, a slide switch on the HB-PCB (not shown) can be used to short the resistors out. C_1 and C_2 are DC blocking capacitors that ensure the safety of the animal in case of a catastrophic or unplanned event. Diodes D_1 and D_2 can be seen as clamping devices, which help limit the voltage at the top of the current source by providing a path for current to flow when stimulus currents through the body are not present.

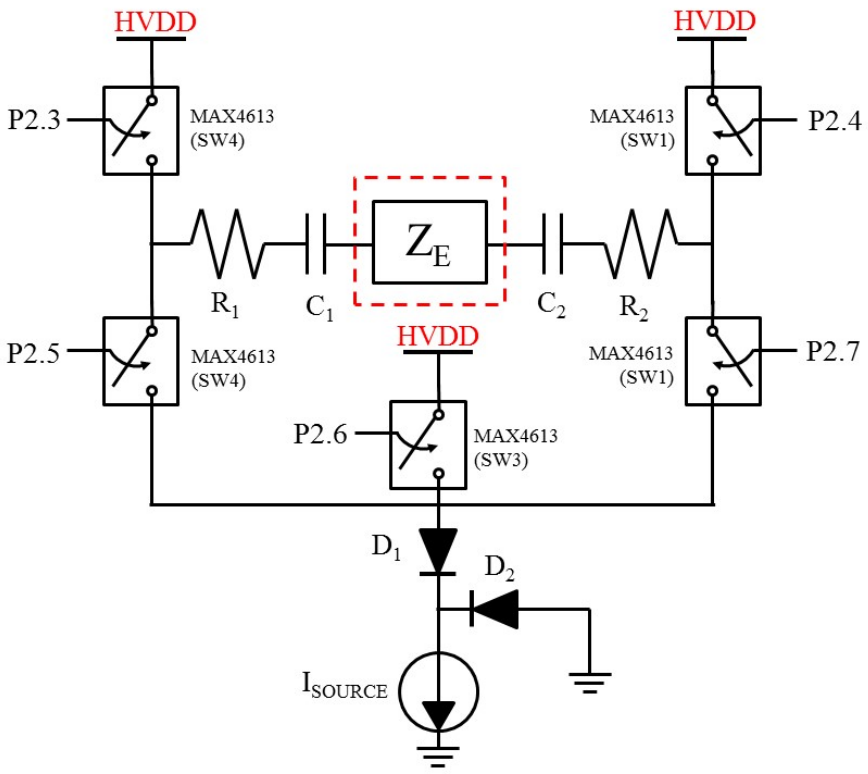


Figure 10: Prototype H-bridge stimulator schematic

The state cycle of the prototype H-bridge stimulator can be seen in Figure 11. The resistors are removed from the schematic as they aren't often used and are not integral to the operation, and the switches are drawn in a simpler manner. In State 1, the upper switches are closed to short the electrodes together to remove excess charge stored from previous stimulus pulses, and the alternate switch is closed to provide a path for current to flow and to precharge the node above the vertical diode. It is important to mention that the diodes are really just used because of the properties of the benchtop current source used. It does not have the capability of rapidly enabling/disabling current flow, so current flow must be enabled before the start of the stimulus event. If the current was enabled and there was no path for it to flow, the current source will quickly rail out (which may be in excess of ±40 V), which could cause unwanted transients when the stimulator proceeds through the state cycle.

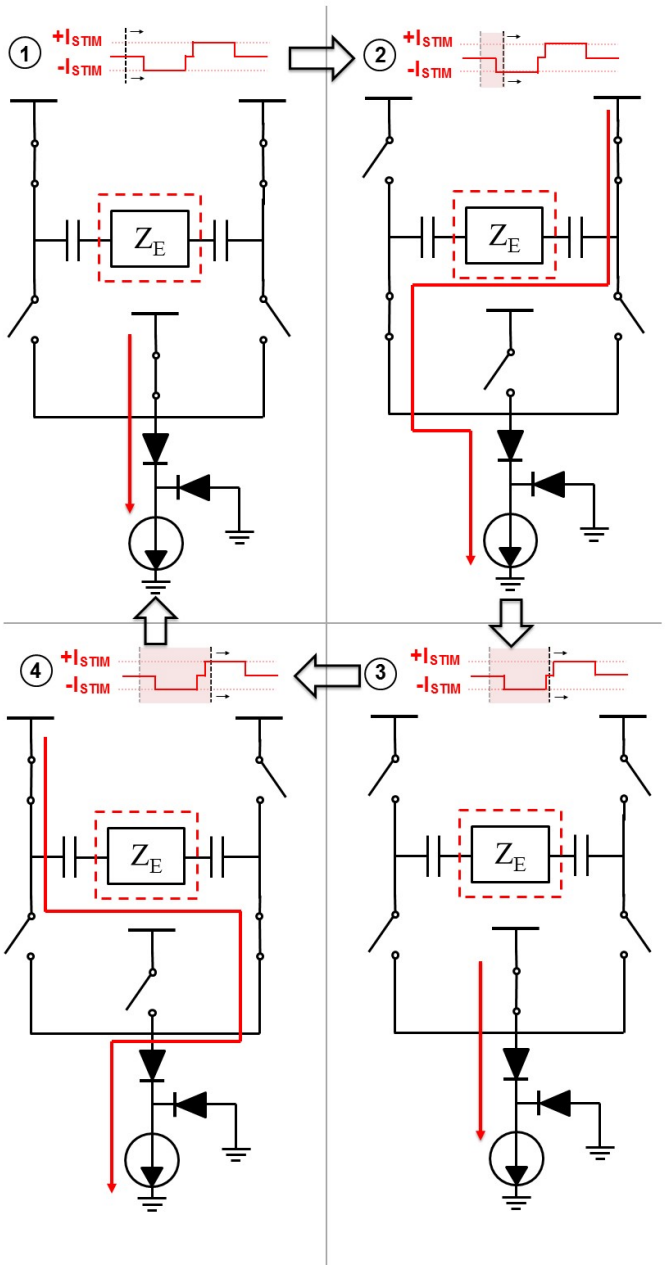


Figure 11: Prototype H-bridge stimulator state cycle (1-4)

At the onset of State 2, the cathodic current begins to flow in relation to the active electrode, which would be on the left side of Z_E in Figure 11. The DC blocking capacitors used are large, on the order of 1 µF or greater, so that the voltage built up across them during stimulation does not exceed 1 mV/µs, even during large stimulus currents on the order of mAs.

Cathodic and anodic current pulse widths are usually on the order of tens or hundreds of microseconds, so the use of the capacitors does not significantly eat into the voltage compliance of the stimulator. State 3 is a short amount of time between the cathodic and anodic current pulses that provides ample time for the action potential to be reached. In State 4, the anodic current pulse is delivered though the body. The stimulation event culminates with a return to State 1 to ensure charge is balanced if there was a net mismatch between charge delivered and absorbed.

3.4 Lab and In-Vivo Testing

Prior to performing any in-vivo testing, the prototype stimulator system was extensively tested in the lab to ensure that it was working as designed and that it could perform functional stimulation into a variety of loads; from purely resistive to purely capacitive. A picture of the MSP-EXP430G2 Launchpad with the HB-PCB can be seen in Figure 12. The HB-PCB was designed to mate directly onto the male header pins of the Launchpad, although if connection reliability is a concern, male header pins can be soldered into the HB-PCB and wires can be used to connect the two. The figure does not include the personal computer, current source, or voltage supply required for operation. Test points were specifically added to the HB-PCB to make for easy connection to oscilloscope probes. The complete schematic, board layout, bill of materials, and C code for this project can be found in the Appendix.

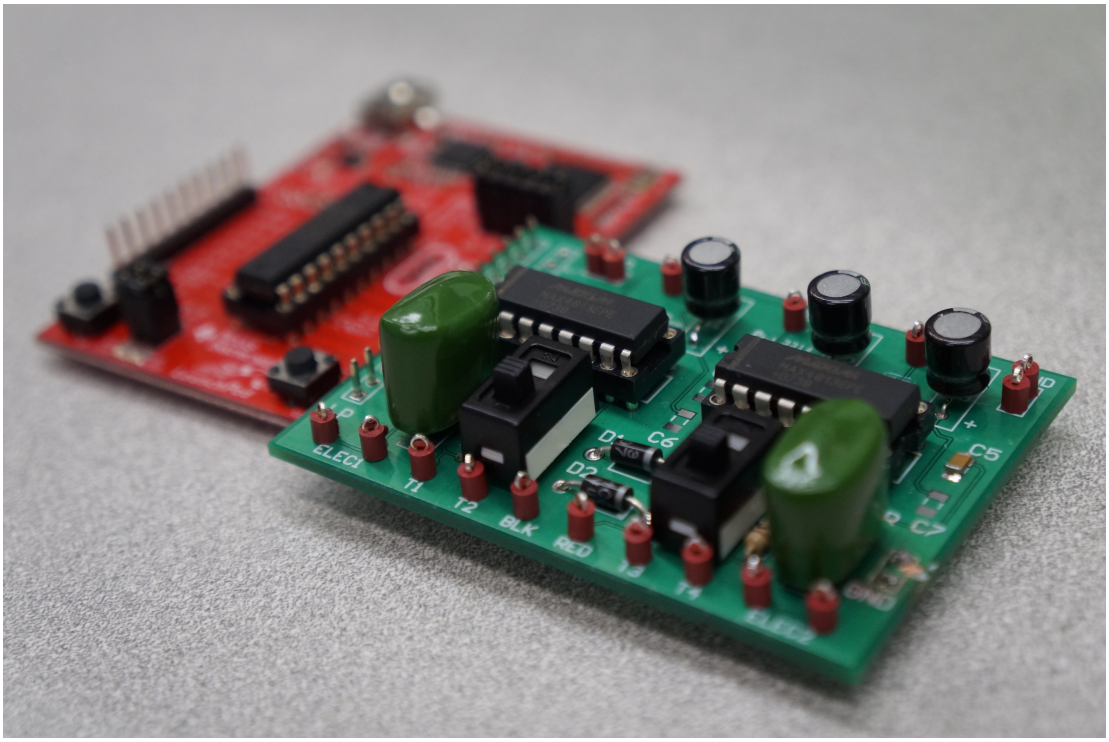


Figure 12: MSP430 Launchpad mated with the HB-PCB

Figure 13 shows the results of lab testing to verify that the prototype H-bridge stimulator system is load invariant. The first row presents the case if Z_E is purely resistive, the second if Z_E is purely capacitive, and the third row shows the case if Z_E is both resistive and capacitive. The left column highlights the voltage across the load and the right column shows the stimulus current. One can see that the stimulus current is biphasic, and how the voltage waveform changes between the different loads.

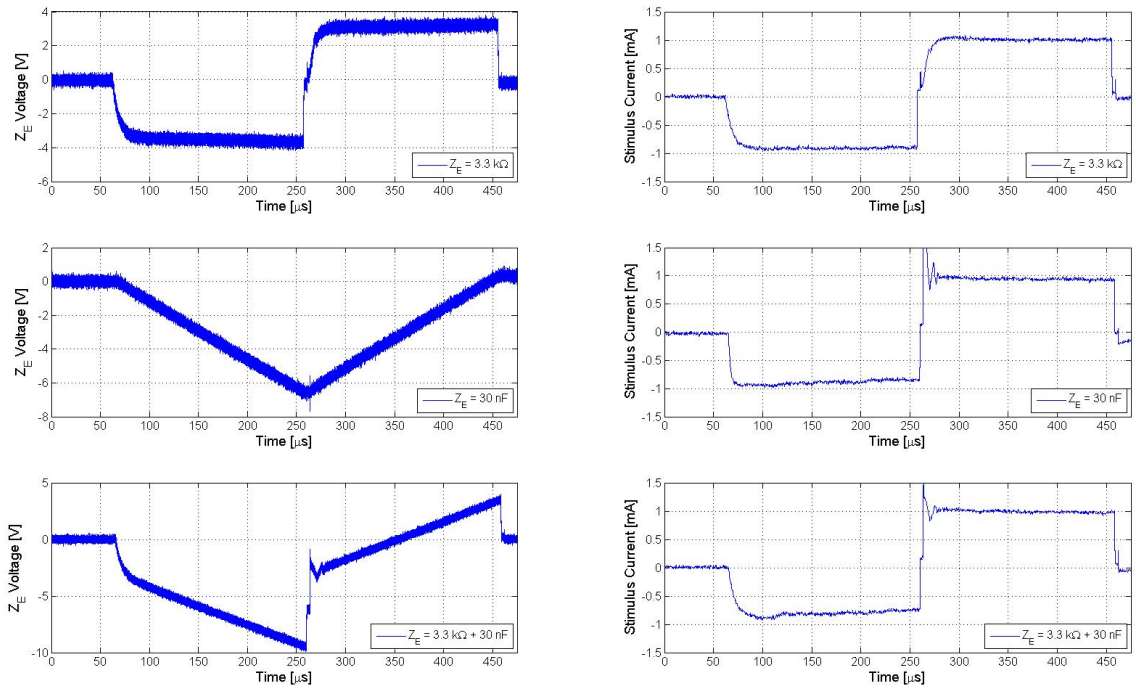


Figure 13: Prototype stimulator lab results testing different loads; voltage across load on left, stimulus current on right

Upon verification that the system was working correctly in the lab, in-vivo testing was performed on two freely moving rats with several different implanted electrode configurations. Stimulation was done on intramuscular, intraspinal, and subdural cortical tissue to test the different voltage compliances and current levels necessary to achieve functional stimulation. The subdural cortical and intraspinal electrodes had distant return electrodes, while the intramuscular electrode had a close return. The active and return electrodes were 300 µm diameter, multistranded stainless steel wires, except for the active intraspinal electrode, which was a 30 µm platinum iridium wire. The wrist-extensor was targeted, and stimulation was confirmed visually and with benchtop electromyography (EMG) recording equipment. Figure 14 provides a picture of the test and electrode setup. The stimulation parameters were configured to provide 200 µs pulse widths, three pulses at a frequency of 300 Hz, a burst frequency of 1 Hz,

and the current amplitudes were gradually increased from low levels to ensure the safety of the animal.

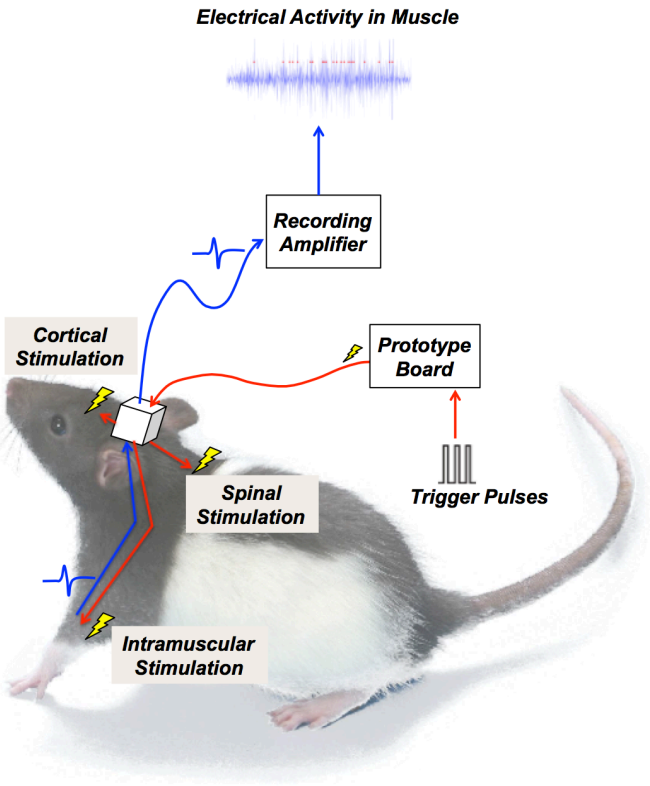


Figure 14: In-vivo test setup with electrode configurations shown

The results of the in-vivo testing were positive, with the design questions addressed and no harm done to the animal. Oscilloscope probing showed that functional stimulation could be achieved with a voltage compliance of ±11 V, and that the active and return currents were approximately equal with the use of the prototype H-bridge stimulator. The stimulation currents required to achieve stimulation gave insight to the range of currents that would be necessary for a general-purpose stimulator. The voltage across Z_E can be seen in Figure 15 for both the intramuscular and subdural cortical stimulation, as well as the active and return currents. The testing also confirmed that the electrode-tissue interface shows resistive and capacitive

properties, as other research has suggested[3,4,5], giving merit to the unique design in the state cycle of the stimulator chip.

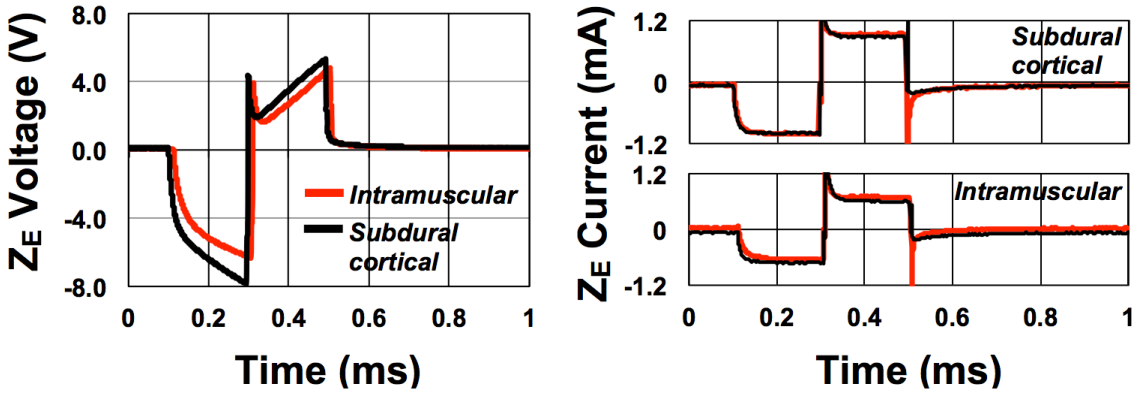


Figure 15: In-vivo test results; voltage across Z_E on the left and current waveforms on the right (1 mA for subdural cortical and 710 µA for intramuscular)

4.0 Circuit Design for the Stimulator ASIC

This chapter is meant to provide insight into the design process of the circuits created for the biphasic stimulator chip, and the various specifications and tradeoffs that were considered during the design. It is not meant to provide an in depth exploration into these circuits, which have entire books dedicated to their background, various implementations, and rigorous mathematical derivations, which are beyond the scope of this thesis. There will be cursory information given to familiarize the reader with these circuits and provide context when necessary. The circuits that I created for the stimulator chip, with more details in the following sections, were an integer-divider PLL for frequency synthesis, an eight-bit IDAC to control the stimulation current, and a clocked comparator to provide error detection feedback.

4.1.1 Frequency Synthesizer PLL Overview

The primary operation of a PLL is to synchronize the output phase of a controlled oscillator to that of a reference oscillator. A PLL can be utilized in many applications for synchronizer purposes; to modulate/demodulate data, for clock multiplication and recovery, as a coherent receiver, and more. For the biphasic stimulator chip, a PLL is used for frequency synthesis to generate the high frequency clock for the DVS blocks. The clock signal controls the movement of charge from the input to the output, or vice versa, to raise or lower the DVS voltage and provide a source path for the stimulation current. There is an industrial, scientific, and medical (ISM) radio band centered at 13.56 MHz, which will serve as the reference frequency signal. Future iterations of the stimulator chip are targeted to use this frequency for wireless power transfer, so the PLL is just taking advantage of a reference signal that will already be present. For the purposes of this chip, an active crystal oscillator IC will be used to

generate the signal, simply for testing purposes. By collaborating with the designer of the DVS, the output frequency of the synthesizer was chosen to be 108.48 MHz, or eight times the reference frequency. This value was decided upon by recognizing that the divider in the PLL could be easily implemented in powers of two, and sizing the elements of the DVS blocks to work with that clocking frequency would minimize the size of the storage capacitors and the number of stages needed for voltage multiplication. There are many performance parameters that go into the design of a PLL, including, but not limited to, the type and order of the system, the transient response, the output spectral purity, and the area and power consumption of the system. These will vary wildly depending on the application, although for this chip, the performance parameters are relatively lax compared to those of a PLL that is used to modulate narrowband data. The PLL is an inherently complex system to design, requiring extensive knowledge in several fields of engineering, and difficult to model in the time or voltage domains.

The theory and models used to design PLLs can be classified into two regions; nonlinear and linear. Nonlinear theory is complicated and difficult to deal with in real world designs. On the other hand, linear control theory is a well-established discipline of engineering that has been found to be accurate enough for PLL design, so long as certain conditions are met. A basic integrated PLL is comprised of a phase frequency detector (PFD), charge pump (CP), loop filter (LF), voltage controlled oscillator (VCO), and a divider (DIV), as seen in Fig. 16(a). The blocks of the design, through negative feedback, servo the output such that $F_{OUT} = N \times F_{REF}$. The system can be modeled in the phase domain, seen in Fig. 16(b), which assumes that the loop is already locked and is valid for small perturbations to the input phase. Although some internal signals of the PLL are digital, pulse width modulated signals, the phase domain model assumes they are continuous-time analog signals, which works well enough to ignore the introduced errors.

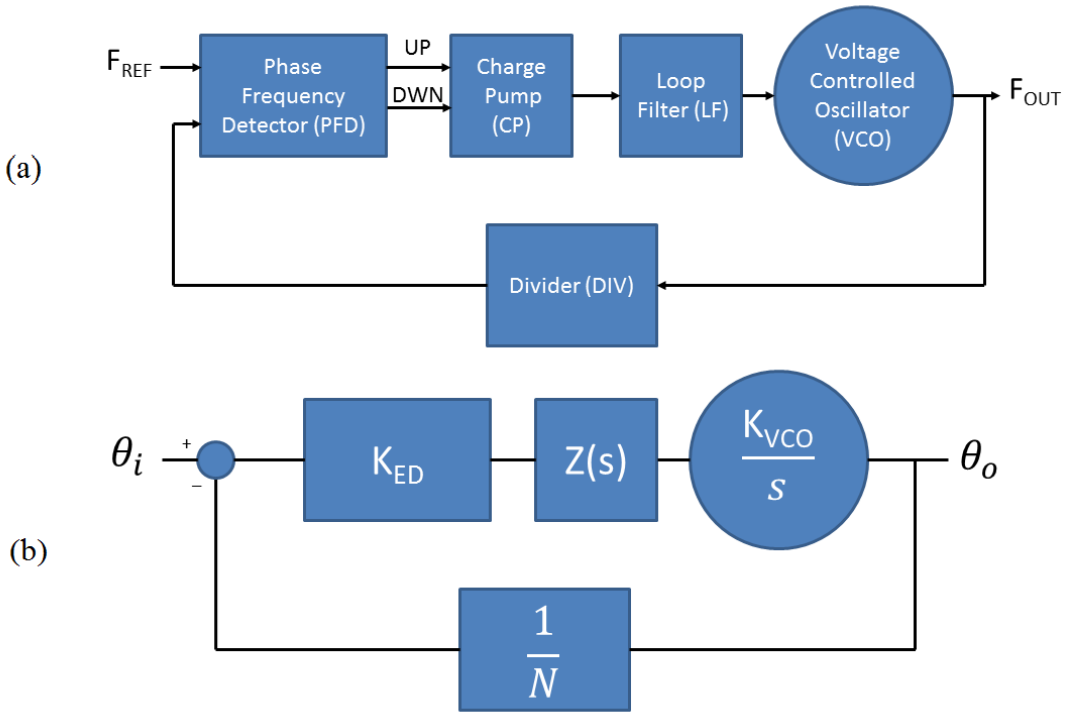


Figure 16: (a) PLL time domain model (b) Linear, time invariant phase domain model

$$G(s) \stackrel{\text{def}}{=} forward\ transfer\ function = \frac{K_{ED}K_{VCO}Z(s)}{s} \tag{4.1}$$

$$H(s) \stackrel{\text{def}}{=} feedback\ transfer\ function = \frac{1}{N} \tag{4.2}$$

$$T(s) \stackrel{\text{def}}{=} loop\ gain = G(s)H(s) = \frac{K_{ED}K_{VCO}Z(s)}{sN} \tag{4.3}$$

$$A_{CL}(s) \stackrel{\text{def}}{=} closed\ loop\ gain = \frac{\theta_o}{\theta_i} = \frac{G(s)}{1+G(s)H(s)} = \frac{K_{ED}K_{VCO}Z(s)}{s + \frac{K_{ED}K_{VCO}Z(s)}{N}} \tag{4.4}$$

The linear, time invariant phase domain model, with each block's respective gain, is shown in Fig. 16(b). Note the difference in units at the input and output between Fig. 16(a) and 16(b); the phase domain model uses Laplace transforms and analyzes the input and output in terms of phase. Frequency is the time derivative of phase, so it can be said that if the two inputs

of the PFD are phase locked, they are also locked in frequency. The PFD and CP are combined in the phase domain model to form an error detector, with a gain of K_{ED} $[A/rad]$. The loop filter converts the output current of the error detector into a voltage, so its gain is simply the impedance, denoted as *Z(s)* $[V/A]$. The gain of the VCO is K_{VCO}/s $[rad/V]$. The divide ratio determines the feedback transfer function, which is a dimensionless $1/N$. The relevant transfer functions of the control system are the loop gain, denoted as *T(s)*, and the closed loop gain, denoted as $A_{CL}(s)$, which are shown in Eqs. 4.1-4.4 with their origins. An important parameter is introduced here; the loop bandwidth w_c is the frequency at which the magnitude of the loop gain drops to unity, i.e. $|T(s)| = 1$. The loop bandwidth is an important design parameter as its value affects stability, noise, reference spurs, component values, and lock time, and may also be constrained by the PLL application.

Two other important descriptions of the PLL are its type and order. The type of the PLL refers to how many integrators are present in the loop gain transfer function, and the order is the highest polynomial in the characteristic equation of the closed loop transfer function. The type and order of the PLL affect the stability, noise, and reference spurs. A type 2, 2nd order PLL is often used as a learning tool, because it's easily stable and 2nd order control systems have been studied in depth over the past several decades. However, in practice, the 2nd order PLL has large control voltage ripples that are undesirable, making it not often implemented. A type 2, 3rd order PLL is often used to provide greater spurious suppression and reduce control voltage ripple, at the risk of introducing instability. The implementation of the loop filter is what determines the type and order of the PLL, and because of the small area cost and improved performance of a 3rd order PLL as compared to a 2nd order PLL, a type 2, 3rd order PLL is chosen as the basis for the design of the frequency synthesizer PLL for the stimulator ASIC.

4.1.2 Development of the Design Equations

This section will provide the derivations of the equations that can be used to design a type 2, 3rd order PLL. The knowledge of how the blocks internal to the PLL will be implemented at the transistor level are unnecessary at this point, as the design is still being modeled in the phase domain. Once the design equations are specified, it is easy to import them into MATLAB to take advantage of the built in Bode plotting and step response tools.

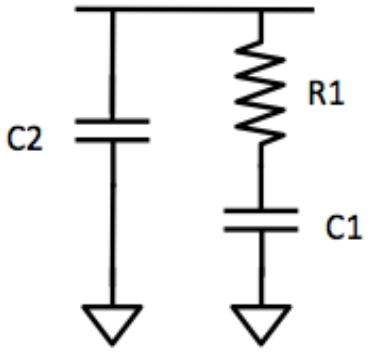


Figure 17: Passive loop filter used in a type 2, 3rd order PLL

A type 2, 3rd order PLL can be created with a passive loop filter as shown in Figure 17. The input to the loop filter is a current from the charge pump, and the output is a voltage provided to the input of the VCO, so the transfer function of the loop filter is simply its equivalent impedance. The addition of capacitor C_2 provides greater spurious rejection and reduces the control voltage ripple by adding a high frequency pole. The equivalent impedance is derived in Eq. 4.5 and put into a standard form with the pole and zero time constants defined in Eq. 4.6.

$$Z(s) = \left(R_1 + {}^{1}/_{sC_1}\right) \parallel {}^{1}/_{sC_2} = \frac{sR_1C_1+1}{s(C_1+C_2)(s\frac{R_1C_1C_2}{C_1+C_2}+1)} \tag{4.5}$$

$$Z(s) = \frac{sT_z+1}{sB(sT_p+1)} \tag{4.6}$$

$$T_z = R_1C_1 \qquad T_p = \frac{R_1C_1C_2}{C_1+C_2} \qquad B = C_1 + C_2$$

At this point, the general loop gain equation for a PLL, given in Eq. 4.3, can be explicitly defined for a type 2, 3rd order PLL, assuming the passive loop filter in Figure 17 is used. By substituting Eq. 4.6 into Eq. 4.3, important relationships can be seen between the loop filter's pole and zero time constants that relate to the stability of the PLL. The loop gain equation is shown in the s-domain in Eq. 4.7 and in Eq. 4.8 after substituting *jw* for *s* and performing some algebraic manipulation.

$$T(s) = \frac{K_{ED}K_{VCO}(sT_z+1)}{s^2BN(sT_p+1)} \tag{4.7}$$

$$T(jw) = \frac{-K_{ED}K_{VCO}T_p(jwT_z+1)}{w^2NC_2T_z(jwT_p+1)} \tag{4.8}$$

The phase margin is an important indicator of the stability of a closed loop system in its response to changes at the input. The phase margin of this type of PLL can be shown to be dependent on the relative positions of the pole and zero in the loop gain, as seen in Eq. 4.9. The phase of the loop gain at low frequencies will asymptotically approach 180° because of the two integrators in the transfer function. It will then begin to rise due to the zero, before falling because of the pole, which creates an absolute maximum. The phase margin can be maximized by setting the absolute maximum of phase to occur at the loop bandwidth frequency, which can be controlled by the positions of the pole and zero. The solution to this relationship can be seen by taking the derivative of the phase margin with respect to *w*, setting it to 0, and solving for *w,* which is shown in Eqs. 4.10 and 4.11.

$$\phi_{PM} = 180^{\circ} + tan^{-1}(wT_z) + tan^{-1}(wT_p) \tag{4.9}$$

$$\frac{d\phi_{PM}}{dw} = \frac{T_z}{1+(wT_z)^2} - \frac{T_p}{1+(wT_p)^2} \tag{4.10}$$

$$w_c = \frac{1}{\sqrt{T_p T_z}} \tag{4.11}$$

Generally, the desired loop bandwidth in an application is known, and the pole and zero time constants are variables, which must be solved. Eq. 4.11 can be rearranged to solve for the value of T_z, and the gamma parameter is added to the numerator, shown in Eq. 4.12. Gamma is a measure of whether the phase maximum is directly at the loop bandwidth, which corresponds to a gamma value of 1. A detailed discussion of gamma and the effects of varying its value can be found in [13], which is beyond the scope of this thesis. To solve for T_p, several operations must be performed. Eq. 4.12 is substituted into Eq. 4.9 and the tangent angle-difference identity must be utilized to combine like terms, before the quadratic equation is used to solve for T_p. The value for the time constant cannot be negative, so there is a single solution for T_p as a function of w_c, ϕ_{PM}, and γ, shown in Eq. 4.13.

$$T_z = \frac{\gamma}{w_c^2 T_p} \tag{4.12}$$

$$T_p = \frac{\sqrt{tan^2(\phi_{PM})(1+\gamma)^2+4\gamma} - tan(\phi_{PM})(1+\gamma)}{2w_c} \tag{4.13}$$

At this point, both the pole and zero time constants can be solved for by specifying the desired loop bandwidth, gamma, and phase margin of the system. The only thing that is left to solve for is the values of the components in the loop filter. To do so, the final remaining variable must be resolved, which is B, or the sum of the capacitances in the loop filter. This can easily be

found by taking advantage of the fact that the magnitude of the loop gain at the loop bandwidth will be unity, and that *B* is internal to the loop gain magnitude equation. So, by using the pole and zero time constants that were previously found, and a specified divider value, error detector gain, and VCO gain, *B* can be found, as shown in Eq. 4.14. To complete the design, the values for the loop filter components can be resolved as shown in Eqs. 4.15(a-c).

$$|T(jw)|_{w=w_c} = 1 \rightarrow B = \frac{C_2 T_z}{T_p} = \frac{K_{ED} K_{VCO} \sqrt{w_c^2 T_z^2 + 1}}{w_c^2 N \sqrt{w_c^2 T_p^2 + 1}} \tag{4.14}$$

$$C_2 = \frac{B T_p}{T_z} \tag{4.15a}$$

$$C_1 = B - C_2 \tag{4.15b}$$

$$R_1 = \frac{T_z}{C_1} \tag{4.15c}$$

4.1.3 Applying the Design Equations to Frequency Synthesizer

The phase domain model, with its corresponding design equations, works well when quickly prototyping a system, and makes it simple to quickly alter the starting design specifications to view the differences in results and component values, especially when built in MATLAB or another simulation program. It is an iterative process to reach an implemented design, often due to variations from the ideal model, and design constraints imposed by specific circuit techniques. The final design must be verified in simulation to ensure that it works as desired in the time domain. The design specifications presented hereafter were the final result of work done in parallel to implement the PLL subcircuits in the transistor domain. Specific circuit

techniques were chosen for the PFD, CP, VCO, etc. for a variety of reasons. The primary design optimizations were to minimize area, power consumption, and lock time, while typical PLL optimizations like jitter were ignored, simply because it is not relevant to this application. Although no quantifiable data was taken to measure the jitter, due to the low multiplier value, and the high bandwidth in combination with a highly accurate crystal for a phase reference, it should be low to moderate. For a more complete analysis of jitter, including the noise transfer functions, tradeoffs during design, and simulation techniques, see [13][14][15].

Table 1: Phase locked loop design process input and output values

User Design Specifications	Value	Component	Output Value
Reference Frequency	13.56 MHz	R_1	30.18 kΩ
Output Frequency	108.48 MHz	C_1	16.7 pF
Divider Value (N)	8	C_2	1.23 pF
Loop Bandwidth (f_c)	1 MHz		
Phase Margin (ϕ_{PM})	60°		
Gamma Parameter (γ)	0.7		
Charge Pump Current (K_{ED})	5 µA		
VCO Gain (K_{VCO})	350 MHz/V		

Table 1 shows the design specifications chosen for the frequency synthesizer PLL and the component values which come from the design equations. The loop bandwidth is chosen relatively wide to minimize the lock time, whilst still being far enough from the reference that stability should not be a concern. The charge pump current is chosen to be small so that the resulting component values are small enough to be implemented on-chip. The phase margin of the system is selected to be 60° so that stability is not a concern. Figures 18 and 19 show the open loop Bode plot and the closed loop step response of the designed PLL, using MATLAB.

The MATLAB code used for design can be found in its entirety in the appendix, accompanied by other useful plotting functions that are user selectable.

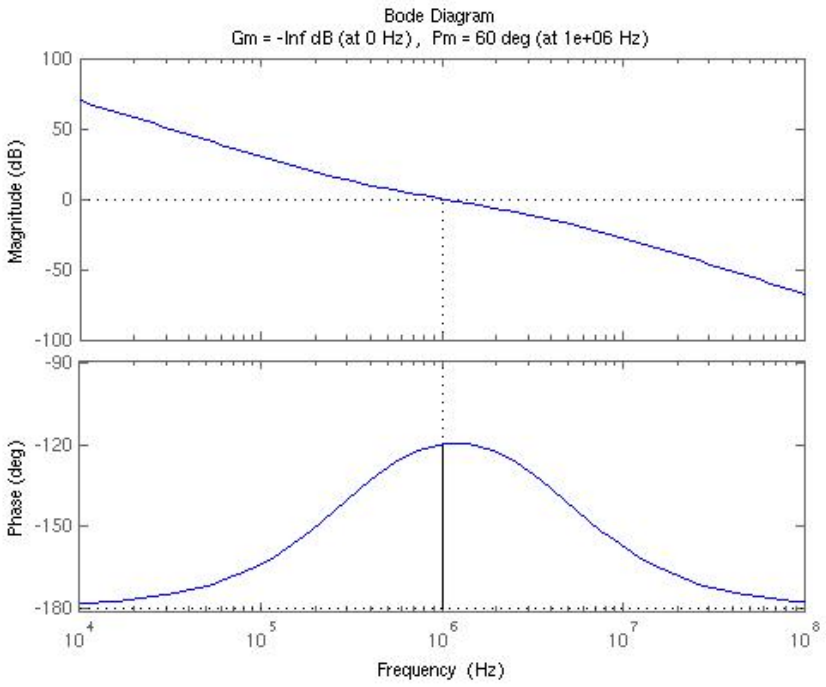


Figure 18: Loop gain bode plot of the frequency synthesizer designed in Table 1

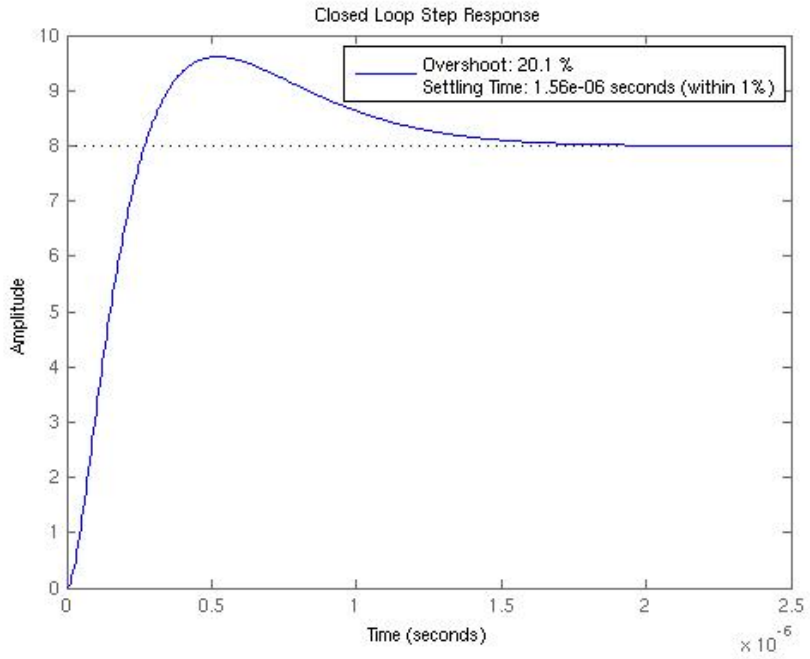


Figure 19: Closed loop step response of the frequency synthesizer designed in Table 1

4.1.4 PLL Subcircuit Design

Phase Frequency Detector (PFD)

The PFD converts the difference in phase between the reference signal and the divided output of the VCO into two, pulse width modulated error voltage signals that get passed to the CP. The output signals are typically denoted as "UP" and "DOWN", as they are used to close the "switch" that controls the flow of current into or out of the loop filter. The PFD chosen for this application, shown in Figure 20, is comprised of two D flip-flops and a handful of logic gates. The logic gates in the reset path add a short reset delay such that when the two input signals are matched in phase, short UP and DOWN pulses are still created. This ensures that there is no "dead zone" in the PLL, which causes low loop gain and increased jitter. One

advantage of this type of PFD is that it theoretically has an infinite pull-in range, which is the range of frequencies that the PFD will correctly function.

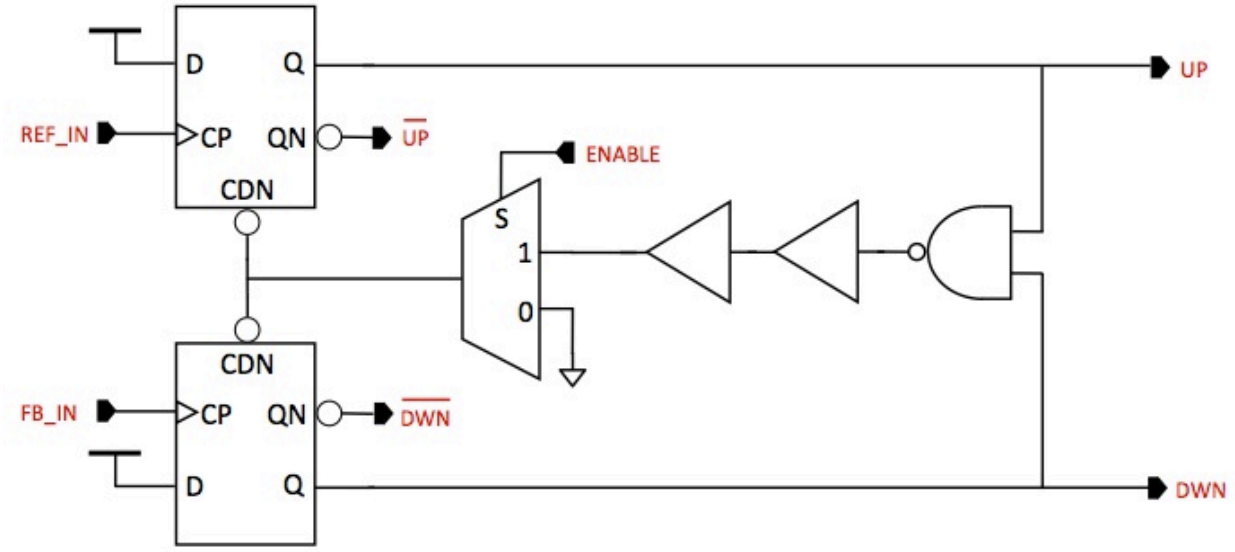


Figure 20: PFD logic gate level schematic

Charge Pump (CP)

The CP utilizes the UP and DOWN signals from the PFD to control the sourcing or sinking action of current to or from the loop filter to raise or lower the control voltage presented to the VCO. Typically, the CP presents several challenges to PLL design that affect the overall noise of the system. Clock feedthrough, charge injection, and current mismatch can contribute to phase drift and create spurious tones in the output of the PLL. However, because noise in this application is not a primary concern, these affects can be largely ignored. The charge pump used in this PLL design can be seen in Figure 21, which was leveraged from another research group at the University of Washington. It uses feedback with a rail-to-rail, folded cascode op-amp to precisely match the UP and DOWN currents of the PMOS and NMOS current mirrors, and it is based off of the design given in [16].

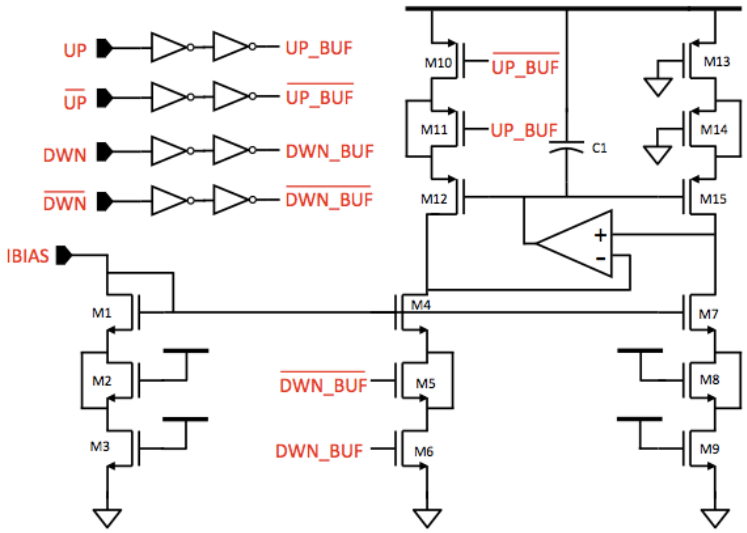


Figure 21: Source and sink current matched charge pump for PLL

Voltage Controlled Oscillator (VCO)

The choice of what type of VCO to use in a PLL is often one of the most important ones. The VCO can have dramatic effects on phase noise, area, and power consumption, and different VCOs have specific advantages and disadvantages. LC oscillators and ring oscillators are two common types of VCOs used in PLLs. LC oscillators are very costly to implement on chip due to large inductor sizes, but offer better noise characteristics than ring oscillators. On the other hand, ring oscillators are very small, easy to implement, and are generally preferred in low output frequency PLLs. The linearity and tuning range of the VCO are other important characteristics. Ring oscillators can be made relatively linear and offer a wide tuning range, which is especially important because the oscillation frequency of ring oscillators can vary dramatically due to on die variation, modeling and simulation inaccuracies, and parasitics. The benefits of ring oscillators make it advantageous to use for this PLL application.

The Barkhausen stability criterion is the condition in which a linear system with feedback will oscillate. In a negative feedback system, this occurs when the magnitude of the loop gain is

equivalent to unity, and the phase shift around the loop is zero or an integer multiple of 2π. Note that the criterion is necessary for oscillation, but not always sufficient. A single ended ring oscillator can be formed from any odd number of cascaded inverters greater than one. A NAND gate can be substituted for a single inverter with one input used as an ENABLE signal. A ring oscillator will oscillate with a period given by $2Nt_d$, where N is the number of inverting stages, and t_d is the time delay of each stage between the input and output changing polarity. It is difficult to estimate the oscillation frequency of a ring oscillator, as MOSFETs are complex, nonlinear devices, and the system itself is also nonlinear, so it is best left to simulation. Controlling the oscillation frequency of a ring oscillator is easily done by "starving" it of current, by putting biased header and footer transistors to limit the charging and discharging current of each inverting stage, which can be seen in the schematic of the VCO presented in Figure 22. The VCO employs binary inputs to potentially shift the VCO transfer curve up and down in the case that the desired oscillation frequency cannot be reached due to deviations from simulated effects, and the control voltage input transistor is degenerated with a resistor to decrease the gain of the VCO to match that of specification provided in the phase domain model.

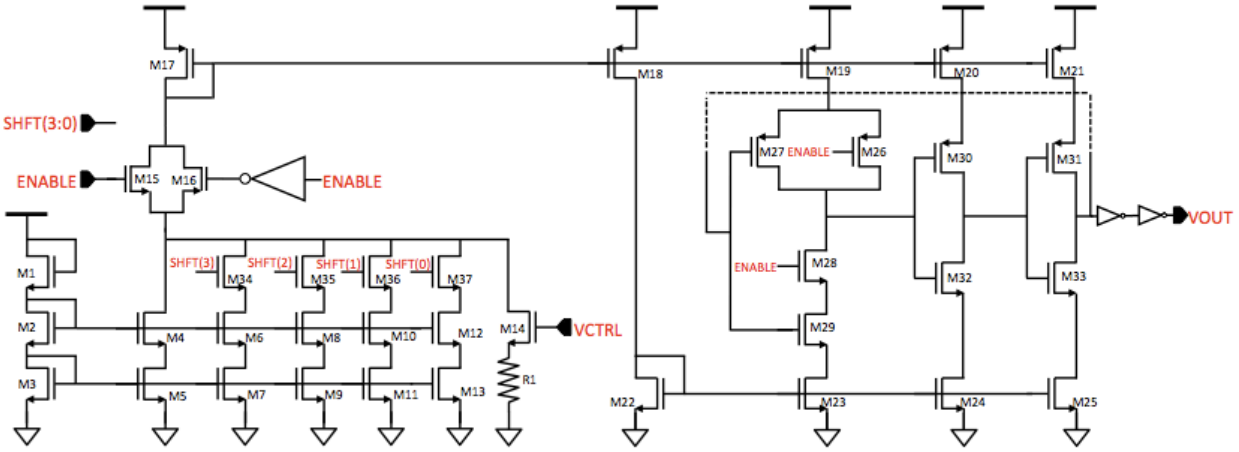


Figure 22: Voltage controlled oscillator employed in the PLL

Divider

The PLL was designed to minimize area costs and design time as much as possible, so before the design had begun, it was decided that the two DVSs would be clocked by a system clock of approximately 108 MHz, which means that the PLL requires a simple divide-by-eight circuit. This divider ratio is trivial to implement at such low frequencies, and is done so with three cascaded D flip-flops, as seen in Figure 22. The divide-by-four and divide-by-two outputs are also used in other points of the system.

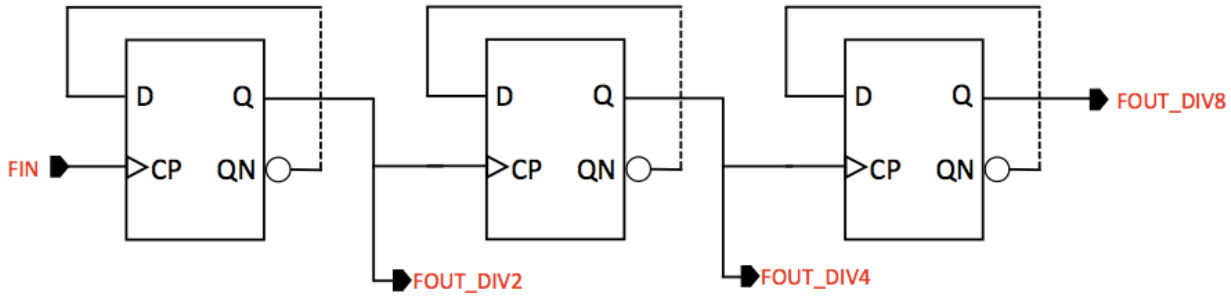


Figure 23: Divide-by-eight circuit for PLL

4.2.1 Stimulator Current DAC Overview

The desired specifications of the on-chip IDAC that is used to generate the currents that activate nervous tissue present unique design challenges that must be addressed; namely the current range, output impedance, and output voltage. The H-bridge stimulator ASIC was designed to function as a general purpose stimulator that is capable of being employed in one of the many medical applications that require an implantable stimulator, which may require widely varying levels of stimulation current. This is in contrast to other stimulator chips, which are often designed for a single application, such that they are only required to generate a small range of currents and can be optimized to do so. The output impedance of the IDAC must be large

enough to accurately maintain a square stimulation current pulse as the stimulation cycle progresses and the drain-source voltages of the current mirror transistors vary. The H-bridge stimulator ASIC is fabricated in a 65 nm process, which inherently degrades the output impedance of the transistors, especially at high currents. The final challenge is the minimization of the required output voltage of the IDAC for it to function as a current source, as any increase in the minimum output voltage directly lowers the voltage compliance of the stimulator.

4.2.2 Design of the H-Bridge Stimulator's Current DAC

The IDAC operates by mirroring a reference current such that the output current is N times greater than the reference. The magnitude of the output current is controlled by eight digital inputs, which provides access to 256 programmable levels of output current. The reference current, which is also the LSB value for the IDAC, was chosen as 10 μA to deliver a reasonable amount of granularity for stimulation applications that require lower current magnitudes. The maximum deliverable stimulation current is 2.56 mA, which is large enough to satisfy most stimulation applications that require high currents. The supporting circuitry of the H-bridge stimulator was designed to operate best with stimulation currents between 50 μA and 2 mA, so in reality the system has 196 programmable levels of output current, even though the IDAC itself can operate beyond those constraints.

The basics of current mirroring and an explanation of the advantages and disadvantages of a multitude of topologies will not be included in this thesis. It is assumed that the reader is familiar with this topic. There are many books on the subject, and the interested reader can find detailed discussions in [17][18][19], for example.

As transistor feature sizes have decreased as new processing technology has been created, the output resistance of a MOSFET in the saturation region has significantly decreased. A single transistor current mirror is no longer sufficient to function as a nearly ideal current source, so other topologies must be used. Cascoding is often employed to improve the output resistance of a current mirror, at the expense of an increased minimum output voltage. The desired output resistance of the IDAC was chosen to be greater than or equal to 1 MΩ and the minimum output voltage limited to $2V_{DS,sat}$, or approximately 250 mV.

The current mirror topology shown in Figure 24 was selected to be used in the IDAC, as the op amp in the feedback path, with it's output at the gate of the cascoded transistor, increases the output resistance considerably. It also requires a relatively small minimum output voltage of $2V_{DS,sat}$, as desired in the specifications. The op amp does require a DC voltage to set the drain voltages of the transistors that are connected at their gates through the feedback path, but provides an added feature of being able to directly control the drain-source voltage such that the transistors are right at the edge of saturation, which minimizes the required output voltage.

The circuit schematic and its corresponding small signal model can be seen in Figure 25(a),(b) for a single output current path. The transistor used as a switch is included to better model the complete schematic. The transistor switch is deep in the triode region, so it's small signal model is simply a resistor. The small signal equations for the output resistance, R_{OUT}, can be seen in Eqs. 4.16-4.19. The output resistance for the IDAC circuit topology is found to be approximately A times larger than that of a cascoded current mirror without the op amp in the feedback path, which is a significant improvement.

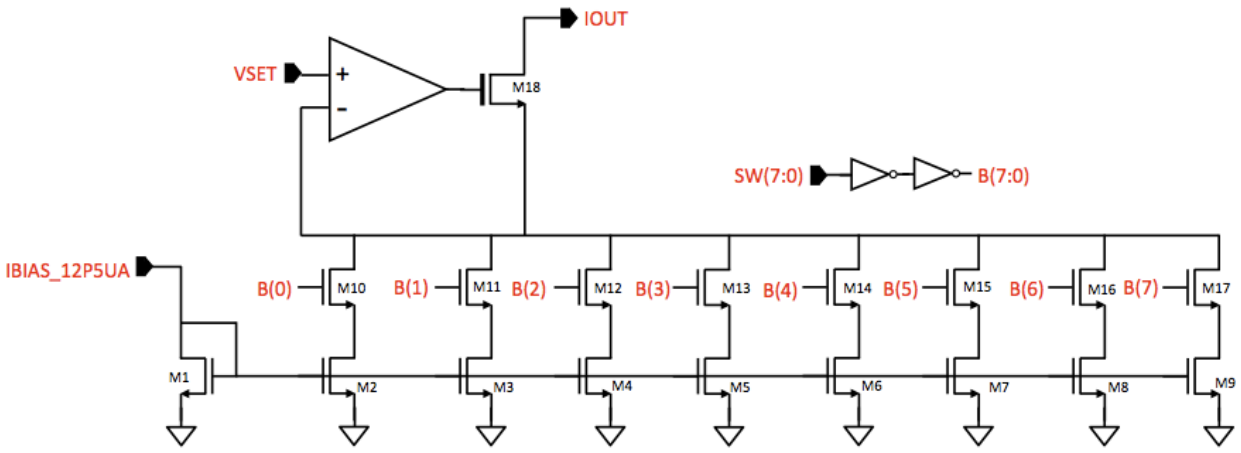


Figure 24: Eight-bit IDAC Top Level Schematic

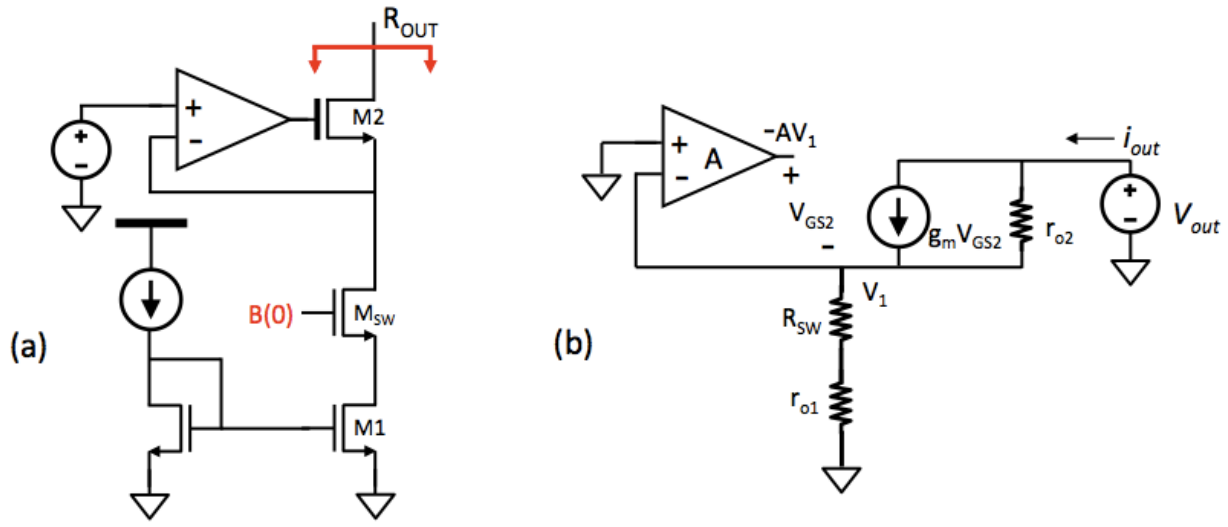


Figure 25: (a) Schematic used for small signal model (b) Small signal model about the bias point

$$V_{GS2} = -AV_1 - V_1 = -V_1(A+1) \tag{4.16}$$

$$V_1 = i_{out}(R_{SW} + r_{o1}) \cong i_{out} r_{o1} \tag{4.17}$$

$$V_{out} = (i_{out} - g_m V_{GS2}) r_{o2} + V_1 \tag{4.18a}$$

$$= (i_{out} + g_m V_1(A+1)) r_{o2} + V_1 \tag{4.18b}$$

$$= (i_{out} + g_m i_{out} r_{o1}(A+1)) r_{o2} + i_{out} r_{o1} \quad (4.18c)$$

$$R_{OUT} = \frac{V_{out}}{i_{out}} = r_{o2} + g_m r_{o1} r_{o2}(A+1) + r_{o1} \quad (4.19a)$$

$$\cong g_m r_{o1} r_{o2} A \quad (4.19b)$$

4.2.3 Current DAC Subcircuit Design

The circuit topology selected for the IDAC requires an operational amplifier for the feedback path, ideally one with a large open loop gain, which directly affects the output resistance of the IDAC. Bandwidth of the op amp is not a large concern, due to the fact that the inputs are not connected to any high frequency AC signals, and the rise time of the voltage at the IDAC output is relatively slow due to the time it takes the DVS the ramp up its output voltage. The primary design constraints for the op amp are that it has a large open loop gain, is very stable, and consumes a minimal amount of current and layout area.

A folded cascode op amp is chosen as the topology to be employed for the feedback path op amp. The output of the op amp is connected to a large capacitive load due to the sizable cascode transistor required to pass the high currents of the IDAC, so a two-stage op amp is not a good design choice. Stability concerns would arise due to the low frequency pole created by the capacitive load, and the low frequency pole typically created when pole splitting is used for compensation. A folded cascode op amp can achieve high gains in just a single stage whilst also maintaining a satisfactory phase margin. The output swing of the op amp can be made to nearly reach the positive rail, which is relevant due to the high gate overdrives required to sink large currents through the cascode transistor. In addition to the features above, a folded cascode op

amp also has a large common mode input range, possibly even reaching below the negative power supply rail.

The schematic for the folded cascode op amp can be seen in Figure 26; the bias circuitry is omitted for brevity. The small signal voltage gain will be found by inspection. If a small voltage is applied at the differential inputs, and it is assumed that the impedance seen looking into the drain of M5 is equivalent to that of the impedance looking into the source of M7, which is a fair assumption (see pp. 318 and pp 222. of [19]), then the small signal current flowing into the output resistance, R_{OUT}, will be approximately $0.75g_{m2,3}$. The output resistance will be the parallel combination of the impedance looking into the drains of M7 and M9, which can be simplified to involve a constant *x* between 0 and 1 that is dependent on the NMOS and PMOS transconductances and conductances [pp. 318, 19]. The equations describing these terms, along with the small signal gain, are summarized in Eqs. 4.20-4.22. The input common mode range (ICMR) is defined in Eq. 4.23, the output swing in Eq. 4.24, and the dominant pole is the reciprocal of the output resistance times the load capacitance. There are five non-dominant poles in the op amp, which can be found by inspection by taking the reciprocal product of the small signal resistance from that node to ground times the sum of the capacitances connected to that node [pp. 224, 19]. Since dominant pole compensation is used for the folded cascode op amp, the others will not be listed here, although they can be found on pp. 320 of [19].

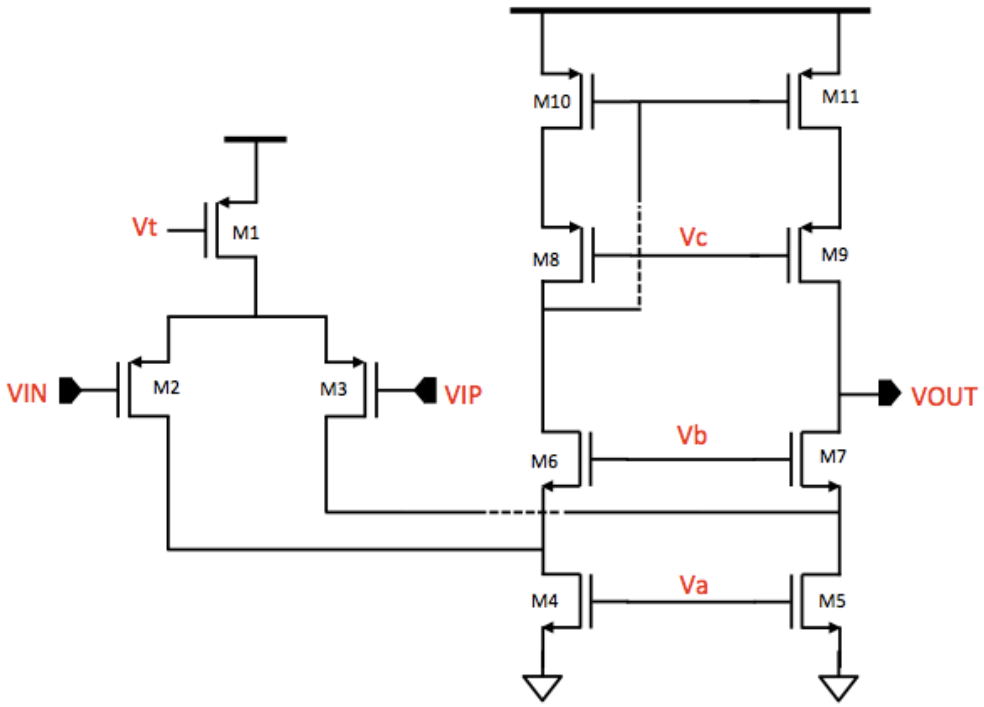


Figure 26: PMOS input, wide swing current mirror load, folded cascode op amp

$$G_m \cong 0.75 g_{m2,3} \tag{4.20}$$

$$R_{OUT} \cong (g_{m9} r_{o9} r_{o11}) \parallel (g_{m7} r_{o7} (r_{o5} \parallel r_{o2})) \tag{4.21a}$$

$$\cong x(g_m r_o^2) \qquad 0 < x < 1 \tag{4.21b}$$

$$A_v = G_m R_{OUT} = 0.75 x (g_m r_o)^2 \tag{4.22}$$

$$V_{CM} < V_{DD} - |V_{DS,SAT1}| - |V_{DS,SAT2,3}| - |V_{th2,3}| \tag{4.23a}$$

$$V_{CM} > V_{DS,SAT4,5} - |V_{th2,3}| \tag{4.23b}$$

$$V_{O,SWING} < V_{DD} - |V_{DS,SAT11}| - |V_{DS,SAT9}| \tag{4.24a}$$

$$V_{O,SWING} > V_{DS,SAT5} + V_{DS,SAT7} \tag{4.24b}$$

4.3.1 Error Detector Comparator

The H-bridge stimulator ASIC requires feedback as it progresses through the state cycle to signal when to transition from one state to the next and also to signal when the dynamic supply voltage that the DVS provides must be increased to keep the IDAC in saturation. The high side diode that is used in the H-bridge as a "switch" must also have some error signal to provide control such that when each PCD is in TRACK mode, no current flows through the diode. A comparator is employed for each of these applications to generate a one-bit error signal that is passed to the control logic of each PCD. The comparator should be high speed, have a small offset, and, ideally, draw no current when not actively making a decision.

The comparator at the output of the IDAC, with one input held at a V_{SET}, determines whether the IDAC is moving out of the saturation region. The error signal that it generates is used in two places in the state cycle. Firstly, the error signal is used to tell the DVS that its output voltage must be increased when either PCD is in SUPPLY mode, both in the cathodic and anodic stimulation phases. Secondly, it is used as a means to provide information so as when to transition from the state where the tissue-electrode capacitance is supplying the stimulation current, and when the balancing PCD must supply stimulation current for the anodic phase of stimulation.

The comparator used to ensure the diode doesn't conduct current when the PCD is in TRACK mode has its inputs connected to each side of the diode through a capacitive divider, to ensure that the input transistors' breakdown voltage is not exceeded. The error signal that it generates signals to the PCD that it must decrease the output voltage of the DVS so that it is approximately equal to that of the electrode voltage. The comparator used here must be able to

operate with input voltages all the way down to 0 V, and the offset voltage of the comparator is critical. Any offset voltages will be multiplied upwards to the diode by the capacitive divider's division ratio, *N*. If the division ratio was large (if the comparator's input voltage range was small), and the offset was large, the diode could potentially be conducting when it should not be, and the cathodic and anodic stimulation currents would not be equal. To simplify the design complexity, the same comparator was used in both places for the system.

A comparator can be characterized by its gain, speed, area, power consumption, input offset voltage, and other specifications. The large number of variables can make designing a comparator very difficult, and often one must select the most important constraints of the design before proceeding. The most important comparator in the H-bridge stimulator is the one whose inputs are taken at the capacitive dividers of the diode. The entire stimulation system could fail if it is not designed properly. The summary of an initial analysis of its application is to follow. It must operate correctly across the entire range of the DVS output voltages, from 0-12 V. It's input offset voltage must be small, under 10 mV as a design constraint. Its power consumption must be minimized as much as possible. If clocked, it must have zero clock feedthrough or charge injection to the inputs, so as not to corrupt the input signals. It must respond to changes at the inputs quickly, meaning its bandwidth must be maximized. As in any analog block, several of these specifications are inversely proportional, meaning there is not an ideal solution.

The high performance comparator required for this application leads towards the implementation of a comparator that uses a low gain preamplifier stage followed by a clocked, positive feedback latch. The inputs to the comparator are voltages taken at the top plates of capacitors in the capacitive divider, which do not get reset between comparison cycles. The voltages must be left completely undisturbed to preserve the integrity of the signals, so kickback

noise and charge injection cannot be withstood. A fully dynamic clocked comparator can thus not be used, due to its kickback noise. "Autozeroing", a process that is often successfully used to reduce comparator offsets down to less than 1 mV, can also not be used due to the charge injection and clock feedthrough that comes along with it. A low gain preamplifier boosts the voltage difference present at the inputs of the comparator to enable the positive feedback latch to operate faster, divides the high input offset of the latch by a factor of its gain, and protects the inputs from kickback noise. A flip flop is used at the output of the comparator to save the output state of the comparator, and a short delay is used to satisfy its hold time requirements.

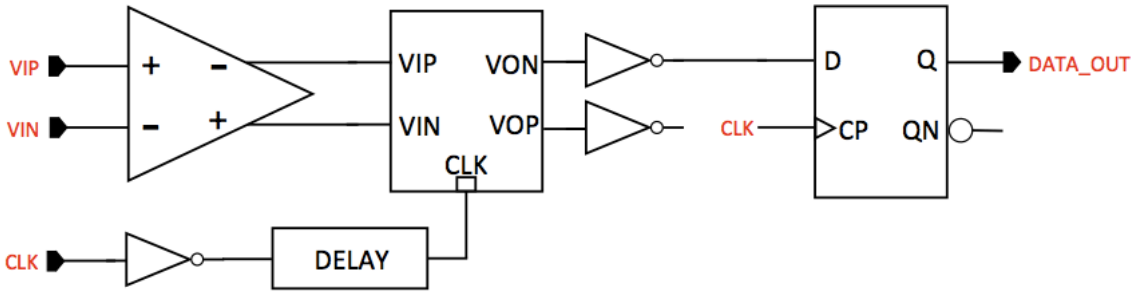


Figure 27: Top level comparator schematic

4.3.2 Comparator Subcircuit Design

Low Gain Preamplifier

The preamplifier of the comparator functions to protect the comparator inputs from kickback noise, reduce the offset contribution of the positive feedback latch, and present a greater voltage difference to the latch to avoid metastability and decrease latching time. As previously stated, the comparator must function across the entire range of the divided down voltages of the DVS. This means a PMOS differential pair must be used, and careful design must be done to ensure that the input common mode range extends down to 0 V. A low to

moderate gain, high bandwidth amplifier is preferred for this stage to maximize the speed of the comparator.

The preamplifier shown in Figure 28 is chosen for the comparator for several reasons. The PMOS devices in the schematic are 2.5 V tolerant devices to allow for a greater input common mode range so that the capacitive divider ratio can be decreased, which increases the tolerable offset of the comparator. The input transistors are also made large to increase their transconductor efficiency by having them operate in the weak inversion region and also improve their matching characteristics. The output nodes of the differential amplifier are low impedance nodes because they are connected to diode connected load transistors, which makes common mode feedback unnecessary, simplifying the design. The cross coupled load transistors present a negative differential impedance looking into their drains, canceling the positive impedance seen looking into the drain of the diode connected transistors, which allows the preamplifier to achieve higher gains. The load transistors are sized carefully so as not to introduce overwhelming positive feedback into the preamplifier that would cause the outputs to latch. It is recommended that M6/M7 are sized smaller than M4/M5 such that the transconductance of M6/M7 is no more than approximately 0.75 times that of M4/M5 [20]. In this design, $g_{m6,7}$ was measured to be 0.81 times that of $g_{m4,5}$. The voltage gain of the preamplifier is summarized in Eq. 4.25, and the input common mode range in Eq. 4.26.

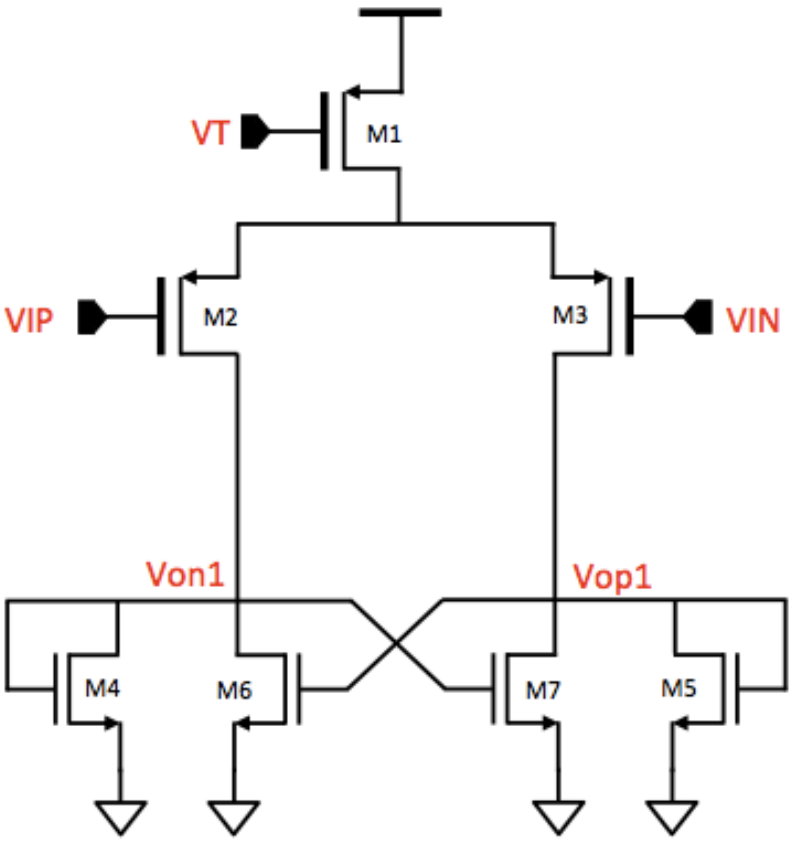


Figure 28: Comparator preamplifier schematic

$$A_v \cong \frac{g_{m2,3}}{g_{m4,5}-g_{m6,7}} \tag{4.25}$$

$$V_{CM} < V_{DD} - |V_{DS,SAT1}| - |V_{DS,SAT2,3}| - |V_{t2,3}| \tag{4.26a}$$

$$V_{CM} > V_{GS5,6} - |V_{t2,3}| \tag{4.26b}$$

Positive Feedback Latch

The second stage of the comparator operates by taking the amplified difference from the preamplifier and employs positive feedback to greatly decrease the time it takes to resolve the outputs to the power supply rails. The latch is clocked to reduce its average power consumption

and erase any potential memory effects that the comparator might have. To erase any memory of the comparator, every node in the latch must be reset to a known potential. The latching stage of the comparator also aids in protecting rapid voltage changes at the comparator outputs from propagating through to the comparator inputs through the parasitic capacitances.

The positive feedback latch topology is derived from DRAM sense amplifier designs, which share a lot of the same specifications. The circuit shown in Figure 29 is taken from [18]. As discussed, all nodes of the circuit must be reset to a known potential, which occurs in this topology when clock is low. When clock is low, M14/M15 pull the outputs up to V_{DD}, which connects the gates of M10/M11 to V_{DD} as well, discharging their drains through the input transistors M8/M9. Although, at the beginning of the decision period, M8/M9 operate in the triode region, good sensitivity can still be achieved because of the large voltage dropped across the gate-source of transistors M10/M11 and the drain-source of the input transistors [pp. 452, 18]. A requirement of this circuit is that at least one of the input transistors must have a gate voltage greater than V_{th}. If neither input transistor has a gate voltage greater than V_{th}, neither transistor conducts the necessary current to ground to resolve the outputs to their full logic levels. The kickback noise of the latch is reduced because the inputs of it are shielded from the rapid changes at the output by transistors M10 and M11.

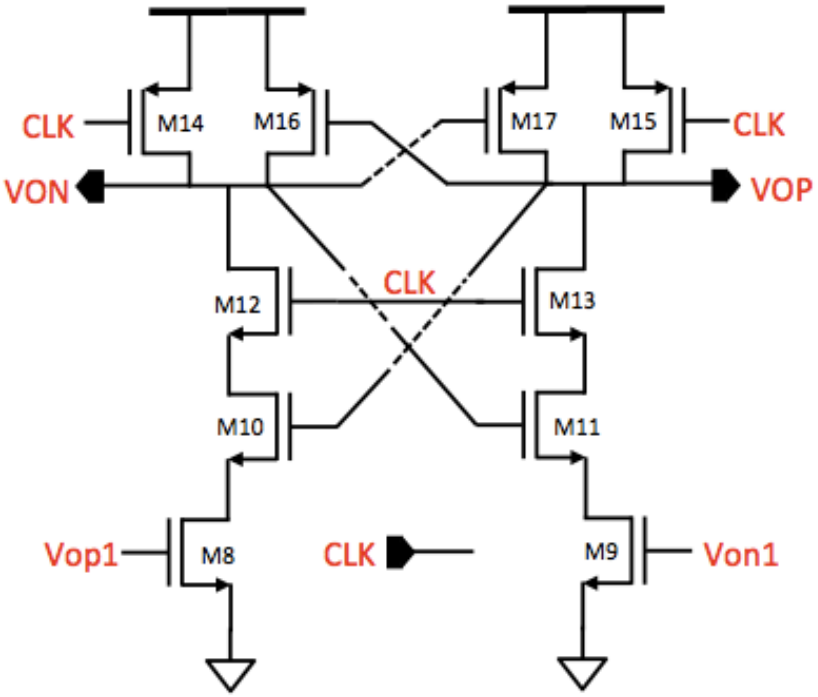


Figure 29: Positive feedback latch schematic

5.0 Post Layout Simulation Results

This chapter takes the circuits and systems designed in the previous chapter, and verifies their desired operation with post layout simulation results. These simulations vary depending on the circuit being tested; the simulation may be a transient test, DC operating point, AC analysis, Monte Carlo analysis, or a combination of many. The completed layouts, which all passed DRC and LVS analyses, will also be included in this chapter, along with their corresponding dimensions. Specific layout techniques may be discussed when matching is concerned. To summarize, this chapter is written as a substitute for the measured results, as the ASIC has not yet been received and tested at the time of this thesis's writing.

5.1.1 Top Level Frequency Synthesizer PLL

A top level block diagram of the completed PLL can be seen in Figure 30. In addition to the subcircuits described in the previous chapter, several additional transistors have been added to the top level system. These transistors act as switches and provide a way to bypass the PLL completely, to ensure that the system can still operate in the case that the PLL does not operate correctly. Both the PFD and VCO have enable inputs so that the PLL can be put in a low power mode when the frequency synthesizer output clocks are not being used. As previously discussed, stimulated tissue typically is given a rest period directly after a stimulation cycle, so it is desirable to turn off all circuits when possible, to minimize wasted power. The layout of the PLL can be in seen in Figure 31, with the total area being approximately 40,000 μm^2, or 0.04 mm^2. The layout is primarily dominated by the loop filter's capacitors and the compensation and noise filtering capacitors used in the charge pump. The layout area of the PFD, VCO, and divider are trivial relative to the loop filter and CP.

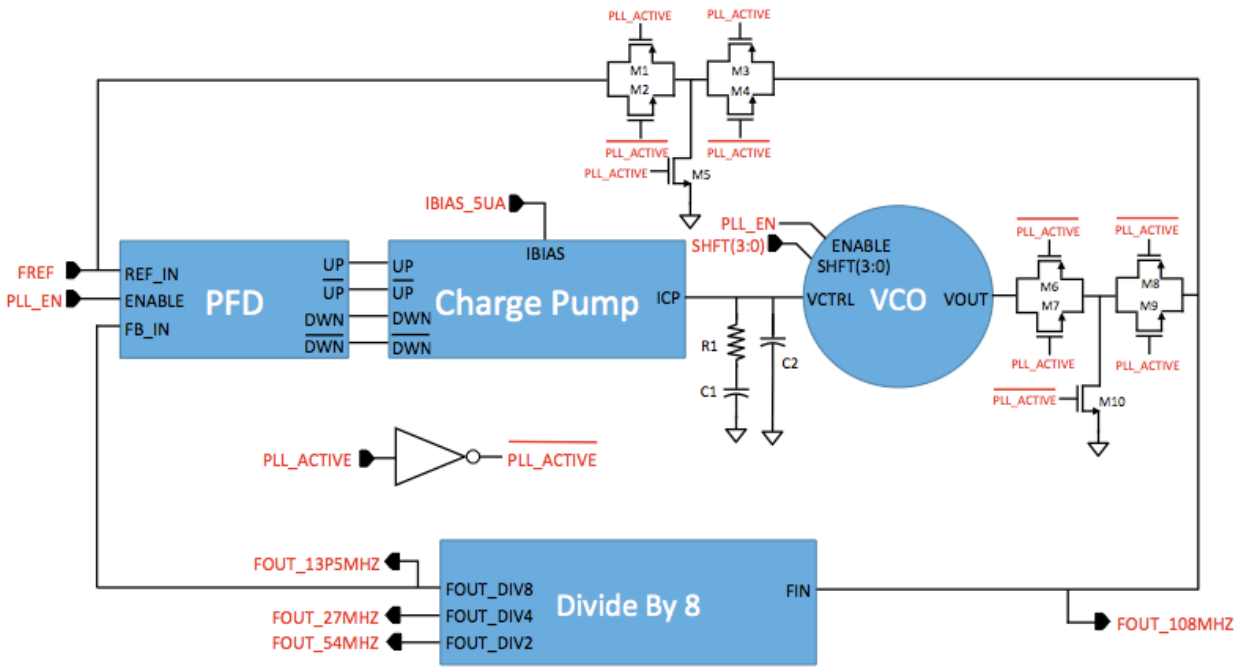


Figure 30: Top level PLL block diagram

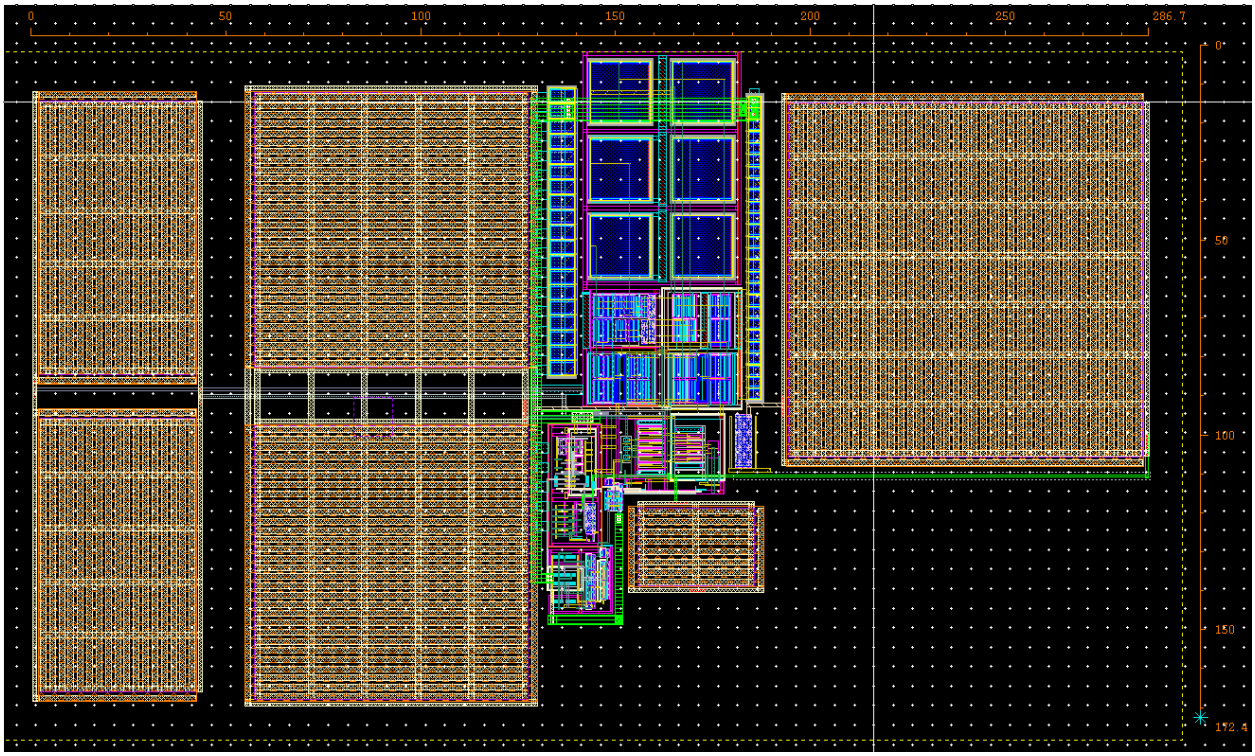


Figure 31: Top level PLL layout

The transient step response of the PLL can be used as a good indicator to determine if the implemented system matches the designed one, and can also be used to verify that the system is stable. Large step response overshoot or excessive ringing can indicate that the system is on the edge of stability. The control voltage is plotted in the time domain when the input signal is stepped in Figure 32. Although the control voltage does not vary smoothly due to the discrete nature of the PLL, the plot closely resembles that of the one shown in Figure 19. If one imagines that Figure 32 had a moving average filter applied to the control voltage to remove the spikes, the overshoot would be approximately 20% and the settling time would be about 1.75 μs, which is in agreement with Figure 19.

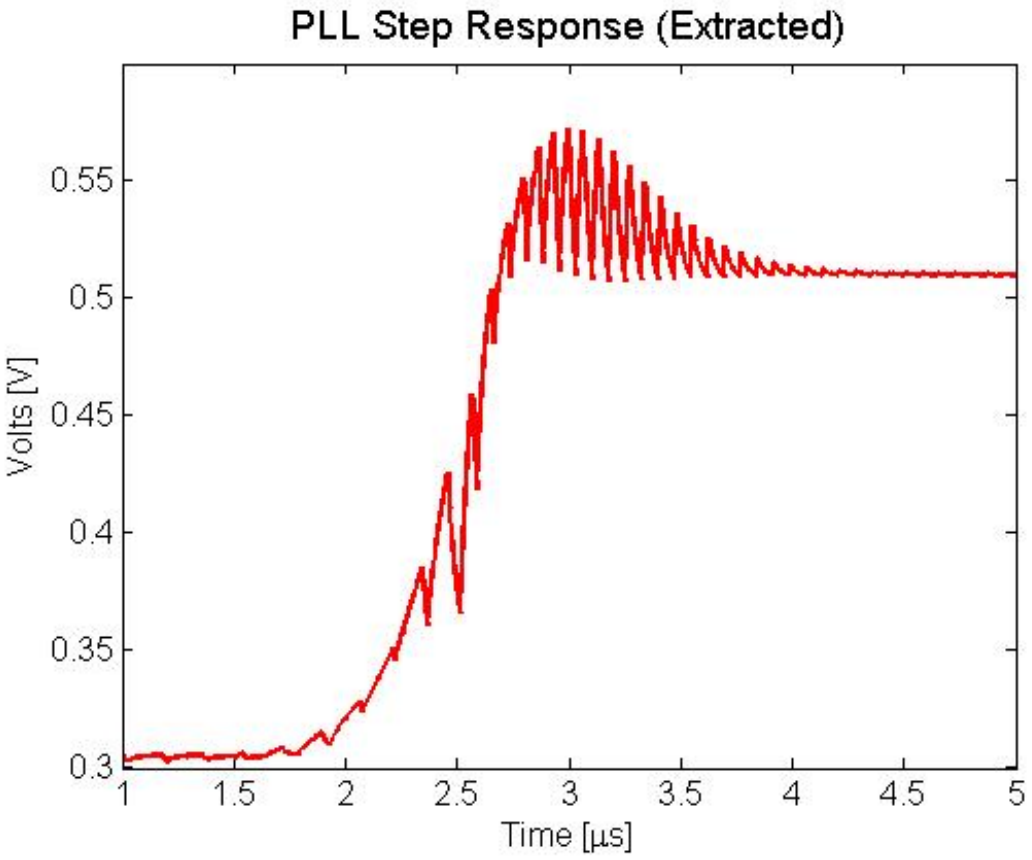


Figure 32: Extracted step response of the PLL

5.1.2 PLL Subcircuit Simulations

Phase Frequency Detector (PFD)

The finite amount of gate delay in the PFD and the non-zero turn on time of the CP due to the gate capacitance of the switches mean that very small phase errors cannot be recognized, which leads to a flattening of the error detector's phase-gain transfer curve that induces undesirable effects. Additional logic gates are added in the reset path of the PFD that helps eliminate it's dead zone by generating short UP and DOWN pulses when small phase errors are present. The identical UP and DOWN pulses of approximately 200 ps seen in Figure 33 occur when both the reference and feedback signals are shorted together.

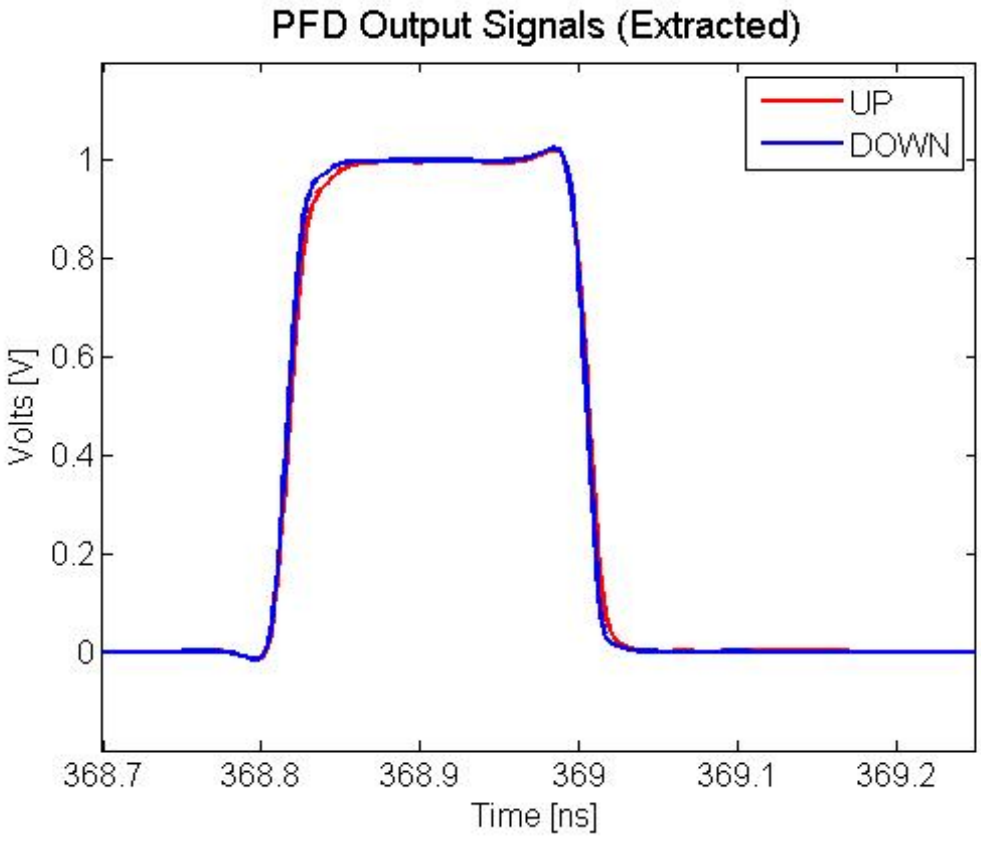


Figure 33: PFD simulation showing the zero phase error control pulses

Charge Pump (CP)

The current matching of the CP is an important characteristic in a frequency synthesizer application. It is an important attribute as it can contribute to static phase error and increased reference spurs, among other things. Current matching and its effects on both of those qualifications is considered in [16]. The finite output resistance of the PMOS and NMOS current source transistors in a CP contribute to a current magnitude difference between sinking and sourcing due to the drain current's dependence on V_{DS}. The CP used in this design uses feedback to minimize the current mismatch across the entire range of possible output control voltages. A plot of the CP output current when the output voltage is held fixed at the potential that causes the VCO to oscillate at the desired frequency and an UP and a DOWN pulse is applied to the CP can be seen in Figure 34. It can be seen that the sinking and sourcing current is nearly identical.

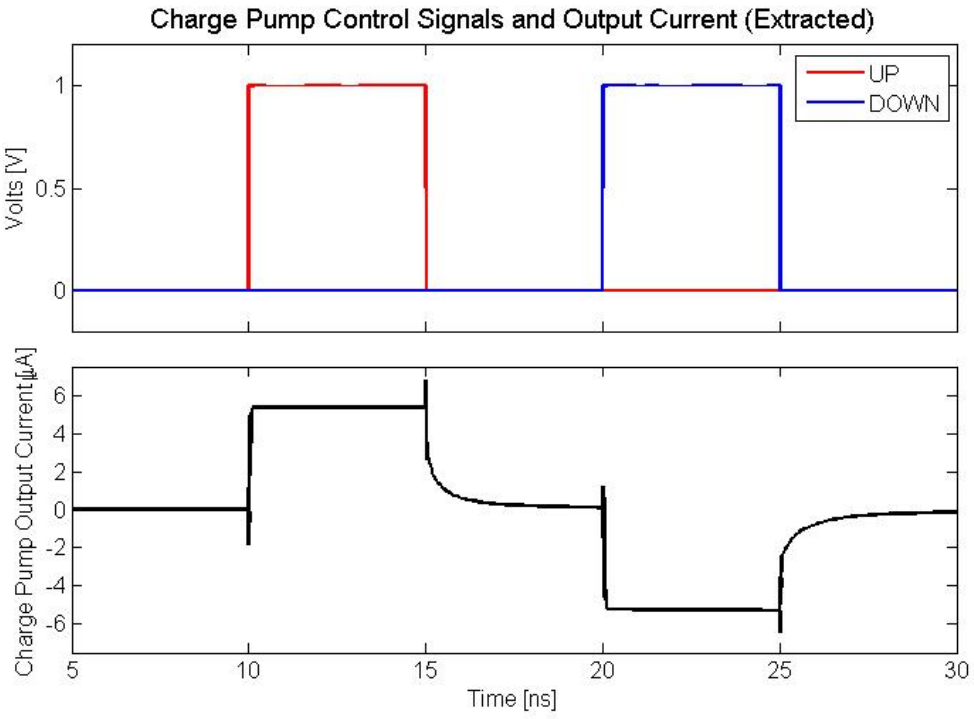


Figure 34: Charge pump current matching simulation with set output voltage

Voltage Controlled Oscillator (VCO)

The oscillation frequency of the VCO for the entire range of possible control voltages can be seen in Figure 35. The phase domain model assumes a perfectly linear transfer curve for each PLL subcircuit, which is generally only true when considering a small deviation from the locked, steady state condition of the PLL. However, the VCO's transfer curve is linear over a control voltage range from approximately 0.15 V to 0.75 V. The gain of the VCO in that linear range is nearly 340 MHz/V, which almost perfectly matches the initial assumption of 350 MHz/V when the PLL was designed. The four control bits to the VCO also provide a methodology to shift the gain curve up or down 30 MHz without affecting the gain, in the case that the VCO does not oscillate as predicted from simulation.

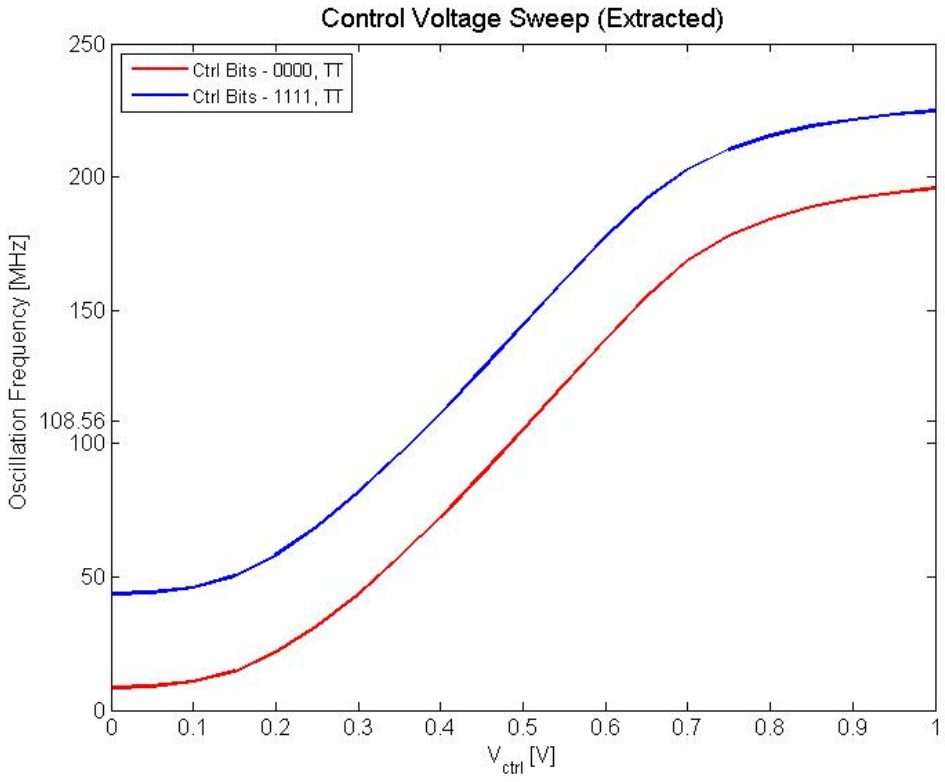


Figure 35: VCO frequency linearity simulation over the range of control bits

5.2.1 Top Level Current DAC

The IDAC for the H-bridge stimulator ASIC achieved the initial desired specifications, and its layout can be seen in Figure 36. The total width and the height of the layout are approximately 120 µm and 95 µm, respectively, giving a total area of 11,400 μm^2, or 0.0114 mm^2. The large current mirror transistors were divided into multiples of unit-sized transistors of 5/1 µm and all of the transistors were arranged in a common centroid manner so as to provide better matching characteristics. The minimum output voltage and the output impedance were the important specifications of the block, and the results for these can be seen in Figure 37. The figure shows the maximum current for the system, 2 mA, as the minimum output voltage will be the largest, and the output impedance the lowest, at this level of current. The minimum output voltage is approximately 200 mV, and the output impedance is on the order of 1 MΩ at 475 mV.

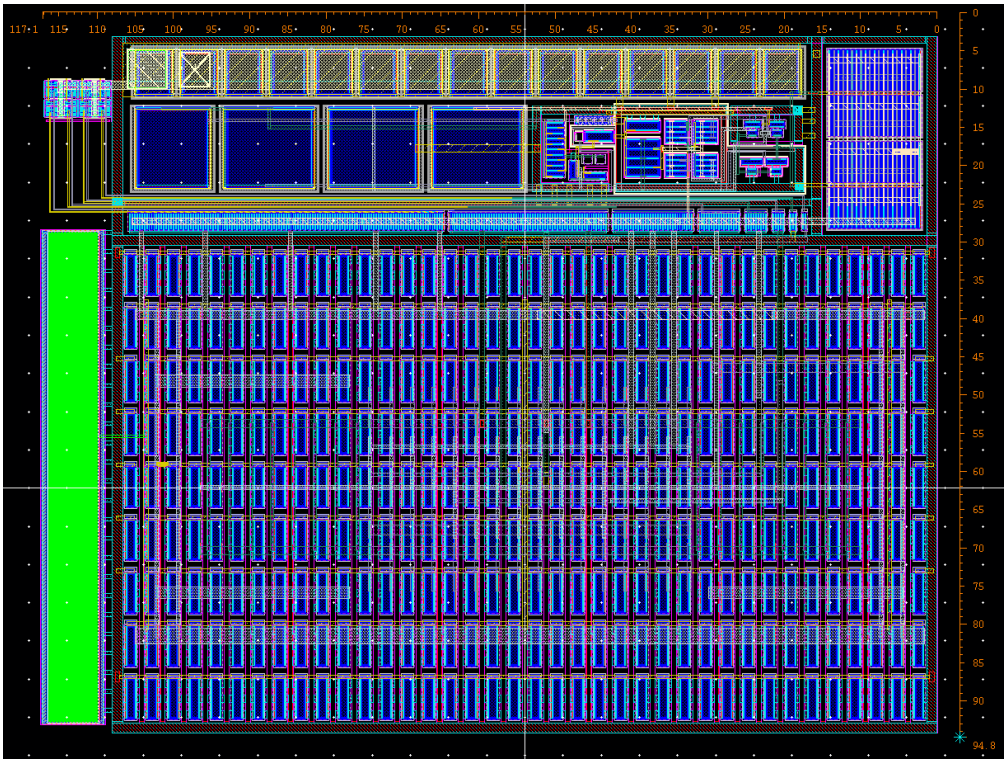


Figure 36: Eight-bit IDAC top level layout

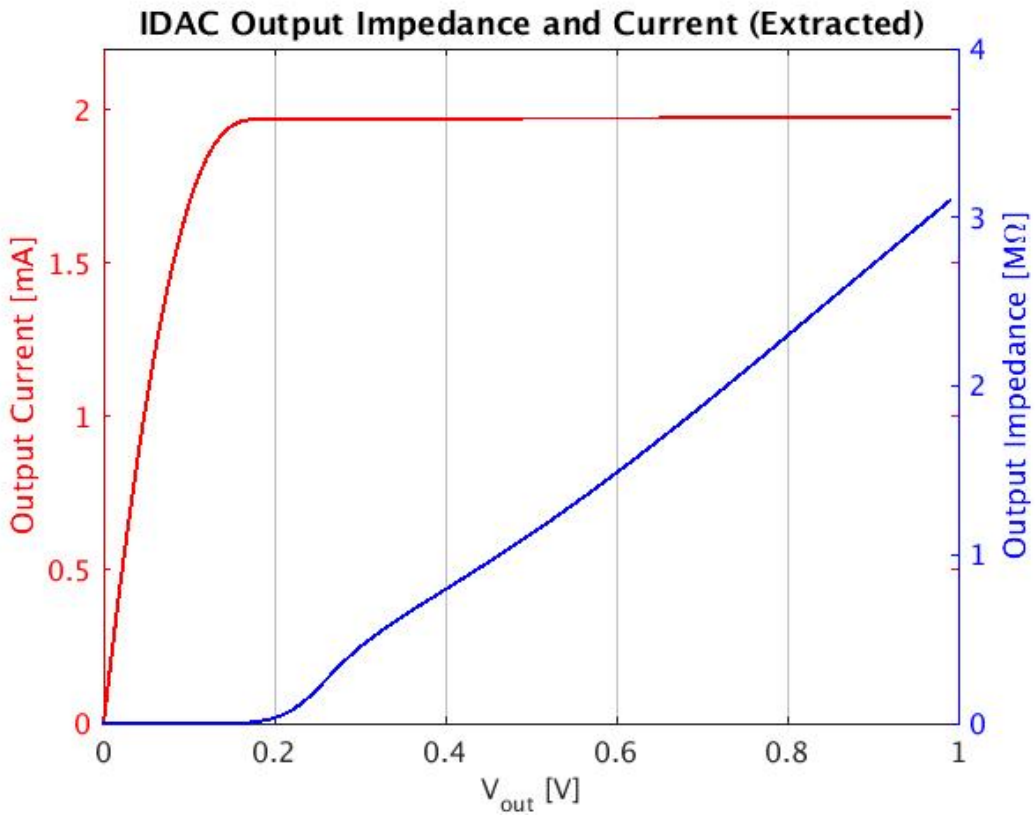


Figure 37: Maximum IDAC current magnitude and output impedance

5.2.2 Current DAC Subcircuit Simulations

As discussed in the previous chapter, the primary design goals for the folded cascode op amp used as the feedback amplifier in the IDAC are for it to have a large DC gain and be sufficiently stable. By taking advantage of Virtuoso's built in simulation tools, the loop gain is simulated of the folded cascode op amp and its feedback path whilst inside the IDAC. This allows for accurate representation of the op amp's characteristics by providing the exact load that it will see, and removes any guesswork that could occur when checking the design results. The open loop gain of the op amp is approximately 1000 V/V, or 60 dB, while the loop gain is approximately 57 dB due to the small signal gain through what is essentially an emitter follower

being slightly less than 1. The phase margin is approximately 75° at a unity gain bandwidth of 30 MHz, which means this system is very stable.

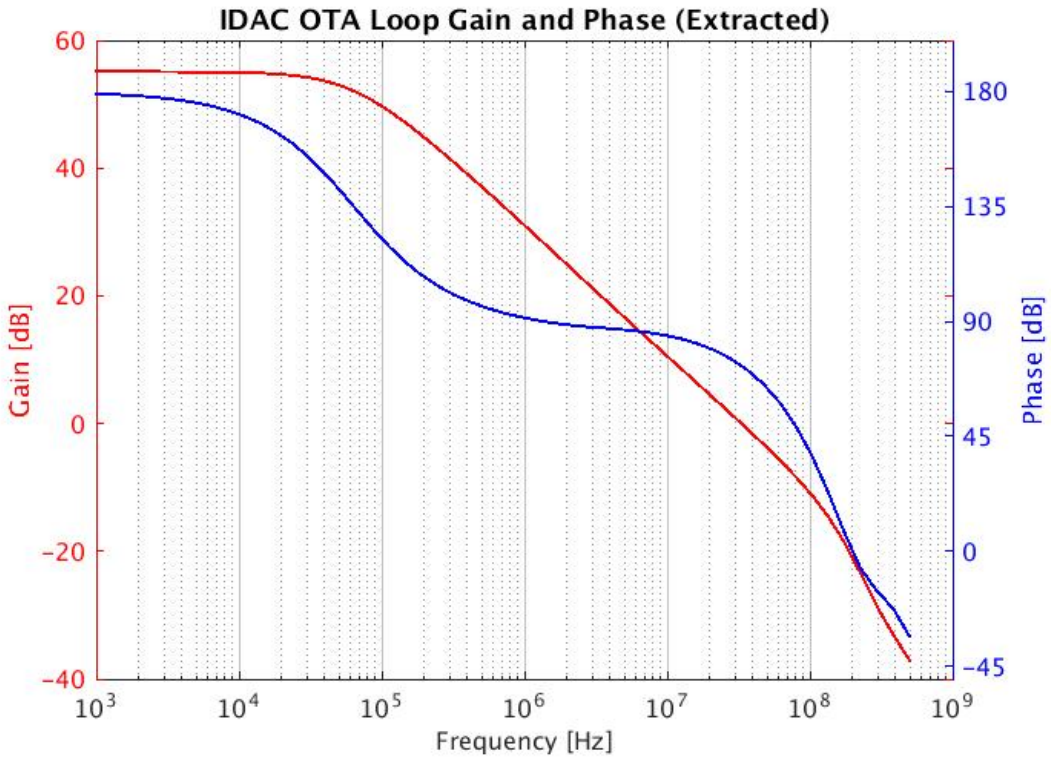


Figure 38: IDAC op amp loop gain and phase

5.3.1 Top Level Error Comparator

The continuous time preamplifier and clocked, positive feedback latch that make up the error comparator met the desired specifications set forth in the design phase. The 2.5 V input devices allowed for a large input common mode range to be had, which eased the specifications of input offset voltage. At the sacrifice of speed, the transistors were made large to minimize transistor mismatch effects. As described later, the bandwidth of the preamplifier was not sacrificed to an excessive level. Also, the choice of a two-stage topology allowed for protection from kickback noise and mitigated the latch's contribution to the input offset voltage. The top

level layout of the comparator, including its bias circuit, can be seen in Figure 39. Common centroid layout techniques are used in both the preamplifier and latch to minimize transistor mismatch, which affects the input offset voltage. Dummy transistors are also used in the preamplifier. The total layout area is approximately 1,100 μm^2. At a potential difference of 1 mV at the inputs of the comparator, extracted simulations showed that the outputs were resolved in approximately 500 ps. The comparator is clocked at 108 MHz, so the time to resolve the outputs is about 11% of time allotted to the decision phase. A Monte Carlo analysis was repeatedly performed to measure the input offset voltage, following the techniques described in [21], which showed a standard deviation of roughly 3.5 mV with N =500.

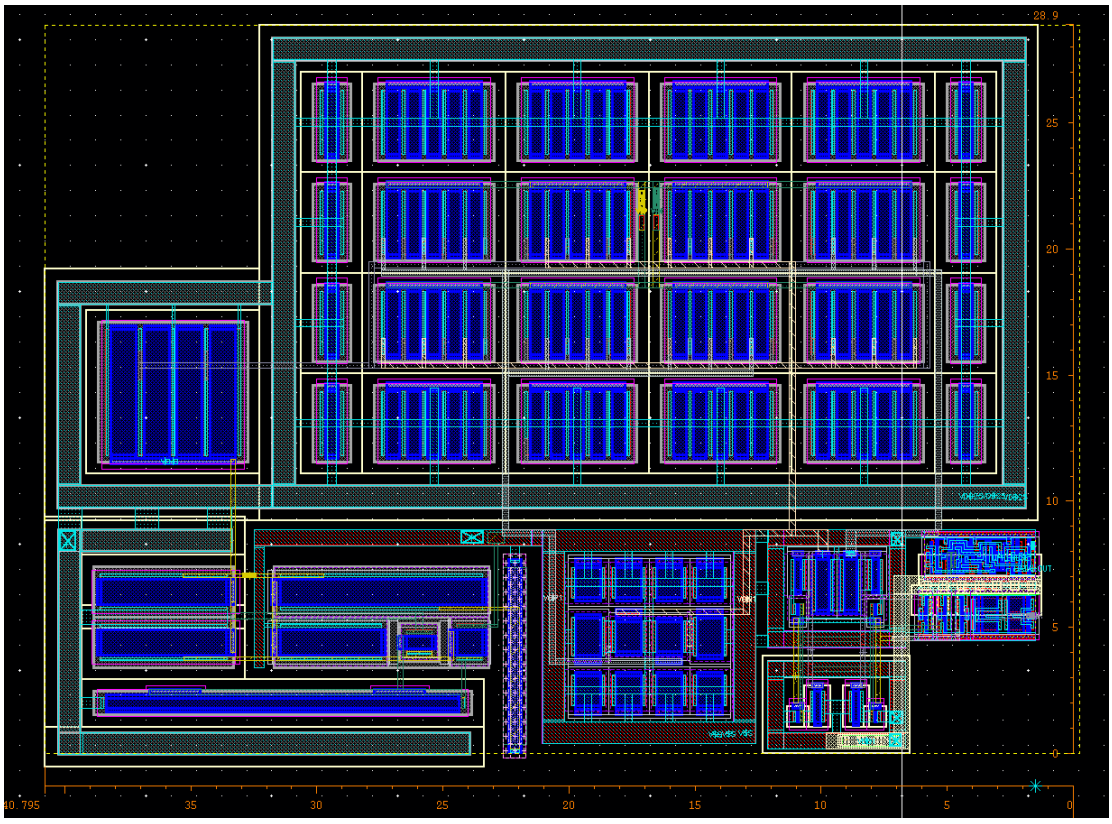


Figure 39: Top level comparator layout, including bias circuit

5.3.2 Comparator Subcircuit Simulations

Preamplifier

The preamplifier of the comparator, as the first stage, must be carefully designed. The bandwidth of the preamplifier must be maximized to get high speed, which directly works against the goal of getting high gain to negate the effects of the latch's offset voltage. This is the reason that preamplifiers often have low to moderate gains, and if larger gains must be achieved, then the preamplifiers are cascaded. A Bode plot of the magnitude of the gain and phase is shown in Figure 40. The gain is approximately 21 dB and the unity gain frequency is at 275 MHz. The moderate gain divides the latch's offset, which can be on the order of tens of millivolts, by a factor of 11, greatly reducing it. The preamplifier time constant is the reciprocal of the -3 dB frequency (in rad/s), or about 6.3 ns. The dynamic comparator is clocked at 108 MHz, for a time constant of roughly 9.25 ns. Thus, after just two clock cycles, the preamplifier output will have settled to within 95% of its final value.

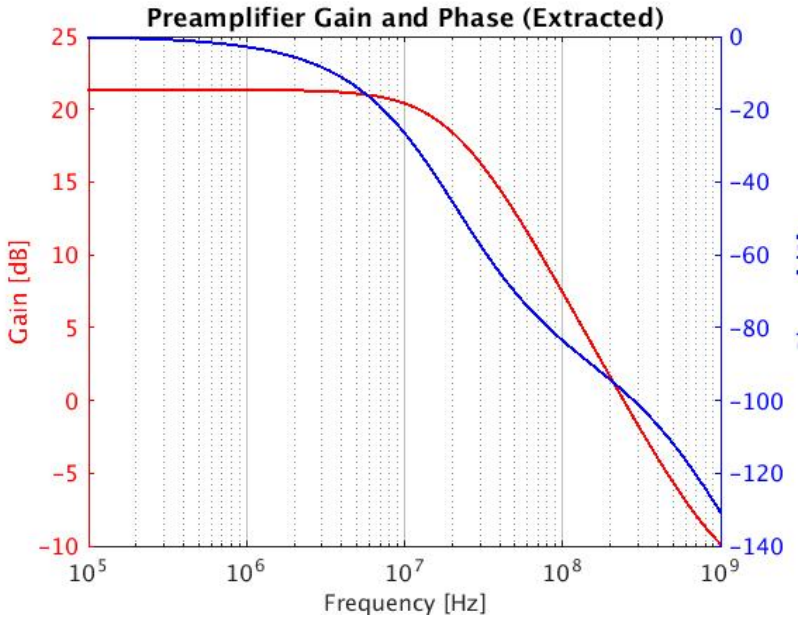


Figure 40: Preamplifier gain and phase plot

6.0 Conclusion

As the years have progressed from the creation of the first transistor, custom analog chips and processors have found their way into increasingly more applications. It is only logical that we have begun to blend engineering with human anatomy. It is an exciting time to be in chip design, and we have the possibility to create devices that don't just entertain us, but aid us in a completely different way. However, much work must still be done to realize the goal of creating widespread, safe, long or short term implantable circuits that do things like treat a mental disorder, stimulate tissue to activate regrowth, or reanimate disabled or non-functioning limbs.

In this thesis, I have presented an introduction to the science behind stimulation, and the mechanisms by which it works. I've also cited relevant papers and projects that align with the same goals that myself and my partner on this project, Eric Pepin, consider to be important and various issues that have been approached with creating implantable stimulator chips. Chapter 1 served to introduce the ideas behind this thesis and provided relevant statistics as to why creating implantable stimulators is important. Chapter 2 covered the top level system description of the system that we aimed to create. In Chapter 3, a board level stimulation system was made, and in-vivo tests were performed on rats to confirm that the methodologies introduced in Chapter 2 were valid. The design of the circuits and systems that I created was the primary focus of Chapter 4. Finally, before this conclusion, the simulation results were discussed in Chapter 5.

There is potential for future work to be performed on this chip, and improvements to be made as it is integrated into a complete SoC. Advances towards the reduction of power consumption would benefit the entire system, and could be had by using an all digital PLL and completely dynamic comparator. The design of the comparator was often met with design

constraints that limited the flexibility that I had with design topologies. With more time, I'm confident that better designs could be achieved. Ultimately, I tried to take a logical approach when designing these circuits, and made sure to verify them as much as possible to ensure that they worked properly.

APPENDIX

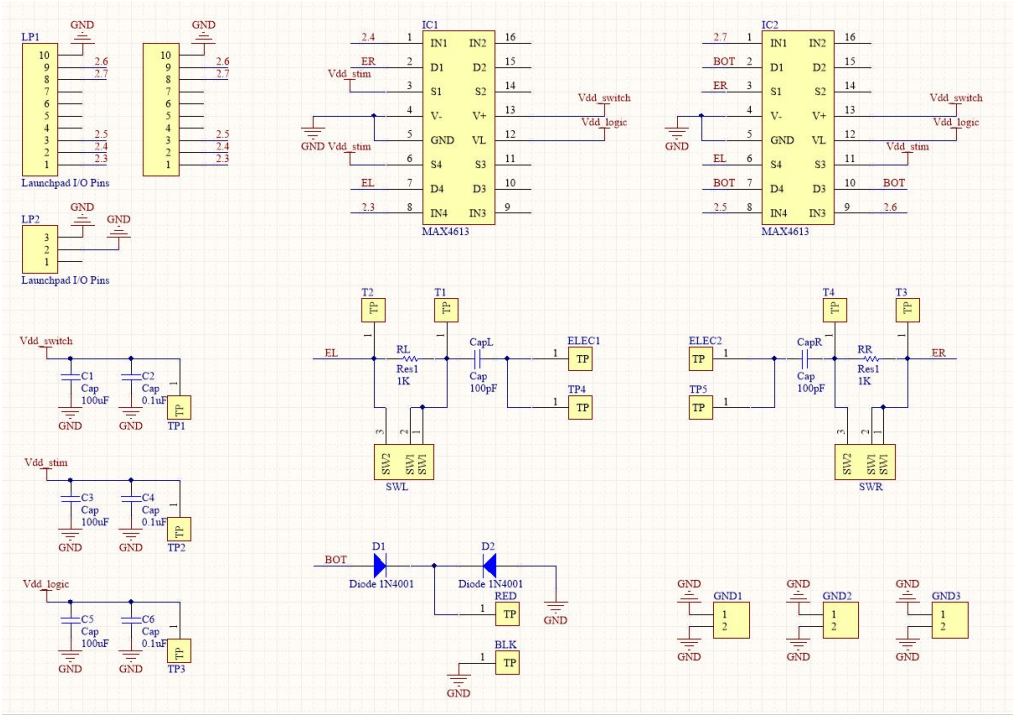


Figure A.1: HB-PCB schematic

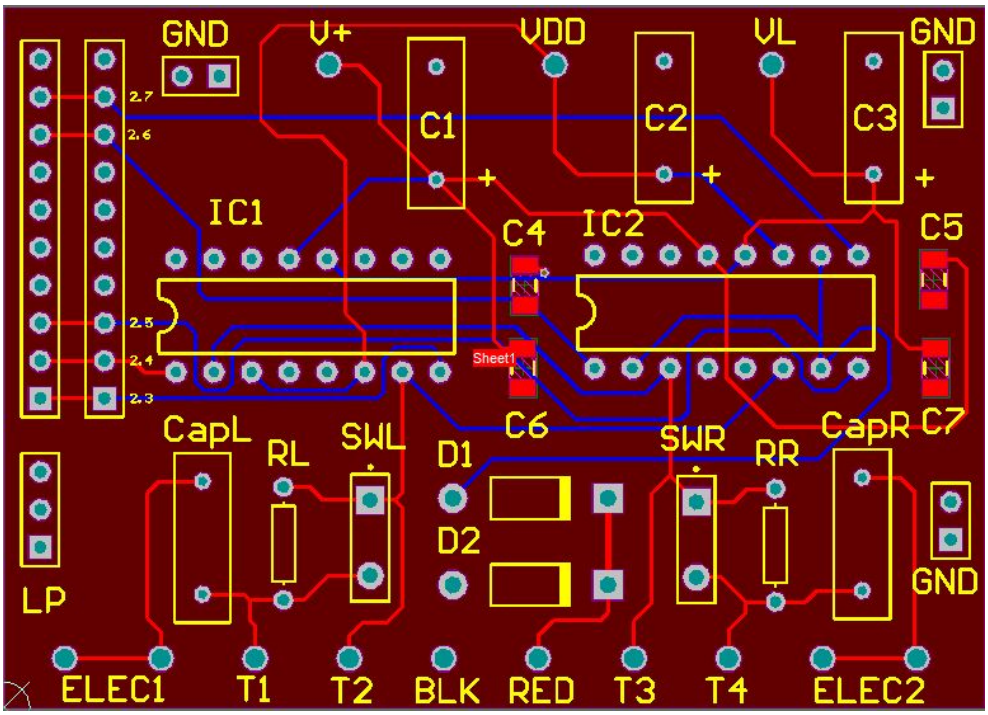


Figure A.2: HB-PCB layout

Table A.1: HB-PCB BOM

	Value	Board Reference	Digikey Part #	Price	Qty
Capacitor (Ceramic, SMD, 1206)	0.1 uF	C4, C5, C6, C7	399-1249-1-ND	0.1	4
Capacitor (Polyester, through hole)	1 uF	CapL, CapR	EF1105-ND	0.85	2
Capacitor (Alum. Electrolytic, through hole)	100 uF	C1, C2, C3	493-1548-ND	0.29	3
Diode (Rectifier, through hole)	N/A	D1, D2	UF4007-TPMSCT-ND	0.35	2
Resistor (through hole)	1 kΩ	RL, RR	CF14JT1K00CT-ND	0.1	2
Test Points (through hole)	N/A	All	5000K-ND	0.34	19
Analog Switch (16 pin, through hole)	N/A	IC1, IC2	MAX4613EPE+-ND	3.34	2
Slide Switch, SPDT (3 pin, 0.1" pitch, through hole)	N/A	SWL, SWR	N/A	0.75	2
2x8 IC Socket (0.1" pin pitch, 0.3" row spacing)	N/A	IC1, IC2 Header	609-4713-ND	0.28	2
Male-Male Pin Header (0.1" pin pitch, 1 row of 10)	N/A	MSP430 Connection	952-1902-ND	0.62	2
			Total	20.31	40

C code for the HB-PCB; main_header.h and main.c

```
/*
 * main_header.h for HB-PCB code
 *
 *  Created on: Apr 21, 2014
 *      Author: Daniel Micheletti
 */

#ifndef MAIN_HEADER_H_
#define MAIN_HEADER_H_

#define CYCLE_TIME 65e-9f
#define PULSE_WIDTH (PULSE_WIDTH_TIME/CYCLE_TIME)
#define PULSE_PERIOD (PULSE_PERIOD_TIME/CYCLE_TIME)-(2*PULSE_WIDTH)-
IP_DELAY_CYCLES-HIGH_Z_CYCLES
#define BURST_PERIOD (BURST_PERIOD_TIME/CYCLE_TIME)-
(PULSE_PER_BURST*PULSE_PERIOD)

//Function definitions
void set_Port1(void);
void set_Port2(void);
void set_Clock(void);
```

```
// Set parameter here to select which electrode sources current first
// Options: LEFT_ACTIVE or RIGHT_ACTIVE on Line 23
#define LEFT_ACTIVE
#ifdef LEFT_ACTIVE
        #define PULSE1_BITS 0x70
        #define PULSE2_BITS 0xC8
#elif RIGHT_ACTIVE
        #define PULSE1_BITS 0xC8
        #define PULSE2_BITS 0x70
#endif
#define IDLE_BITS 0x18
#define IP_DELAY_BITS 0x00
#define HIGH_Z_BITS 0x00

#endif /* MAIN_HEADER_H_ */

#include <msp430.h>
#include <math.h>
#include <float.h>
#include "main_header.h"

/*
 * main.c for HB-PCB
 */

//******************USER SPECIFIES PARAMETERS HERE************************//
// Also specify parameter which electrode sources current first in header file
#define IP_DELAY_CYCLES 50
#define HIGH_Z_CYCLES 50

// All mode settings
#define PULSE_WIDTH_TIME 200e-6f
#define PULSE_PERIOD_TIME 1000e-6f
// Single mode settings only
#define NUM_OF_PULSES 1
// Burst mode settings only
#define PULSE_PER_BURST 3
#define BURST_PERIOD_TIME 10e-1f

// Select which mode here - BURST/SINGLE/CONTINUOUS - by setting a single macro to 1
and the others to 0
#define SINGLE_MODE 1
#define CONTINUOUS_MODE 0
#define BURST_MODE 0
//************************************************************************//
```

```
typedef enum{
        RUNNING,
        WAITING
}program_state_t;

program_state_t program_state = WAITING;

int main(void) {
  WDTCTL = WDTPW | WDTHOLD;          // Stop watchdog timer

  set_Clock();
  set_Port1();
  set_Port2();

  unsigned int i;
  __enable_interrupt();

  while(1){
        if (program_state == RUNNING){
                if (SINGLE_MODE){
                        for (i = 0; i < NUM_OF_PULSES; i++){
                                P2OUT = PULSE1_BITS;
                                __delay_cycles(PULSE_WIDTH);
                                P2OUT = IP_DELAY_BITS;
                                __delay_cycles(IP_DELAY_CYCLES);
                                P2OUT = PULSE2_BITS;
                                __delay_cycles(PULSE_WIDTH);
                                P2OUT = HIGH_Z_BITS;
                                __delay_cycles(HIGH_Z_CYCLES);
                                P2OUT = IDLE_BITS;
                                __delay_cycles(PULSE_PERIOD);
                        }
                        program_state = WAITING;
                }
                else if (CONTINUOUS_MODE){
                P2OUT = PULSE1_BITS;
                __delay_cycles(PULSE_WIDTH);
                P2OUT = IP_DELAY_BITS;
                __delay_cycles(IP_DELAY_CYCLES);
                P2OUT = PULSE2_BITS;
                __delay_cycles(PULSE_WIDTH);
                P2OUT = HIGH_Z_BITS;
                __delay_cycles(HIGH_Z_CYCLES);
                P2OUT = IDLE_BITS;
```

```
                __delay_cycles(PULSE_PERIOD);
                }
                else if (BURST_MODE){
                        for (i = 0; i < PULSE_PER_BURST; i++){
                        P2OUT = PULSE1_BITS;
                        __delay_cycles(PULSE_WIDTH);
                        P2OUT = IP_DELAY_BITS;
                        __delay_cycles(IP_DELAY_CYCLES);
                        P2OUT = PULSE2_BITS;
                        __delay_cycles(PULSE_WIDTH);
                        P2OUT = HIGH_Z_BITS;
                        __delay_cycles(HIGH_Z_CYCLES);
                        P2OUT = IDLE_BITS;
                        __delay_cycles(PULSE_PERIOD);
                        }
                        __delay_cycles(BURST_PERIOD);
                }
        }
  }

        return 0;
}

//---- Clock Settings ----//
void set_Clock(void){
        DCOCTL = CALDCO_16MHZ; //Calibrate DCO to run at 16 MHz
        BCSCTL1 = CALBC1_16MHZ;
}

//---- Port 1 Pin Settings (8 Bit I/O) ----//
void set_Port1(void){
        P1DIR = ~(BIT3);     //Port 1 Pin Directions - OOOO IOOO
        P1REN = BIT3;                //Input pullup/downs enabled
        P1OUT = BIT3;                //Inputs have pullups and outputs are set to low
        P1IES = BIT3;          //Button interrupt enabled on high-to-low transition
        P1IFG = 0x00;          //Clear all interrupts
        P1IE = BIT3;
        //P1SEL |= (BIT4 + BIT7);   //This sends SMCLK (DCO) to P1.4 AND comparator out
to P1.7
}

//---- Port 2 Pin Settings (8 Bit I/O) ----//
void set_Port2(void){
  P2DIR = 0xFF;       //Port 2 Pin Directions - OOOO OOOO
  P2SEL = 0x00;       //Set Port 2 to be all I/O (P2.6/P2.7 on PUC/RESET not I/O)
  P2OUT = IDLE_BITS;        //Initialize outputs to idle
```

```
}
//---- Interrupts to set events ----///
#pragma vector=PORT1_VECTOR
__interrupt void Port_1_ISR(void){
        program_state = RUNNING;
        P1IFG = 0x00;
}
```

MATLAB code to design a type 2, 3rd order PLL

```
close all
clear all
clc
%{
Author: Daniel Micheletti
MATLAB code for the design of a type 2, 3rd order PLL

*All equations derived from the TI PLL App. Note starting at Pg
174

The transfer function of a 2nd order loop filter is given by:

  F(s) = (1 + s*C2*R2) / (s*(1 + s * (C1*C2*R2)/(C1+C2)))

     = (1 + s*T2) / (s*A0*(1 + s*T1))

      T2 = R2*C2
      T1 = R2*C2*C1 / C1+C2
      A0 = C1+C2
%}

% ----------- User Specifications -----------%
loop_bw_hz = 1000e3;  %in hertz
loop_bw_rad = 2*pi*loop_bw_hz;
phase_margin = 60;  %in degrees
gamma_opt_param = 0.7;
Icp = 5e-6;
Kphi = Icp; %charge pump gain in A
Kvco = 350e6; %VCO gain in Hz/V
Fout = 108.49e6; %output frequency in Hz
Fref = 13.56e6; %reference frequency in Hz
% -------------------------------------------%

% Calculate divider ratio
N = round(Fout/Fref);
```

```
% Calculate poles and zeros
T1 = (sqrt((1+gamma_opt_param)^2*tan(phase_margin*pi/180)^2+4*gamma_opt_param)
- (1+gamma_opt_param)*tan(phase_margin*pi/180))/ (2*loop_bw_rad);
T2 = gamma_opt_param/(loop_bw_rad^2*T1);

% Calculate capacitance sum
A0 =
((Kphi*Kvco)/(N*loop_bw_rad^2))*sqrt((1+loop_bw_rad^2*T2^2)/(1+loop_bw_rad^2*T1
^2));

% Solve final values
C1 = A0*T1/T2;
C2 = A0 - C1;
R2 = T2/C2;

% --- If you want to view the results of setting your own
% --- component values, uncomment this section and comment
% --- the above section out
% C1 = 5.0185e-12;
% C2 = 66.826e-12;
% R2 = 15.08e3;
%
% A0 = C1+C2;
% T2 = R2*C2;
% T1 = C1*T2/A0;
% --- End test values --- %

% Print component values to command window
C1_s = sprintf('C1 is %0.5g pF',C1/1e-12);
C2_s = sprintf('C2 is %0.5g pF',C2/1e-12);
R2_s = sprintf('R2 is %0.5g kOhms\n',R2/1e3);
disp('2nd ORDER LF COMPONENT VALUES');
disp(C1_s);
disp(C2_s);
disp(R2_s);

%{
Open loop response of a PLL is given by:

  H(s)*G(s) = Kphi * Kvco * F(s) / (s*N)

Useful functions:
  pzmap(F) - pole zero map
  rlocus(F) - root locus
  bode(F) - bode plot
```

```
%}

% Loop filter transfer function
s = tf('s');
F = (s*T2+1)/(A0*s*(s*T1+1));

% Loop gain transfer function
AB = Kphi*Kvco*F / (s*N);

% Closed loop transfer function
G = (Kphi*Kvco*(1+s*T2))/(A0*T1*s^3+A0*s^2+(T2*Kphi*Kvco/N)*s+Kphi*Kvco/N);

% Loop gain plots
margin(AB); %bode plot
x = gcr;
x.AxesGrid.Xunits = 'Hz';

% Closed loop plots
figure;
step(G); %default settling time value is 2%, see stepinfo()
title('Closed Loop Step Response');
y = stepinfo(G,'SettlingTimeThreshold',0.01); %settling time threshold to 1%
ySettle = y.SettlingTime;
yOvershoot = y.Overshoot;
legend(sprintf('Overshoot: %.1f %%\nSettling Time: %0.3g seconds (within
1%%)',y.Overshoot,y.SettlingTime));

disp('CLOSED LOOP POLE PARAMETERS');
damp(G) %Print natural frequency, damping ratio, and poles

% Closed loop zeros and poles
figure;
pzmap(G);
grid on
```

	Component	Value	Fingers	Multiplier
PLL TOP	M1-M10	2.4um/0.12um	1	2
	R1	30.18 kΩ		
	C1	16.7 pF		
	C2	1.23 pF		

	Component	Value	Fingers	Multiplier
PLL CP	M1,M4,M7,M12,M15	5um/0.5um	1	2
	M2,M3,M5,M6,M8,M9	0.39um/0.06um	4	1
	M10,M11,M13,M14	0.52um/0.06um	4	1
	C1	10 pF		

	Component	Value	Fingers	Multiplier
PLL VCO	M1	1um/1um	1	1
	M2,M3	2.5um/0.3um	1	1
	M4 - M13	1um/0.3um	1	1
	M14	1um/1um	1	1
	M15,M16	2.5um/0.08um	2	1
	M17 - M21	0.6um/0.3um	1	1
	M22 - M25	0.45um/0.3um	1	1
	M26 - M31	1.125um/0.08um	4	1
	M32,M33	0.76um/0.08um	1	1
	M34 - M37	1um/0.08um	1	1

	Component	Value	Fingers	Multiplier
IDAC TOP	M1	5um/1um	1	1
	M2	5um/1um	1	1
	M3	5um/1um	1	2
	M4	5um/1um	1	4
	M5	5um/1um	1	8
	M6	5um/1um	1	16
	M7	5um/1um	1	32
	M8	5um/1um	1	64
	M9	5um/1um	1	128
	M10	2um/0.12um	1	1
	M11	2um/0.12um	2	1
	M12	2um/0.12um	4	1
	M13	2um/0.12um	8	1
	M14	2um/0.12um	16	1
	M15	2um/0.12um	32	1
	M16	2um/0.12um	64	1
	M17	2um/0.12um	128	1
	M18	5um/0.28um	20	4

	Component	Value	Fingers	Multiplier
IDAC OTA	M1	4um/1um	4	1
	M2,M3	2.5um/0.5um	4	2
	M4,M5	1.75um/0.5um	1	1
	M6,M7	1um/0.5um	1	1
	M8,M9	2.5um/0.5um	1	1
	M10,M11	1um/0.5um	1	1
	M12	4um/1um	1	1
	M13	2um/0.5um	10	1
	M14,M15	0.6um/0.5um	1	1
	M16	0.55um/0.5um	1	1
	M17	3.25um/1um	1	1
	M18	2.5um/0.5um	1	1
	M19	0.5um/2um	1	1
	R1	4.37 kΩ		

	Component	Value	Fingers	Multiplier
COMP	M1	4um/1um	4	1
	M2,M3	2.5um/0.5um	4	2
	M4,M5	1.75um/0.5um	1	1
	M6,M7	1um/0.5um	1	1
	M8,M9	2.5um/0.5um	1	1
	M10,M11	1um/0.5um	1	1
	M12,M13	4um/1um	1	1
	M14,M15	2um/0.5um	10	1
	M16,M17	0.6um/0.5um	1	1

	Component	Value	Fingers	Multiplier
COMP BIAS	M1,M2	5um/1um	1	1
	M3	8um/1um	1	1
	M4	4um/1um	1	1
	M5	1um/1um	1	1
	M6	0.4um/14um	1	1
	M7	1um/0.5um	1	1
	R1	12.6 kΩ		

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