A 40nm CMOS Single-Ended Switch-Capacitor Harmonic-Rejection Power Amplifier for ZigBee Application

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Abstract

A 40nm CMOS single-ended switch-capacitor harmonic-rejection power amplifier for ZigBee application

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Chair of the Supervisory Committee:

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Electrical Engineering

This thesis describes a single-ended switch-capacitor harmonic-rejection power amplifier for the 915 MHz ISM band for ZigBee applications. A multipath feed-forward harmonic-rejection technique is employed to suppress the $2^{nd}/3^{rd}/4^{th}$ harmonics of the switch-capacitor power amplifier (PA) by 48/17/24 dB, respectively. The measured PA peak drain efficiency is 43% at a peak output power of 8.9dBm with the harmonic-rejection enabled. This PA was implemented in a 40nm TSMC CMOS process with an active area of 180μm×700μm.

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Chapter 1. INTRODUCTION

1.1 BACKGROUND

Devices utilizing the Wireless Personal Area Network (WPAN) continue to proliferate with the advent of low-power radio applications including wearable electronics for health monitoring, new sensing features and components for industrial control. Implementation of these transceivers as a single-chip CMOS solution continues to be attractive from the perspective of low-cost, potentially very low power consumption and exceptional small form factors. ZigBee has evolved as a popular WPAN standard to address numerous low-power applications. ZigBee applications, according to the 802.15.4 standards [1], has two frequency implementation bands. One is at 915MHz with Binary Phase Shift Key (BPSK) modulation, and the other is at 2.4GHz with Offset Quadrature Phase Shift Key (OQPSK) modulation. The 915MHz band is of interests for low power applications because of the favorable path loss properties as compared to the higher frequency commercial standards.

1.2 TRANSMITTER HARMONICS

ZigBee transceivers utilize constant-envelope BPSK/OQPSK modulation, thus allowing switch-mode topologies to implement small form-factor and high efficiency PAs. However, the non-linear nature of a switch-based PA will generate significant unwanted harmonic components. The fact that virtually all 915MHz ZigBee PAs are implemented as a single-ended device further exacerbates unwanted spurious components with a 2^{nd} Harmonic falling in the crowded 1.8 GHz spectrum (DCS 1800). In addition, the 3^{rd} and 4^{th} order harmonics can potentially interfere with

the International Mobile Telecommunication (IMT-E) and LTE bands. The harmonic components have the potential two ways to corrupt both the in-band and out-of-band receiver input signal:

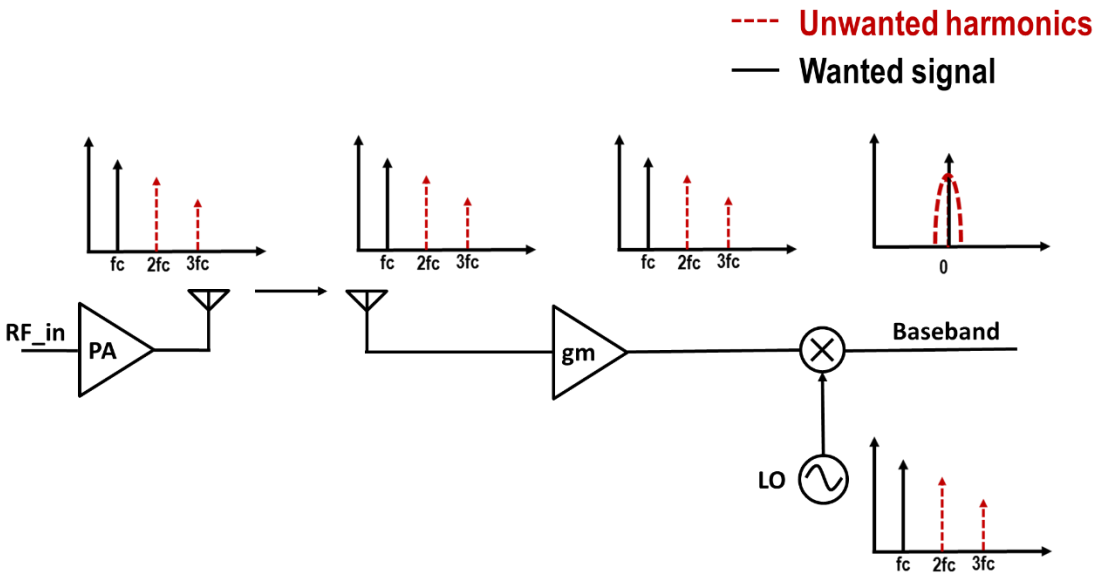

Figure 1.1. Effect of PA output harmonics on receivers at harmonic band.

For in-band receivers, the harmonic components corrupt the input signal through reciprocal mixing, especially receivers implemented without a narrow band Low Noise Amplifier (LNA). Take current-mode mixer topology as an example (Figure 1.1), the harmonic components will go through the gm stage with little attenuation because the gm stage is designed to be very wide band.

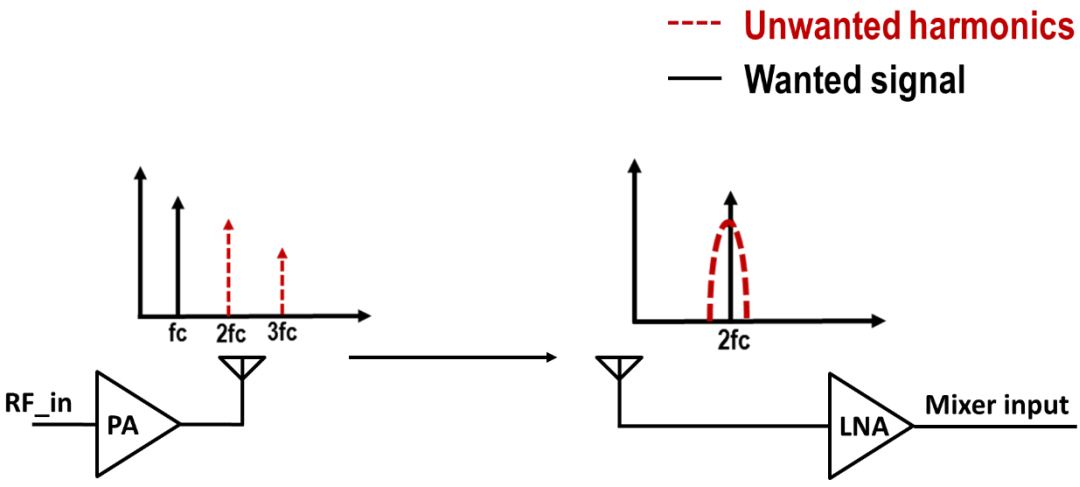

Figure 1.2. Effect of PA output harmonics on receivers in same band.

Then, the harmonic components that appear at the mixer input will mix with the harmonics of the LO to generate unwanted signals at the baseband which will corrupt the wanted (desired) signal. For receivers that are out of the transmitter's band, they might be in the same frequency band as the transmitter's harmonic band. So the harmonics will present as an in-band blocker to saturate the receiver front-end. (Figure 1.2).

Chapter 2. STATE-OF-THE-ART OF HARMINC SUPPRESSION/CANCELLATION TECHNIQUE

2.1 FILTER

A typical RF transmitter (Figure 2.1) comprises of a digital baseband, local oscillator (LO), mixers, PA, filters, and antenna. The traditional and widely used approach to reduce the PA output harmonics is adding a harmonic suppression filter, such as a low-temperature co-fired ceramic (LTCC) filter, at the PA output. The LTCC filter has the capability to integrate both passive and active components in a module to achieve the system-in-a-package (SiP) approach. A LTCC filter with less than 2 dB insertion loss and more than 60dB second order harmonic rejection at 2.4GHz has been reported [2].

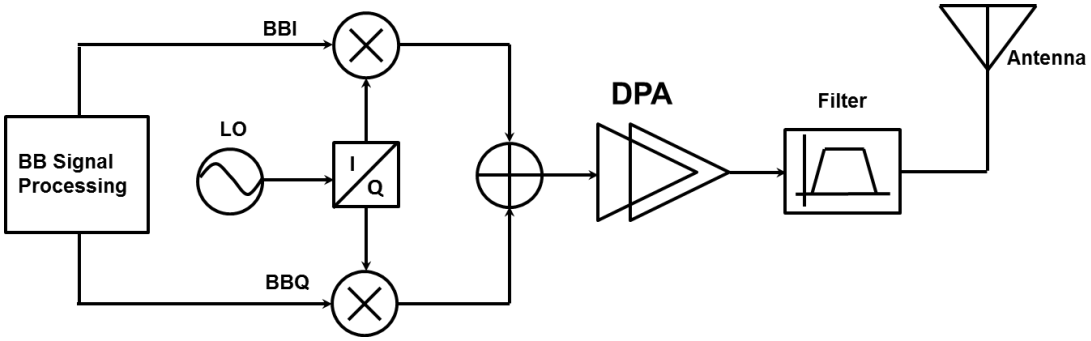

Figure 2.1. A conventional transmitter block diagram.

Using a discrete filter comes with limitations mainly, filters usually have an insertion loss larger than 1.5dB, resulting in a degradation of the PA output power and efficiency. Second, these filters are difficult to integrate on-chip because of the passive components which is usually done with large area inductors that have a low quality that would likely degrade the output power. Lastly, filters are frequency specific, thus having little use for highly-programmable software defined radio applications.

2.2 LOADS DESIGN FOR HARMONIC REJECTION

Certain types of PAs such as Class-E, Class-F, and Class-F^{-1} require harmonic load networks to eliminate harmonics in order to shape the voltage or current waveforms, to make the PA more efficient. Creating the ideal load impedance is known as the Zero Voltage crossing (ZVS), and Differential Zero Voltage Crossing (dZVS) condition [3]. When the impedance is optimized in these switched-based PAs, the overlap between the voltage and current in the switching device is minimized so the PA efficiency approaches 100%, theoretically. Therefore, a harmonic load

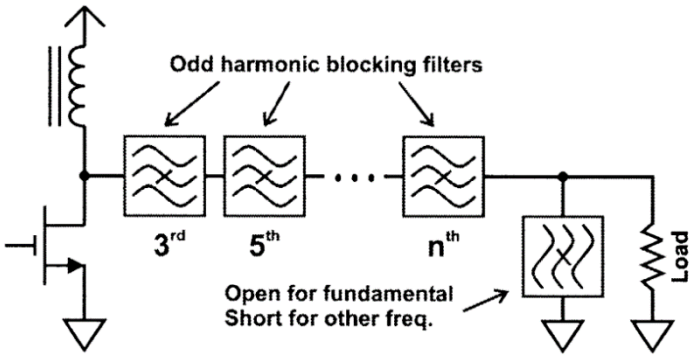

Figure 2.2. Typical Class-F PA topology.

matching network can decrease the output harmonics as well as increase the PA Power Added Efficiency (PAE) [4].

These harmonic blocking filters in a Class-F PA (Figure 2.2) helps shape the voltage waveform to achieve ZVS and dZVS. However, such harmonic traps and filters are limited to a specific PA class like Class-F. If integrated on chip, this class of harmonic peaking network in the RF frequency band, such as 915MHz, will utilize a prohibitively large amount of chip area due to the size and value of inductance required at lower operating frequencies (1GHz). Such topologies are usually implemented at mm-Wave band frequencies where both the value and physical size of the inductance is much smaller.

2.3 CONDUCTION ANGLE CALIBRATION

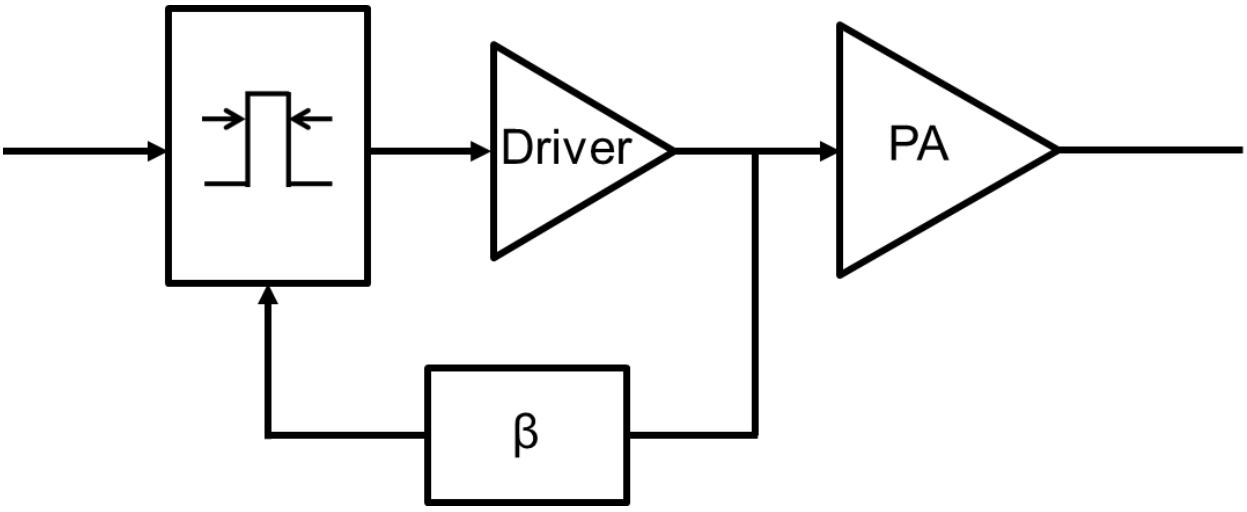

Figure 2.3. Conduction angle calibration system I.

Conduction angle calibration was proposed recently to cancel the second order harmonic [5], [6]. The input signal for the Class-D stage is a square wave, and the square wave's Fourier expansion contains fundamental component and corresponding harmonics. The coefficient of each harmonic component has a relationship with the duty cycle of the square wave. Therefore by adjusting the duty cycle of the input signal, the output second order harmonic can be minimized. Two different conduction angle calibration systems have been proposed but they are challenged with a variety of

practical issues. The first conduction angle calibration system (Figure 2.3) senses the second order harmonic at the buffer output/PA input. So this system only minimizes the input second order harmonic to the PA. The second order harmonic generated by the PA itself remains problematic. The other conduction angle calibration system (Figure 2.4) senses the signal at the PA output. This method successfully solves the issue of mitigating the self-generated harmonics, however this is done at the expense of increasing the total area and power by utilizing a replica PA, see fig 2.4. Therefore, both of these methods are problematic for high power applications. The first approach

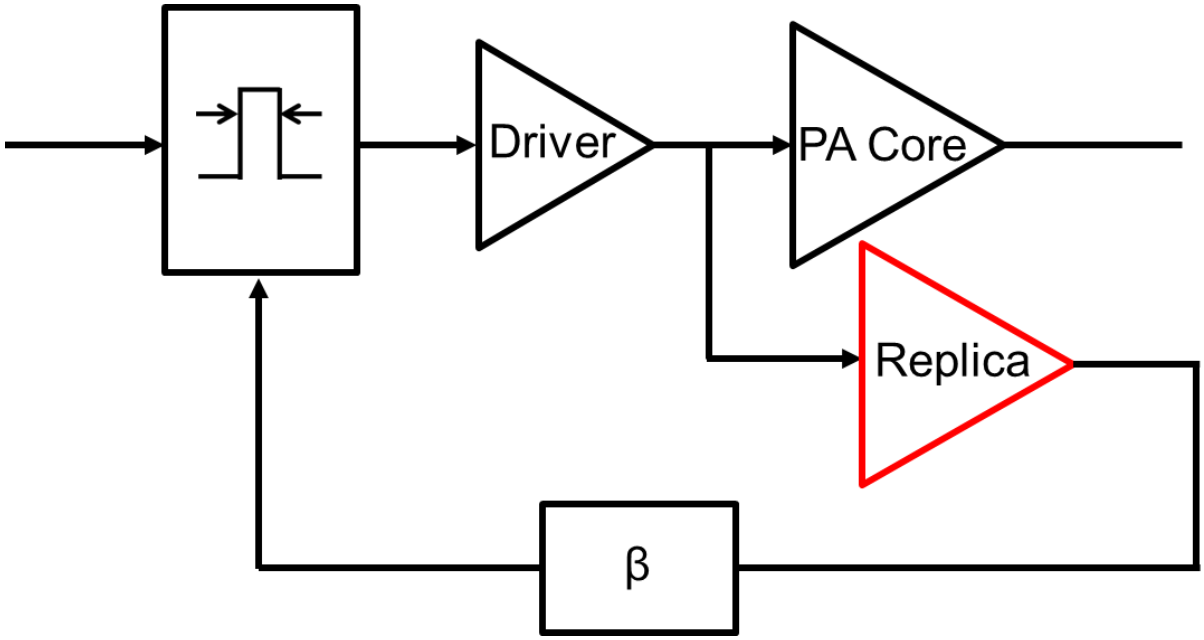

Figure 2.4. Conduction angle calibration system II.

[5] is not able to cancel the second order harmonic generated by the PA itself. The second approach[6] increases the power consumption and area for the entire PA.

2.4 POLYPHASE MULTIPATH CANCELLATION

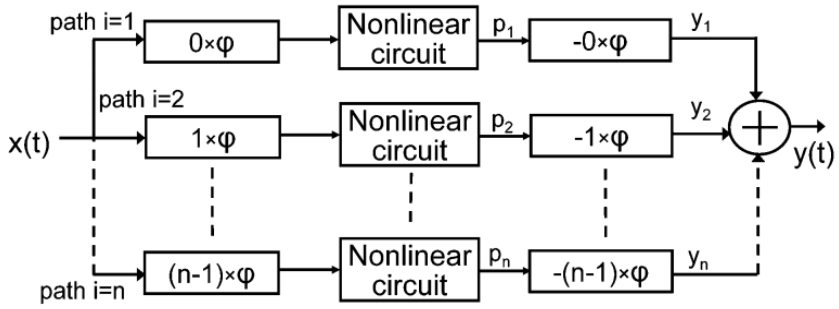

Figure 2.5. Polyphase multipath system diagram.

Polyphase multipath cancellation [7] is based on a feed-forward method which cancels the self-generated harmonic components. The basic idea is shown in (Figure 2.5) where the input signal is first split into n paths. Each path is then adds a unique phase shift to the harmonics without adding any phase shift to the fundamental (carrier) frequency. Finally, by combining all the paths all the paths, the self-generated harmonics of the non-linear circuits are cancelled while the fundamental frequency of interest remains intact. Polyphase multipath method is able to cancel the harmonic components very well, but it requires a complicated LO distribution system. In addition, this approach is it is not able to cancel any of the harmonics present at the input.

Chapter 3. HARMONIC-REJECTION POWER AMPLIFIER

3.1 HARMONIC REJECTION POWER AMPLIFIER (HRPA)

The aforementioned techniques have limitations with respect to targeting specific harmonics and are typically implemented at the expense of both power consumption and large silicon area. The proposed solution in this thesis which minimizes the power and efficiency degradation while providing a very clean cancellation on the harmonics is discussed next.

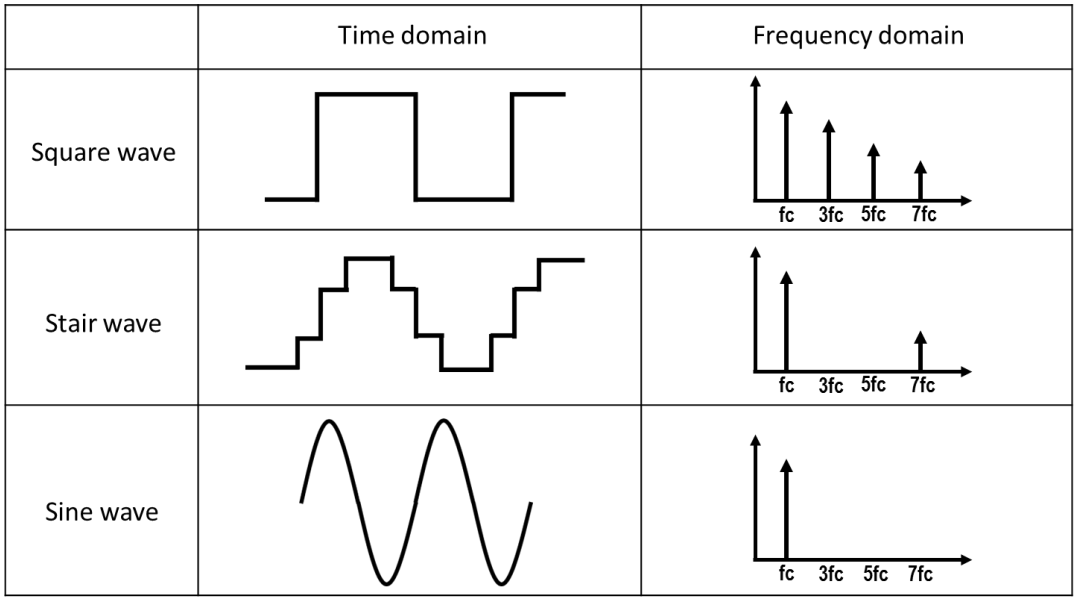

Figure 3.1. Time and frequency domain response for ideal waveforms.

3.1.1 *Stair wave function*

Going back to the fundamental principle surrounding the generation of a harmonic components of a square-wave function will provide some insight on how to more elegantly suppress unwanted harmonics. Assuming the square-wave has a 50% duty-cycle, in frequency domain the square-wave will have spectral content at the fundamental frequency in addition to spurious spectrum created at all the odd order harmonics; i.e. 3rd Harmonic, 5th Harmonic, etc. (Figure 2.5 row 1). If

square-waveforms with different gain and phase ratio are summed up, a staircase like wave function can be created (Figure 2.5 row 2). This staircase wave will not contain any third and fifth order harmonics if the proper phase and gain ratios are selected prior to combining these waveforms. It should be noted that if additional square waves are added on top of the proposed staircase waveform, the shape of the resulting waveform will eventually approach that of a sine wave, thus ideally cancelling out all the higher order harmonics. The question now arises as to how each of component of the staircase function can be generated in the PA of a wireless transmitter.

3.1.2 *HRPA Concept*

Similar ideas as compared to those introduced in a harmonic-rejection mixer [8] can be adopted in the design of a Harmonic-Rejection Power Amplifier (HRPA) by generating a staircase waveform in the PA output.

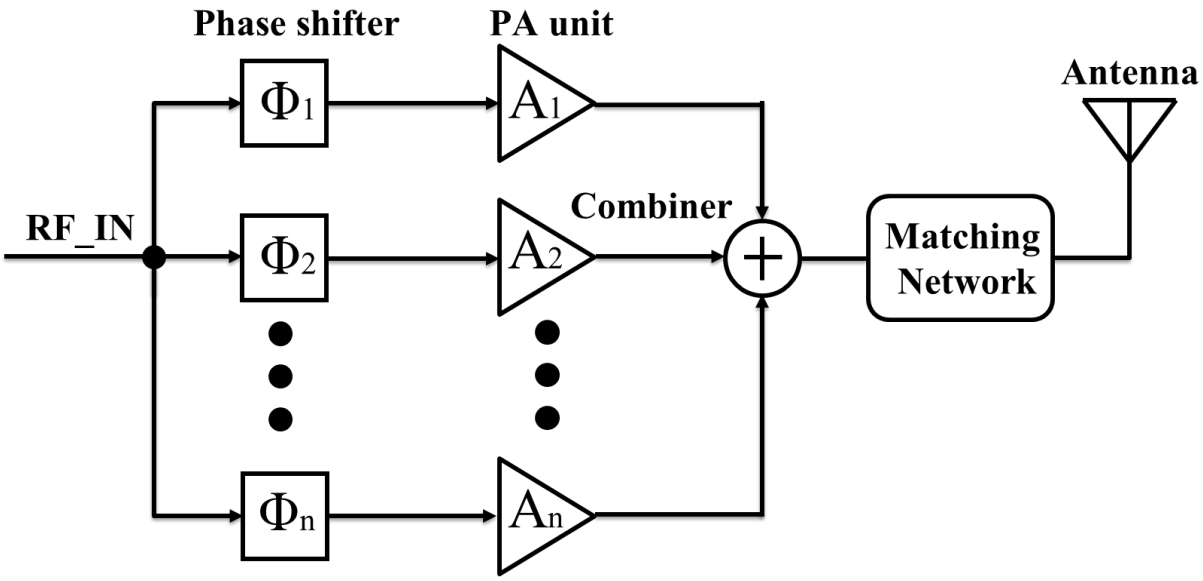

Figure 3.2. Conceptual block diagram for HRPA.

The HRPA system concept uses n driver paths each of which contain a digital phase shifter, a PA unit, an output power combiner and matching network, see fig 3.2. Accordingly, the baseband signal is frequency upconverted to RF where it is applied to the PA input. Multiple paths are then used in the PA, each with a specific phase shift and gain; by properly choosing the phase and gain ratios among the pathways, specific undesired harmonics of the combined signal path can be cancelled at the PA output, while the desired RF carrier is passed with little attenuation.

For ZigBee applications which transmit in the 915MHz band, the 2nd order harmonic becomes most problematic as it will fall directly onto 1800MHz ISM and DCS 1800 bands. This is further exacerbated by the fact that the 2nd Harmonic has the highest power amongst all the harmonics present in a square waveform. As such, it is typically imperative to minimize the 2nd order

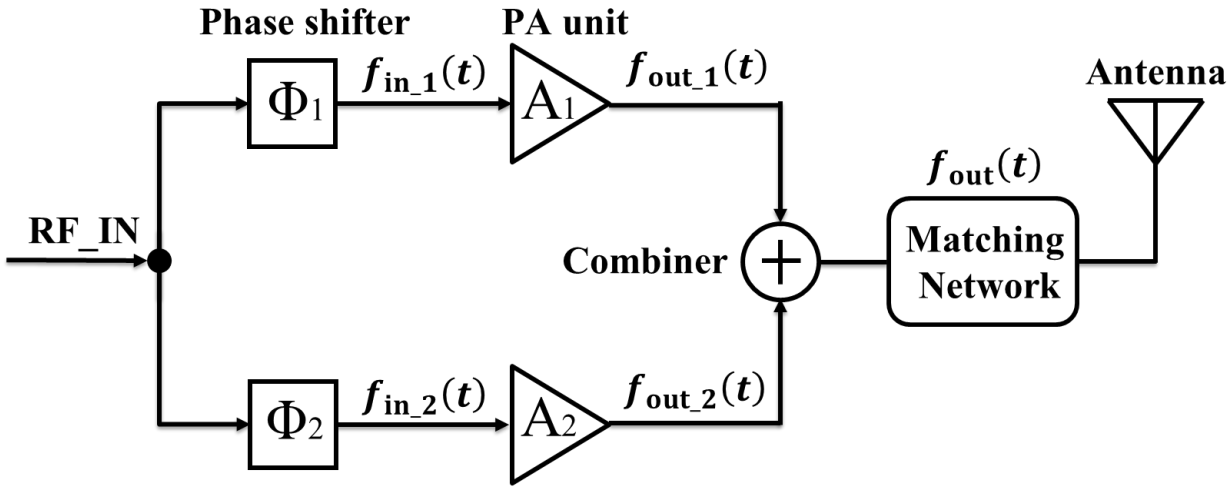

Figure 3.3. Block diagram for HRPA with n=2.

harmonic to eliminate the possibility of interfering with users in the 1800MHz band. To achieve that, a HRPA system with n=2 can be implemented:

To analyze the cancellation performance of such system, a Fourier Expansion is applied to the input signal. Assuming other than the fundamental frequency, the input signal contains a series of unwanted sinusoidal harmonic signals with different amplitudes. The fundamental signal has an

amplitude of a_1 and a phase of θ, the second harmonic has an amplitude of a_2 and a phase of 2θ, and etc. So when represented as a phasor, the RF input signal should have the following form:

$$\text{RF input signal} = a_1 e^{-i\theta} + a_2 e^{-2i\theta} + a_3 e^{-3i\theta} + \cdots \quad (3.1)$$

Now assuming that the phase shifter blocks provide a phase shift of Φ_1/Φ_2 related to the original phase with identical gain (assuming gain of 1 here), so the waveform at the output of the phase shifters $f_{in\_1}(t)$, and $f_{in\_2}(t)$ should have the following form:

$$f_{in\_1}(t) = a_1 e^{-i(\theta+\Phi_1)} + a_2 e^{-2i(\theta+\Phi_1)} + a_3 e^{-3i(\theta+\Phi_1)} + \cdots \quad (3.2)$$

$$f_{in\_2}(t) = a_1 e^{-i(\theta+\Phi_2)} + a_2 e^{-2i(\theta+\Phi_2)} + a_3 e^{-3i(\theta+\Phi_2)} + \cdots \quad (3.3)$$

If the PA unit provides the same gain for signals at all frequency, and assuming the top path has a gain of A_1, and bottom path has a gain of A_2, the output signals of the PA units are:

$$f_{out\_1}(t) = A_1(a_1 e^{-i(\theta+\Phi_1)} + a_2 e^{-2i(\theta+\Phi_1)} + a_3 e^{-3i(\theta+\Phi_1)} + \cdots) \quad (3.4)$$

$$f_{out\_2}(t) = A_2(a_1 e^{-i(\theta+\Phi_2)} + a_2 e^{-2i(\theta+\Phi_2)} + a_3 e^{-3i(\theta+\Phi_2)} + \cdots) \quad (3.5)$$

By summing two output signals up, the fundamental and HD_2 (2^{nd} Harmonic distortion) are:

$$\text{Fundamental} = a_1(A_1 e^{-i(\theta+\Phi_1)} + A_2 e^{-i(\theta+\Phi_2)}) \quad (3.6)$$

$$HD_2 = a_2(A_1 e^{-2i(\theta+\Phi_1)} + A_2 e^{-2i(\theta+\Phi_2)}) \quad (3.7)$$

$$HD_3 = a_3(A_1 e^{-3i(\theta+\Phi_1)} + A_2 e^{-3i(\theta+\Phi_2)}) \quad (3.8)$$

If equation 3.7 is equal to 0, this will represent complete cancellation of the 2nd order harmonic. Setting A_1=1, and $\theta=\Phi_1=0$, in equation 3.7, then solving for A_1, Φ_1, and Φ_2,

$$A_1 = A_2 = 1 \quad (3.9)$$

$$\Phi_1 = 0°, \Phi_2 = 90°, \quad (3.10)$$

The PA is a very non-linear block. It will generate unwanted harmonic component regard to a single tone input. The time domain response for the PA is:

$$f_{out}(t) = A_1 f_{in}(t) + A_2 {f_{in}}^2(t) + A_3 {f_{in}}^3(t) + \cdots \quad (3.11)$$

The proposed HRPA system is not only able to cancel the input harmonics, but is also able to address the harmonic components generated by the PA itself due to non-linearity.

The fundamental signal goes into the PA unit and has the following form:

$$f_{in\_1}(t) = a_1 e^{-i\Phi_1} \quad (3.12)$$

$$f_{in\_2}(t) = a_1 e^{-i\Phi_2} \quad (3.13)$$

Therefore, the non-linear response of the fundamental frequency at the PA output is:

$$f_{out\_1}(t) = a_1(A_1 e^{-i\Phi_1} + A_1 e^{-2i\Phi_1} + A_1 e^{-2i\Phi_1} + \cdots) \quad (3.14)$$

$$f_{out\_2}(t) = a_1(A_2 e^{-i\Phi_2} + A_2 e^{-2i\Phi_2} + A_2 e^{-2i\Phi_2} + \cdots) \quad (3.15)$$

The second order harmonic component after summing up at the PA output will be:

$$HD_2 = a_1(A_1 e^{-2i\Phi_1} + A_2 e^{-2i\Phi_2}) \quad (3.16)$$

So plugging in the solution from 3.9-3.10 back into 3.16, one observes that the 2nd order harmonic component will also get cancelled.

Therefore, the proposed HRPA structure is able to cancel both the harmonics that are already present at the PA input to the input, and those which self-generated harmonics by the PA itself.

3.1.3 *Limitation of HRPA with n=2*

A HRPA with n=2 is able to cancel both the input 2nd order harmonic and self-generated harmonics but with limitations.

The HRPA with n=2 is not able to cancel the 3rd and 4th order harmonics. Plugging in the solution for 3.9-3.10 back into 3.8 will give:

$$HD_3 = a_1(1 + e^{-i\frac{3}{2}\pi}) \quad (3.17)$$

$$HD_4 = a_1(1 + e^{-i2\pi}) \quad (3.18)$$

The magnitude of the 3rd and 4th order harmonics will be:

$$|HD_3| = \sqrt{2}a_1 \tag{3.19}$$

$$|HD_4| = 2a_1 \tag{3.20}$$

So n=2 will increase the third and fourth order harmonics. Increase n to a large number will solve this problem since one more paths will introduce an extra degree of freedom to cancel out additional harmonics. As such, if a designer wants to target cancelling n^{th} order harmonics, a HRPA system will require at least n+1 paths to achieve this cancellation.

3.1.4 *HRPA with n=3 paths*

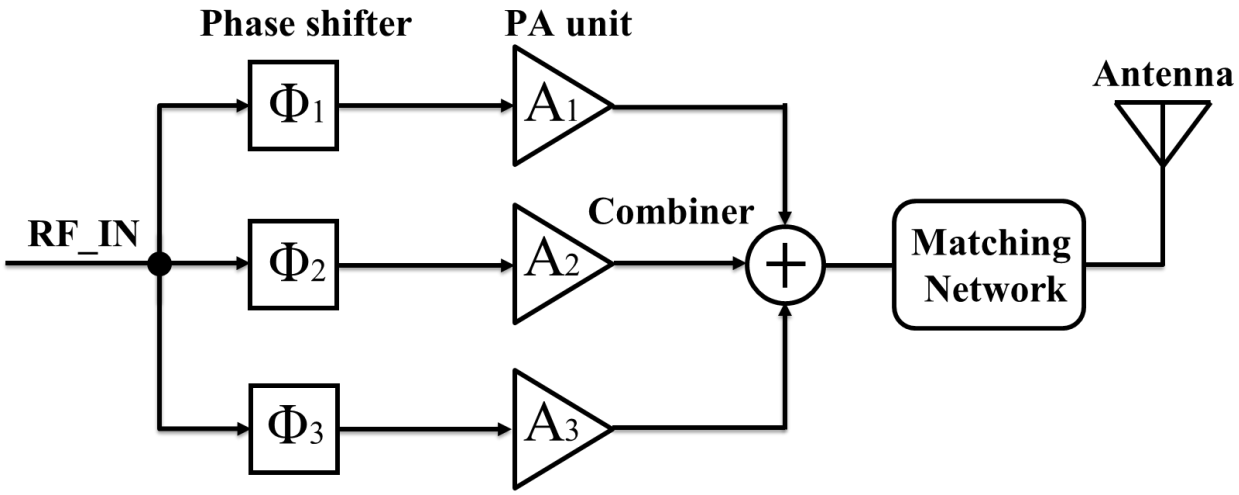

Figure 3.4. Block diagram for HRPA with n=3 paths.

As such, an HRPA with n = 3 is able to cancel out two harmonics. The harmonic components at the PA output will have the following form:

$$HD_2 = A_1 e^{-2j\Phi_1} + A_2 e^{-2j\Phi_2} + A_3 e^{-2j\Phi_3} \tag{3.21}$$

$$HD_3 = A_1 e^{-3j\Phi_1} + A_2 e^{-3j\Phi_2} + A_3 e^{-3j\Phi_3} \quad (3.22)$$

$$HD_4 = A_1 e^{-4j\Phi_1} + A_2 e^{-4j\Phi_2} + A_3 e^{-4j\Phi_3} \quad (3.23)$$

Normalizing all three terms regard to $A_2 e^{-nj\Phi_2}$(i.e. setting A_2=1 and Φ_2=0), the equation set will be simplified to:

$$HD_2 = A_1 e^{-2j\Phi_1} + 1 + A_3 e^{-2j\Phi_3} \quad (3.24)$$

$$HD_3 = A_1 e^{-3j\Phi_1} + 1 + A_3 e^{-3j\Phi_3} \quad (3.25)$$

$$HD_4 = A_1 e^{-4j\Phi_1} + 1 + A_3 e^{-4j\Phi_3} \quad (3.26)$$

Using Euler's formula to expand equation 3.21-3.23, produces six equations:

$$HD_2 = A_1 \cos(2\Phi_1) + 1 + A_3 \cos(2\Phi_3) \quad (3.27)$$

$$HD_2 = j(A_1 \sin(2\Phi_1) + A_3 \sin(2\Phi_3)) \quad (3.28)$$

$$HD_3 = A_1 \cos(3\Phi_1) + 1 + A_3 \cos(3\Phi_3) \quad (3.29)$$

$$HD_3 = j(A_1 \sin(3\Phi_1) + A_3 \sin(3\Phi_3)) \quad (3.30)$$

$$HD_4 = A_1 \cos(4\Phi_1) + 1 + A_3 \cos(4\Phi_3) \quad (3.31)$$

$$HD_4 = j(A_1 \sin(4\Phi_1) + A_3 \sin(4\Phi_3)) \quad (3.32)$$

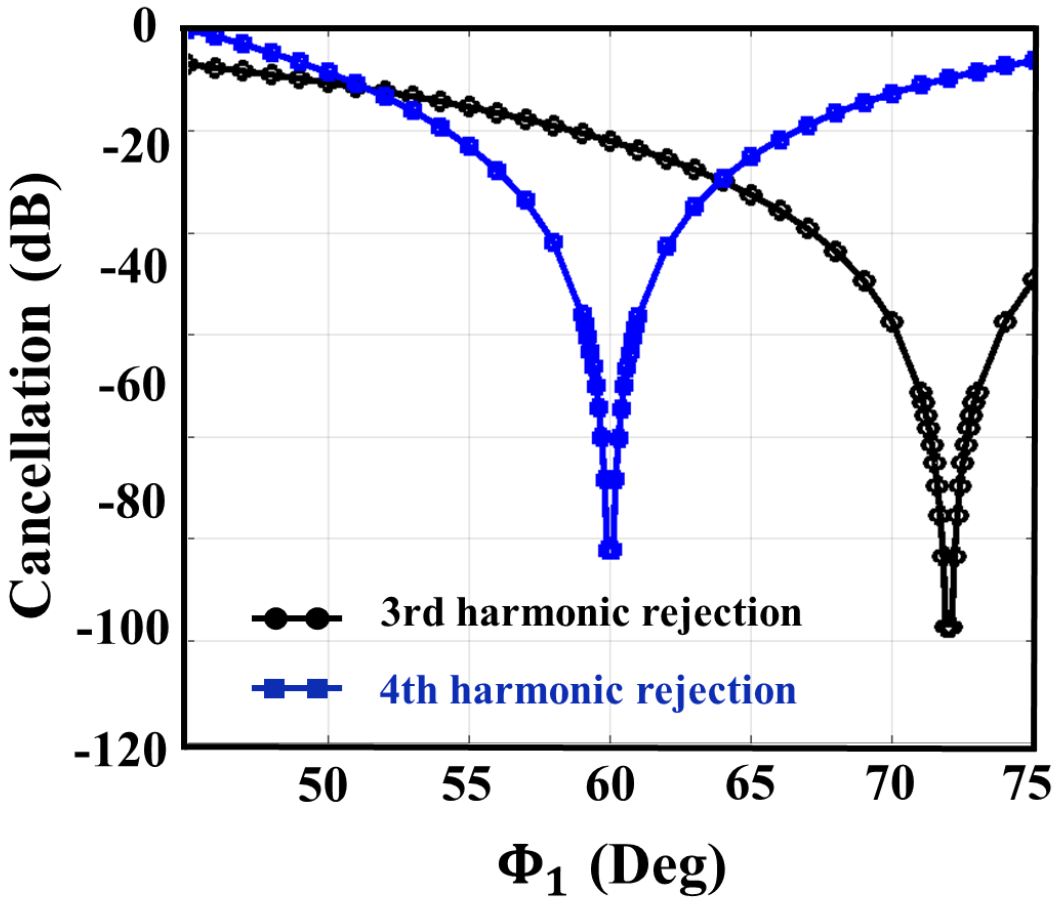

Figure 3.5. $3^{rd}/4^{th}$ order harmonic cancellation with HD2 set to zero.

From Eq. (3.27)-(3.32), setting $HD_2=HD_3=HD_4=0$ will result in 6 equations but only 4 variables. Thus, a single solution cannot be obtained to *completely* cancel all three harmonics, simultaneously. This can only be done with additional driver paths. However, with n-3, the HRPA can be configured to completely cancel the HD_2 with a partial cancellation of HD_3 and HD_4. Normalizing $A_1 = A_3 = 1$, $\Phi_3 = -\Phi_1$, and $\Phi_2 = 0$ and assuming no mismatch, from Eq. (3.21-2.23), A_2 can be solved as a function of Φ_1 by setting $HD_2=0$, plots may be generated for HD_3 and HD_4 as a function of Φ_1 (Fig. 2). Although there is a window where the cancellation is greater than 20dB, the HD_3 and HD_4 suppression is maximized when $\Phi_1=64°$ which maps to an $A_2=1.23$.

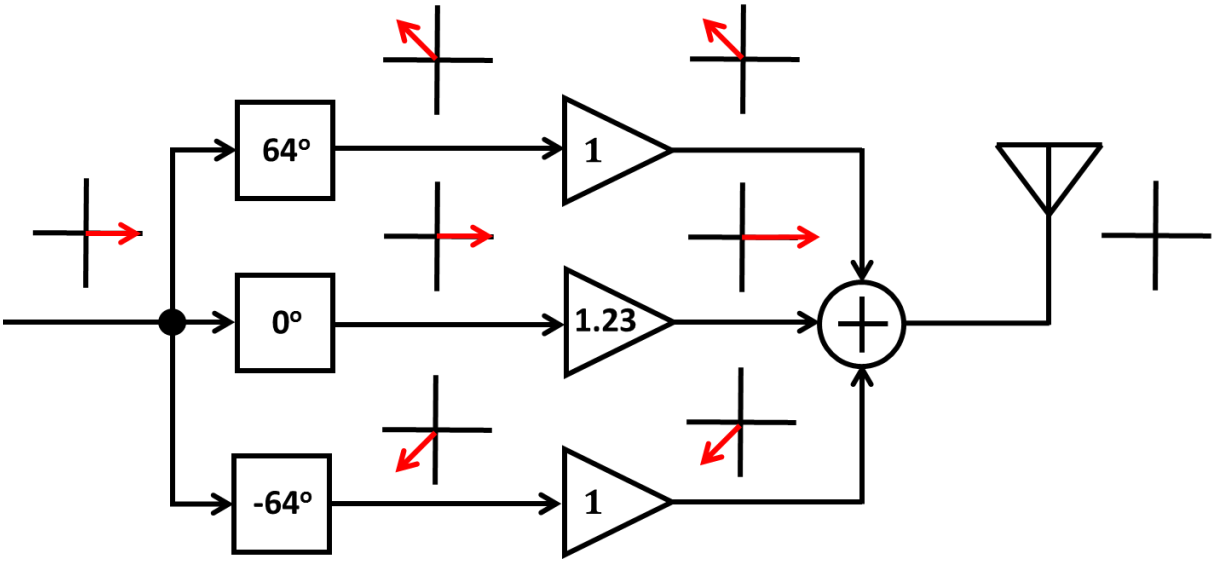

Figure 3.6. Frequency plot showing the cancellation of input third harmonics.

A more intuitive description of how the HPRA works in the specific case that n=3 and is configured to cancel the 2nd order harmonic is shown in (Fig. 3). The 2nd order harmonic presented to the PA input is shown as a red phasor with 0° of phase shift. After passing through the phase shifters in each of the three paths, the 2nd order rotates such that the phase relationship between the three paths will allow complete cancellation when combined at the PA output.

While in the prior example the harmonics which are already present at the PA input will experience cancellation, the question arises as to the cancellation of the harmonics which are generated by the PA driver stages as the signal passes from the input to the output. Each PA driver has its own non-linearity that will "self-generate" 2nd order harmonics. Applying the same phasor argument (Fig. 3.7) with the blue arrow representing the fundament, f_0, the phasor summation of the self-generated 2nd order, again sums to zero at the power combiner output. Accordingly, the 3-path HRPA can achieve cancellation of both the PA input and self-generated 2nd order harmonics.

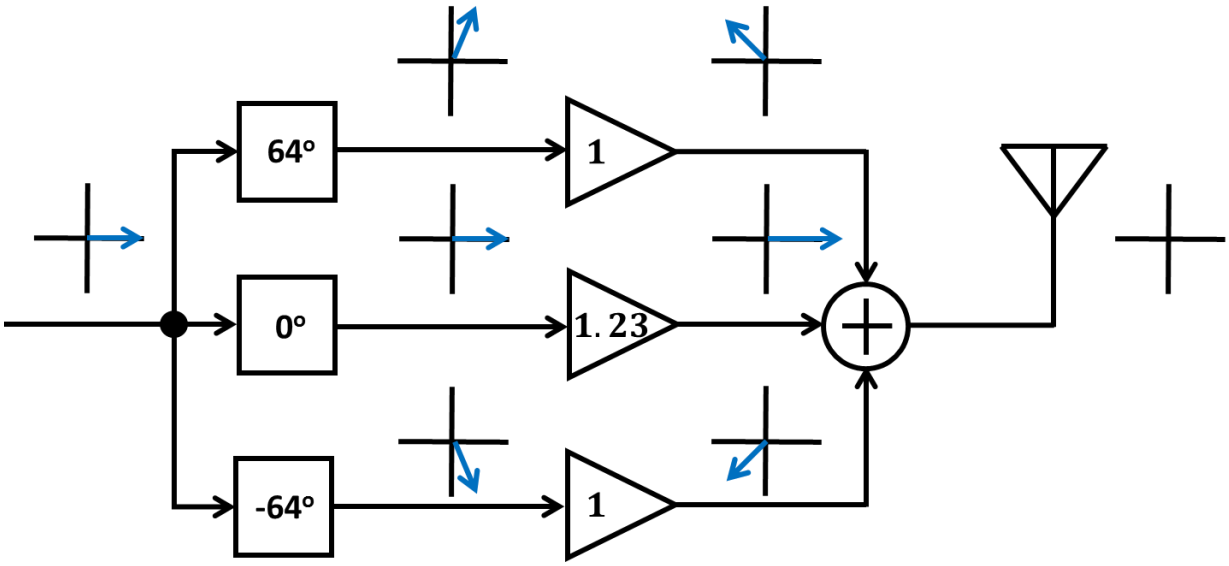

Figure 3.7. Frequency plot showing the cancellation of self-generated third harmonics.

3.2 PA CLASSES

PA consists of at least three components (Figure 3.8), the input device, DC feed components and matching network. Different methodologies may be applied to the design on these three components, and will ultimately determine the class of PA operation.

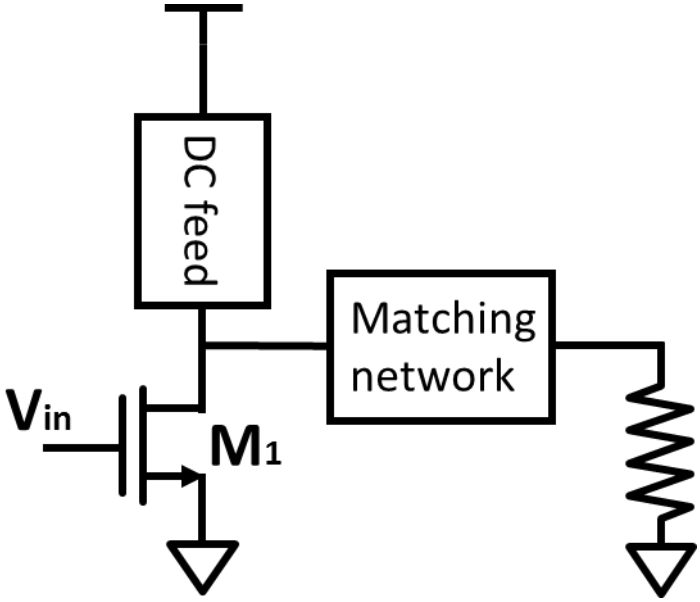

Figure 3.8. Ideal block diagram for PA.

3.2.1 *Linear PA*

A general characteristic of linear amplifiers is to bias the transconductance device in a region where it is conducting of the entire cycle of the input signal. As such, if this input device, typically connected as a common-source amplifier, operates as a transconductance stage, the output signal

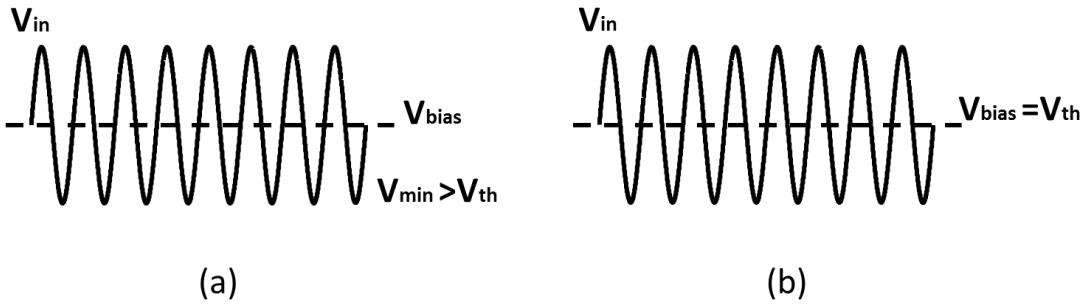

Figure 3.9. (a) Input signal for Class-A PA, (b) Input signal for Class-B PA.

will have a linear relationship with the input signal. Therefore, this type of PA can be categorized as linear PA. Under the realm of linear PAs, there are different classes which can be categorized relative to the amount of time per period of the carrier signal that the input device is turned on. If the input device is always on, this type of PA is called a Class-A PA. If the input device only turns on for half of the input cycle, this type of PA is called Class-B PA. If the input device turns on between a full cycle and a half cycle, this type of PA is called Class-AB PA. The conduction angle is set by the bias voltage at the gate of the input device, which is the DC bias voltage for V_{in} (Figure 3.9). Class-A operation can be set by making the minimum value for V_{in} bigger than V_{th} (Figure 3.9(a)), and Class-B operation can be set by making the DC bias voltage of V_{in} equal to V_{th}.

3.2.2 *Switch-type PA*

If the input device operates as a switch, this type of PA is called non-linear PA or switch-type PA. Among non-linear PAs, the class can be further divided based on the designs of DC feed components and the matching network.

If the DC feed component is a complementary PMOS device, this type of PA is called Class-D PA (Figure 3.10 (b)). If the DC feed component is an inductor, this type of PA falls into Class-E/F PA (Figure 3.10(a)). If the matching network contains harmonic termination, this type of PA is Class-F PA (Figure 2.2).

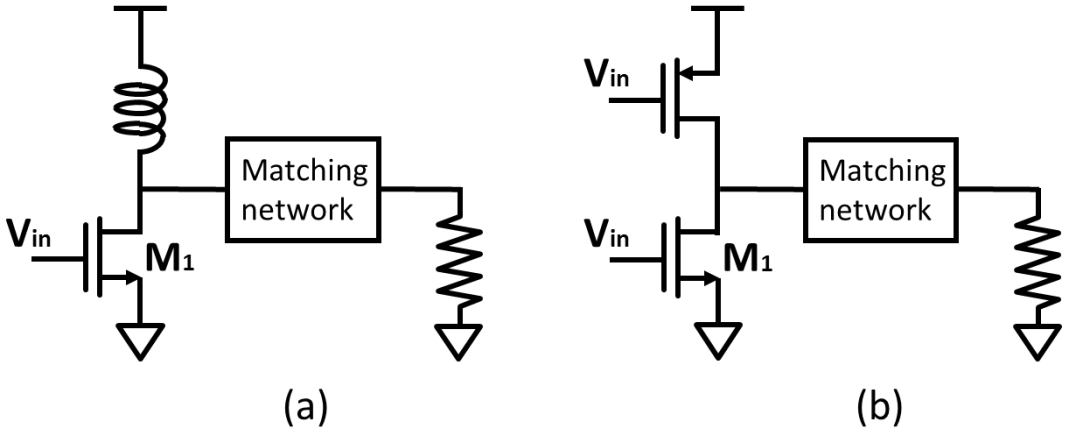

Figure 3.10. (a)Class-E/F PA, (b) Class-D PA.

The input device M_1 for Switch-type PA (Figure 3.8) only turns on when the input signal is a logic high. When the input device is turning on, assuming ideal case that the input device R_{on} is zero, so there is no voltage drop across the source and drain of the input device. When the input device is turning of, the supply starts to charge the load and generates output voltage. So theoretically there is no overlap between the voltage at the output node of the input device and the current flowing through input device. Thus making the efficiency for switch-type PA 100%. The non-overlapping voltage and current, however, leads to a shortcoming that switch-type PA is only able to amplify signal with phase information. Therefore, switch-type PAs by itself is only able to amplify constant

envelope modulated signals such as FSK, BPSK, QPSK and etc. In order to amplify the amplitude modulated signal, a more sophisticated system must be implemented to linearize the switch-based PAs.

3.2.3 *PA class for HRPA implementation*

In general, the HRPA can be implemented with all PA classes mentioned above. However, there are practical considerations which are revealed after more careful analysis. In the case of a linear PA, it is redundant to implement harmonic rejection function because by definition the PA is linear and therefore does not produce harmonic components. On the other hand, implementing a harmonic-rejection function for a switch-based PAs is more beneficial as there are strong harmonics produced. The nature of switch-type PA makes it generate high order harmonics which potentially could violate emission limits outlined for radios in other standards. The proposed harmonic rejection technique provides an approach to canceling the harmonics in a switch-based PA, obviating the need for an external discrete RF filter. In addition, removing the need for the front-end RF filter helps to reduce PA and transmitter losses and ultimately improve the efficiency of the overall system.

While implementing the overall harmonic rejection function for a switch-type PA is promising with respect to cancelling unwanted spurious transmitter components, designing the correct load for the output of the PA becomes quite challenging. Unlike a harmonic rejection mixer, each PA

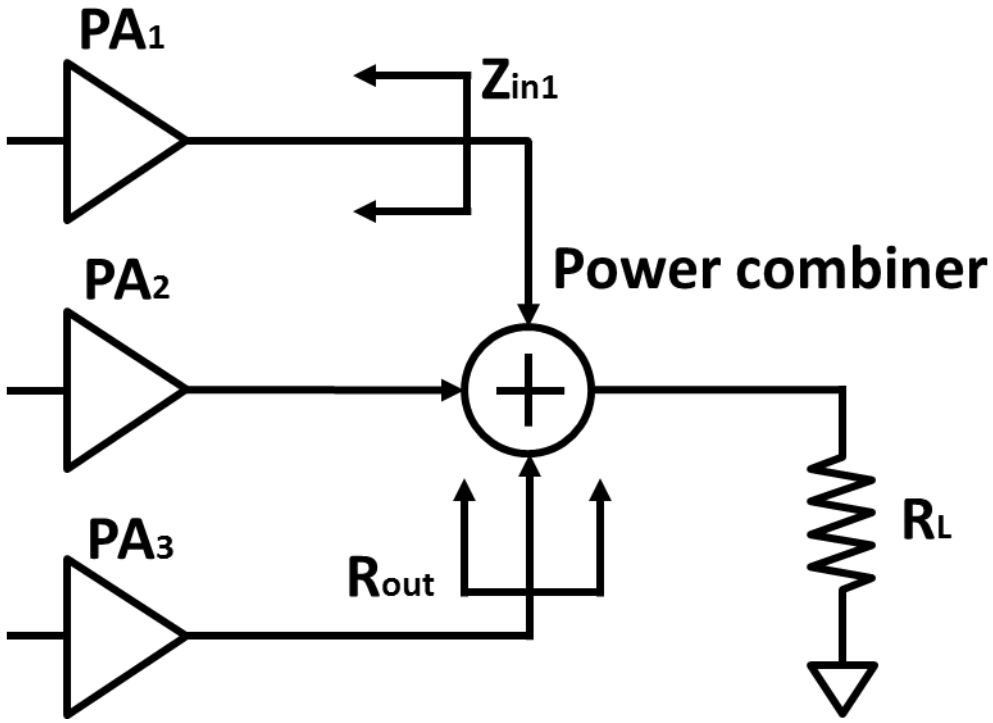

Figure 3.11. Output impedance for single HRPA unit cell.

unit of an HRPA is directly driving a comparatively small output impedance. The input load impedance R_{out} for each PA unit (Figure 3.11), mainly comprised of two parts, the load impedance R_L, and the input impedance looking into other PA units such as Z_{in1}. If the PA is modeled as an ideal current source, the Z_{in1} is infinite so it will not affect the output impedance. If the PA is modeled as an ideal current source with finite parallel impedance, and all the PA units are turn on and off at the same time, Z_{in1} will not impact the output impedance. However for the case of the HRPA, which requires different PA unit cells turning on and off at different times. For example, PA_3 and PA_1 in Figure 3.11 will be on at different times. In this case, Z_{in1} will influence the output impedance of PA_3.

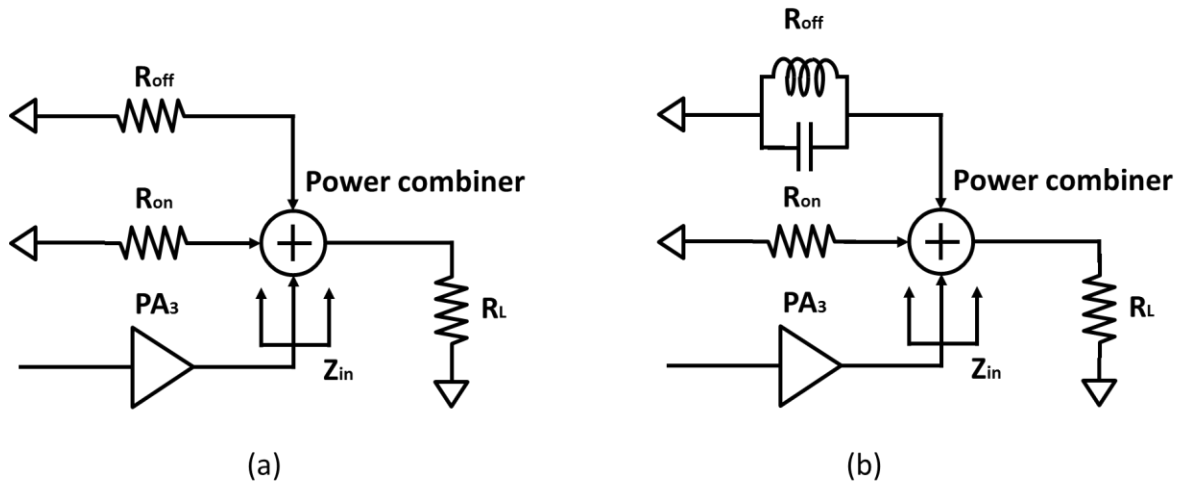

Figure 3.12. Model of loading (a) for Class-D PA, (b) for Class-E/F PA.

Depending on the class of PA, Z_{in1} will present different impedance. When an individual PA unit is on, it will present a finite on resistance, and when the PA unit is off the impedance becomes a parasitic capacitance in parallel with a DC feed component impedance. Assuming PA_1 is on, and PA_2 is off (Figure 3.11), for Class-D PA, PA_1 presents the on resistance of an NMOS transistor, and PA_2 presents the on resistance of PMOS (Fig 3.12 (a)). So for the class-D PA, if the PMOS and NMOS are sized properly, the impedance contributed by the other PA units remains roughly at R_{on}. For other types of PAs using an inductor as a DC feed component, PA_1 presents a parasitic capacitor and a DC feed inductor in parallel, and PA_2 presents an on resistance (Fig 3.12 (b)). It is hard to make the parasitic capacitor and the DC feed inductor resonant at the correct operating frequency with a reasonable Q, such that the same R_{on} is presented as when the input device is turning on.

In conclusion, a class-D PA will create less impedance deviation for HRPA operation compared to a Class E/F PA. But the extra impedance still remains a problem which calls for a good output power combiner to isolate the extra impedance.

3.3 OUTPUT POWER COMBINER DESIGN

The HRPA requires an output combiner to add the signals from each of the different paths to achieve harmonic cancellation function. It is hard to realize an output combiner as compared to

Figure 3.13. Ideal 2-to-1 combiner.

the relative ease of combining signals when using a harmonic rejection mixer. This is mainly due to the PA driving a small load impedance. As such, the design of the PA output power combiner must address this challenge of a low load impedance.

3.3.1 *Isolated output power combiner*

Output power combiners are usually realized using some form of a passive component. The implementation of an integrated output power combiner is generally divided into two categories: isolated power combiners and non-isolated power combiners. The difference between the isolated power combiner and non-isolated power combiner is their coefficients (S parameter) between two input ports are different. Assuming port 2 and port 3 are input ports and port 1 is output port (Figure 3.13). The combiner is passive, so the S parameter is reciprocal. As such, the S_{23} equals to S_{32} equals to 0. S_{23} and S_{32} equal to zero means the two input signals will have no effect on each other.

This kind of matching network is called isolated power combiner. Wilkinson lines are typically used isolated output power combiner. The S_{23} for Wilkinson line power combiner (Figure 3.14) is 0. The isolation is achieved with a resistor between port 2 and port 3 ($2Z_0$ in Figure 3.14). A

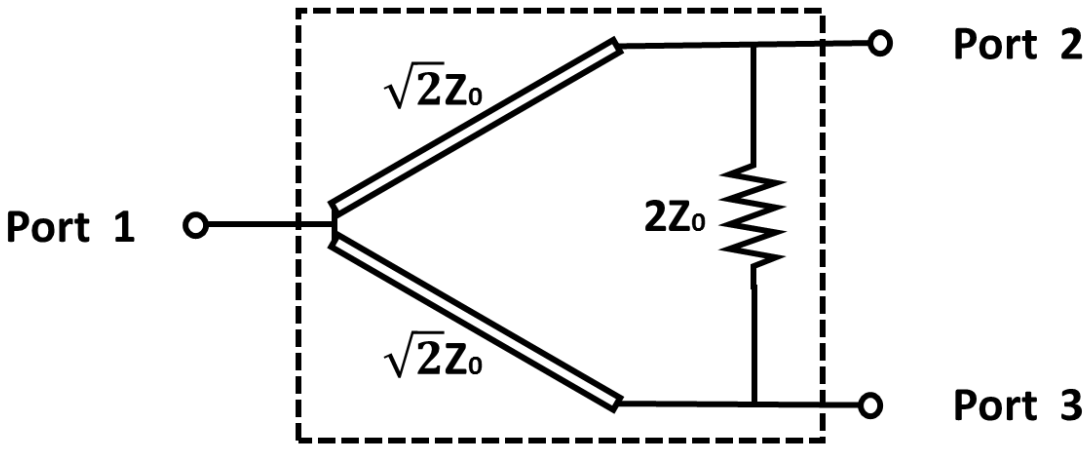

Figure 3.14. Wilkinson line power combiner.

straightforward way to understand how the isolation works is when inputs from port 2 and port 3 are not balanced, the unbalanced signal will be absorbed on the resistor Z_0 between the ports. Thus, the extra differential signals will not corrupt the operation of the PA unit which is at the input port of the Wilkinson line.

From an isolation perspective, the Wilkinson line works very well for the proposed HRPA topology. Wilkinson lines, however, have some limitations, one of which is that it only combines ports by power of two, so for the HRPA the input ports need to be at least four. This issue becomes more problematic when the input ports increase due to the design complexity and extra passive loss. Another limitation is the size for Wilkinson line depends on the operating frequency. In the RF frequency band, it takes a huge amount of chip area to fabricate a Wilkinson line.

3.3.2 *Non-isolated output power combiner: transformer*

A Non-isolated output power combiner is widely used in PA at RF frequency band due to the fact that less silicon area is required as compared to using a Wilkinson combiner and lower loss. These favorable properties relate to the fact that non-isolated power combiners do not provide a perfect isolation between different output ports. The loading condition needs to be carefully investigated. A transformer is a typical non-isolated output power combiner. Transformer based HRPA (Figure 3.15) has the fundamental drawback of poor isolation between the different PA driver output ports. For example, at the transformer primary side, due to the characteristic of HRPA operation, the phases at different input ports are not the same as would be the case in a classic power combining PA [9]. Take port P_1 and P_2 as an example, assuming they have a phase difference of θ. So the

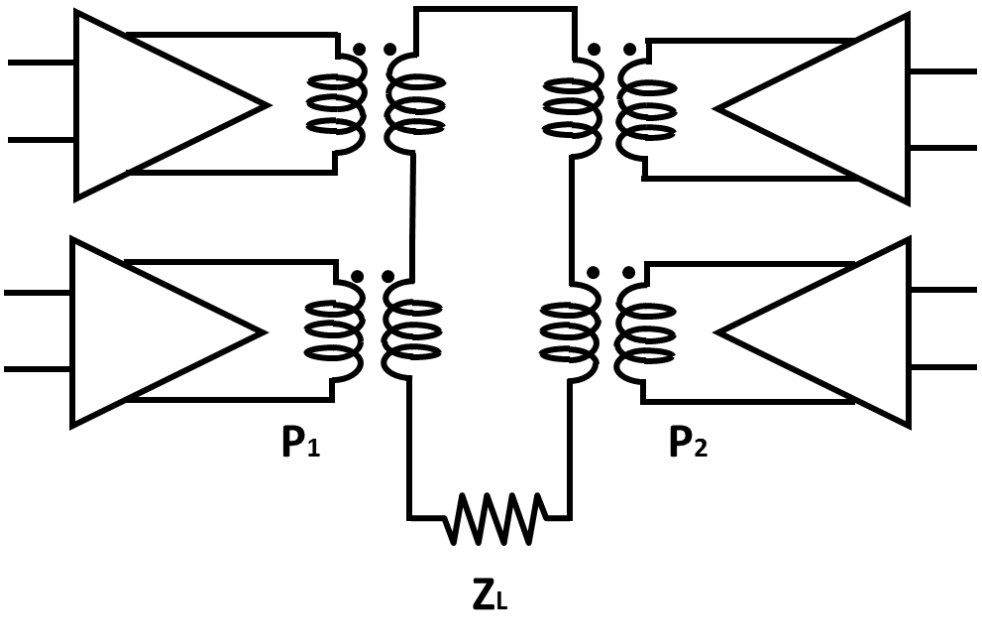

Figure 3.15. HRPA with transformer output power combiner.

signal on the primary side of P_1 will couple to the secondary and then generate a signal at the secondary side of P_2. This signal on the secondary side of P_2 will couple back to the primary side

of P_2 to degrade the signal on the primary side of P_2, and vice versa. This mutual loading condition can be analyzed using large signal analysis techniques:

Assuming the two PA units as ideal voltage sources (Figure 3.16(a)). The output signals are combined with an ideal transformer. Assuming the top and bottom PA unit (Figure 3.16(a)) generate output signals with the same frequency ω and magnitude V_m, but different phases (θ and -θ), the following describes the voltage at V_A and V_B [10].

$$V_A = V_m \sin(\omega_0 t + \theta) \tag{3.33}$$

$$V_B = V_m \sin(\omega_0 t - \theta) \tag{3.34}$$

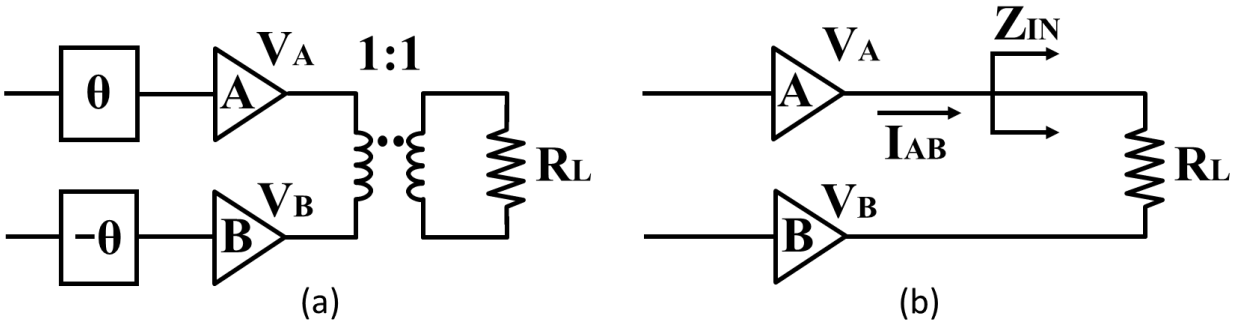

Figure 3.16. HRPA transformer output power combiner, (b) simplified model of power combiner loading on the drivers.

Assuming the transformer has a 1:1 turns ratio, the transformer can be seen as transforming the load from secondary to the combiner primary side. The mutual loading current for the top PA unit can be defined as:

$$I_{AB} = \frac{V_A - V_B}{R_L} \tag{3.35}$$

Plug (3.33) and (3.34) in (3.35), we can get:

$$I_{AB} = \frac{V_m \, sin(\omega_0 t + \theta) - V_m \, sin(\omega_0 t - \theta)}{R_L} \tag{3.36}$$

Expanding the sine term in the nominator, the expression for I_{AB} can be simplified to:

$$I_{AB} = \frac{2V_m \cos(\omega_0 t)\sin(\theta)}{R_L} \tag{3.37}$$

The input impedance can be calculated as:

$$Z_{in} = \frac{V_A}{I_{AB}} \tag{3.38}$$

Plug (3.33) and (3.37) into (3.38), we arrive at,

$$Z_{in} = \frac{V_m \sin(\omega_0 t + \theta)}{2V_m \cos(\omega_0 t)\sin(\theta)} R_L \tag{3.39}$$

Then expanding the sine term in the nominator:

$$Z_{in} = \frac{\sin(\omega_0 t)\cos(\theta) + \cos(\omega_0 t)\sin(\theta)}{2\cos(\omega_0 t)\sin(\theta)} R_L \tag{3.40}$$

Now, splitting the nominator gives:

$$Z_{in} = \frac{R_L}{2} + \frac{R_L \sin(\omega_0 t)}{2\cos(\omega_0 t)} \cot(\theta) \tag{3.41}$$

Since the numerator and denominator of the fraction in the second term are 90 degree out of phase, it introduces a –j in the equivalent impedance. Thus, the input impedance can be transformed to:

$$Z_{in} = \frac{R_L}{2} - j\cot(\theta)\frac{R_L}{2} \tag{3.42}$$

The input impedance from (3.42) shows that it is dependent on θ. For HRPA applications, when θ = 45 degree, the imaginary part will have the same magnitude as the real part. This imaginary part will have a huge effect on the output impedance of the PA.

This mutual loading effect can be alleviated using additional passives[11] to cancel out the second term in equation 3.42. Since the passive values will be dependent on the phase difference, and the phase difference will be changing according to different cancellation modes the PA has been set to. This almost means the circuit needs a capacitor bank with a wide tuning range and good resolution. This capacitor bank will greatly increase the chip area, design complexity and degrade the output power due to the finite qualify factor of the passive components, mainly the inductor.

Another problem with transformer is linearity of the PA output power as a function of the control code. The loading will change for different control codes and this will affect the PA output power if a non-constant envelope modulation is present at the PA input.

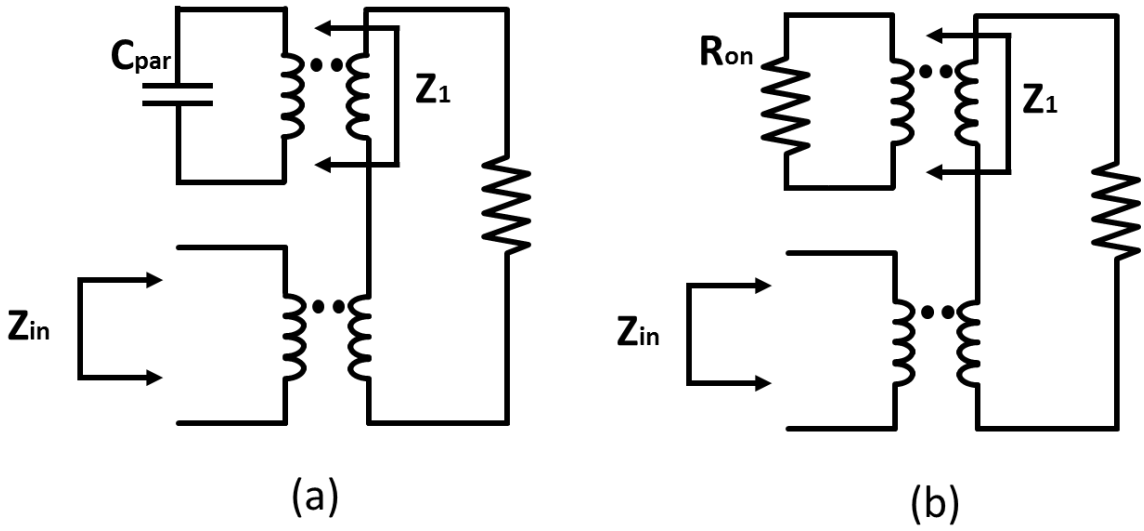

Figure 3.17. Input impedance when (a) PA unit is off, (b) PA unit is on.

Assuming L_1 is the inductance on the primary side and L_2 is the inductance on the secondary, R_L is the load impedance on the secondary side, and M is the mutual coupling coefficient, the input impedance looking into the primary of a transformer is:

$$Z_{in} = L_1 s - \frac{M^2 s^2}{R_L + L_2 s} \tag{3.43}$$

Assume M = L and $L_1 = L_2 = L$. When PA is at back-off mode, assuming the upper PA unit is idle, the load presents a parasitic capacitor, C. The output impedance looking into the upper PA unit from the secondary can be described by (Figure 3.17):

$$Z_1 = Ls - \frac{L^2 s^2}{\frac{1}{sC} + Ls} = \frac{Ls}{1 + LCs^2} \tag{3.44}$$

When the PA is at its maximum output mode, the load is R_{on}, so the impedance looking into the PA is:

$$Z_1 = \frac{R_{on} Ls}{R_{on} + Ls} \tag{3.45}$$

It is impossible to make the output impedance at (3.44) and (3.45) equal, therefore, the linearity performance will be affected when the power is backed-off because the load impedance is changing as a function of different control codes.

3.3.3 *Switch-Capacitor PAs*

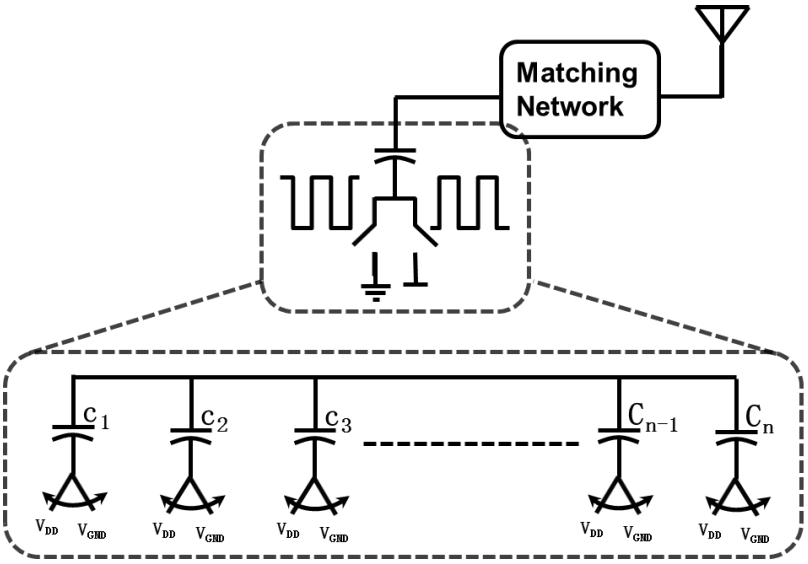

Figure 3.18. Block diagram for switch capacitor PA.

The SCPA topology benefits from CMOS scaling and has a better linearity and efficiency performance compared to other PA approaches[12]. In an SCPA, each Class-D PA unit generates an output signal that toggles between V_{DD} and ground. The capacitors realize the output matching network and fulfil the role as a power combiner. SCPA has many advantages for HRPA design, and the details will be elaborated in the following section.

3.4 SWITCH-CAPACITOR HRPA ANALYSIS

3.4.1 *Large signal analysis of mutual loading effects*

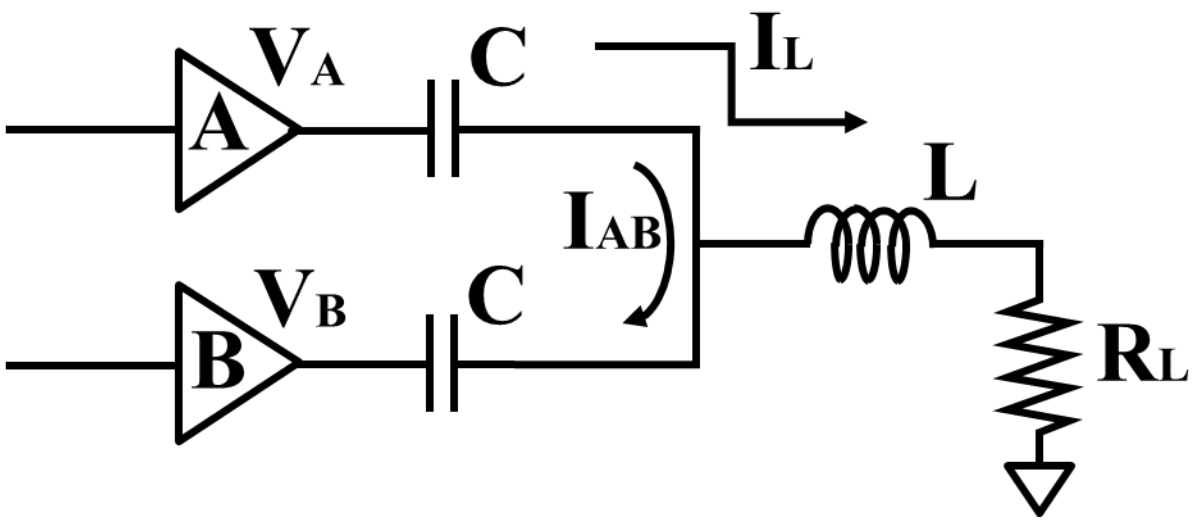

Figure 3.19. HRPA mutual loading model for SCPA.

These capacitors have the added advantage of improving the isolation between the driver stages, thus minimizing the effect of a time-varying load impedance. It can be proven with the same analytical method used in Section 3.3.2.

The model (Figure 3.19) assumes each PA is a voltage source and generates V_A and V_B with same amplitude V_m and frequency ω, but with a different phase (θ and -θ).

$$V_A = V_m \sin(\omega_0 t + \theta) \tag{3.46}$$

$$V_B = V_m \sin(\omega_0 t - \theta) \tag{3.47}$$

Using superposition, the input current of the top PA cell contains two components, I_{AB} which is the mutual loading current and I_L which is the current that flows to the load,

$$I_A = I_{AB} + I_L \tag{3.48}$$

Use large signal analysis, we can get I_{AB} and I_L as:

$$I_{AB} = \frac{V_A - V_B}{\frac{1}{j\omega C} + \frac{1}{j\omega C}} \tag{3.49}$$

$$I_L = \frac{V_A}{\frac{1}{j\omega C} + j\omega L + R_L} \tag{3.50}$$

The input impedance of the top PA unit can be calculated by:

$$Z_{in} = \frac{V_A}{I_A} \tag{3.51}$$

Plug 3.48 in 3.51, we can get

$$Z_{in} = \frac{V_A}{I_{AB} + I_L} \tag{3.52}$$

Plug 3.49, and 3.50 in 3.52, the input impedance is:

$$Z_{in} = \frac{V_A}{\frac{V_A - V_B}{\frac{1}{j\omega C} + \frac{1}{j\omega C}} + \frac{V_A}{\frac{1}{j\omega C} + j\omega L + R_L}} \tag{3.53}$$

Simplified the denominator,

$$Z_{in} = \frac{V_A}{\frac{j\omega C}{2}(V_A - V_B) + \frac{V_A}{\frac{1}{j\omega C} + j\omega L + R_L}} \tag{3.54}$$

Cancelling V_A in the nominator and denominator, results in,

$$Z_{in} = \frac{1}{\frac{j\omega C}{2}\left(\frac{V_m \sin(\omega_0 t + \theta) - V_m \sin(\omega_0 t - \theta)}{V_m \sin(\omega_0 t + \theta)}\right) + \frac{1}{\frac{1}{j\omega C} + j\omega L + R_L}} \tag{3.55}$$

V_m drops out of the first term in the denominator which gives,

$$Z_{in} = \frac{1}{\frac{j\omega C}{2}\left(\frac{\sin(\omega_0 t + \theta) - \sin(\omega_0 t - \theta)}{\sin(\omega_0 t + \theta)}\right) + \frac{1}{\frac{1}{j\omega C} + j\omega L + R_L}} \tag{3.56}$$

Expanding the sine term in both the nominator and denominator results in,

$$Z_{in} = \frac{1}{j\omega C \frac{\sin(\omega_0 t)\cos(\theta)}{\sin(\omega_0 t)\cos(\theta) + \cos(\omega_0 t)\sin(\theta)} + \frac{1}{\frac{1}{j\omega C} + j\omega L + R_L}} \tag{3.57}$$

Dividing the nominator and denominator by the first term of the denominator gives,

$$Z_{in} = \frac{1}{j\omega C \dfrac{1}{1 + \dfrac{\cos(\omega_0 t)\sin(\theta)}{\sin(\omega_0 t)\cos(\theta)}} + \dfrac{1}{\dfrac{1}{j\omega C} + j\omega L + R_L}} \tag{3.58}$$

Since the numerator and denominator of the fraction in the first term of the denominator are 90 degrees out of phase, this will introduce a complex component "j" in the equivalent impedance. Thus, the input impedance can be transformed to:

$$Z_{in} = \frac{1}{j\omega C \dfrac{1}{1 + j\tan(\theta)} + \dfrac{1}{\dfrac{1}{j\omega C} + j\omega L + R_L}} \tag{3.59}$$

Simplifying the first term of the denominator gives,

$$Z_{in} = \frac{1}{j\omega C \dfrac{1 - jtan(\theta)}{1 + \tan^2(\theta)} + \dfrac{1}{\dfrac{1}{j\omega C} + j\omega L + R_L}} \tag{3.60}$$

Moving the denominator of the first term to nominator gives,

$$Z_{in} = \frac{1}{j\omega C(1 - jtan(\theta))\cos^2(\theta) + \dfrac{1}{\dfrac{1}{j\omega C} + j\omega L + R_L}} \tag{3.61}$$

If it is assumed that L is resonating with the total C, the equivalent impedance will be L',

$$Z_{in} = \frac{1}{j\omega C(1 - jtan(\theta))\cos^2(\theta) + \frac{R_L - j\omega L'}{(\omega L')^2 + {R_L}^2}} \tag{3.62}$$

If the real part and imaginary part are combined together,

$$Z_{in} = \frac{1}{\frac{R_L}{(\omega L')^2 + {R_L}^2} + \omega C sin(\theta)\cos(\theta) - j(\frac{\omega L'}{(\omega L')^2 + {R_L}^2} + \omega C\cos^2(\theta))} \tag{3.63}$$

The mutual loading will create two components both a real and imaginary part impedance. These two parts are all proportional to the value of C. The imaginary impedance component, at the frequency of interest, is dominated by the value of Capacitor, C. Thus, a smaller C will significantly reduce the effective capacitance introduced by the driver time-varying output impedance. This is intuitively pleasing as generally, smaller capacitors present a larger series impedance.

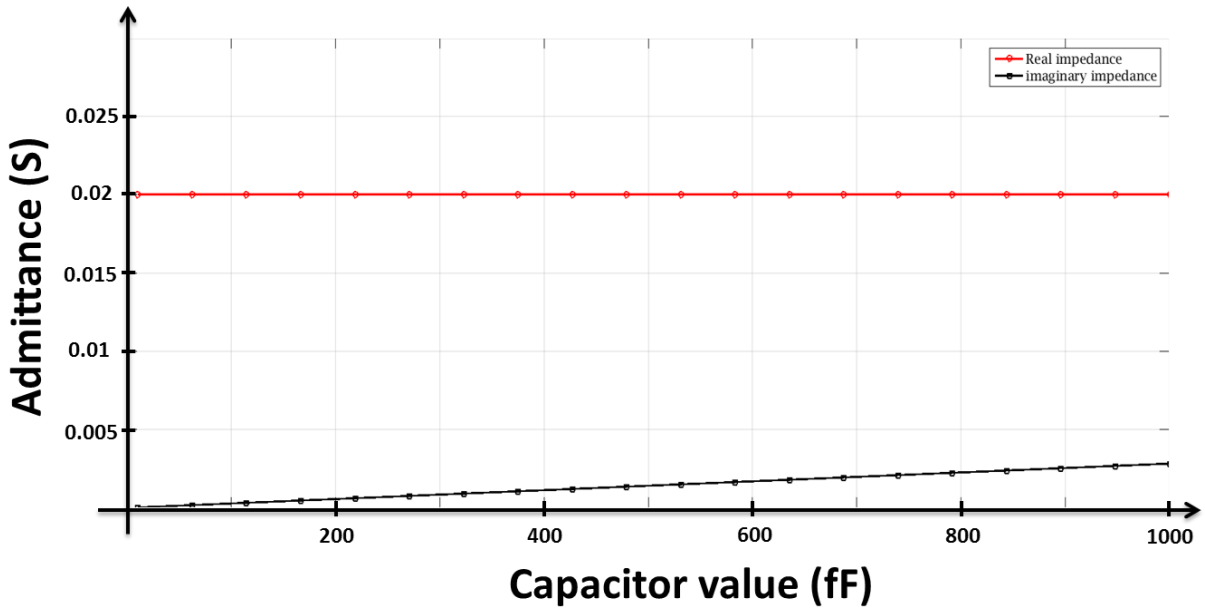

Figure 3.20. Impedance comparison.

3.4.2 *Isolation under power back-off*

The SCPA has a good linearity to perform amplification of non-constant envelope modulated signals. A simplified model (Figure 3.21) assumes the top PA unit is idle and the middle PA unit

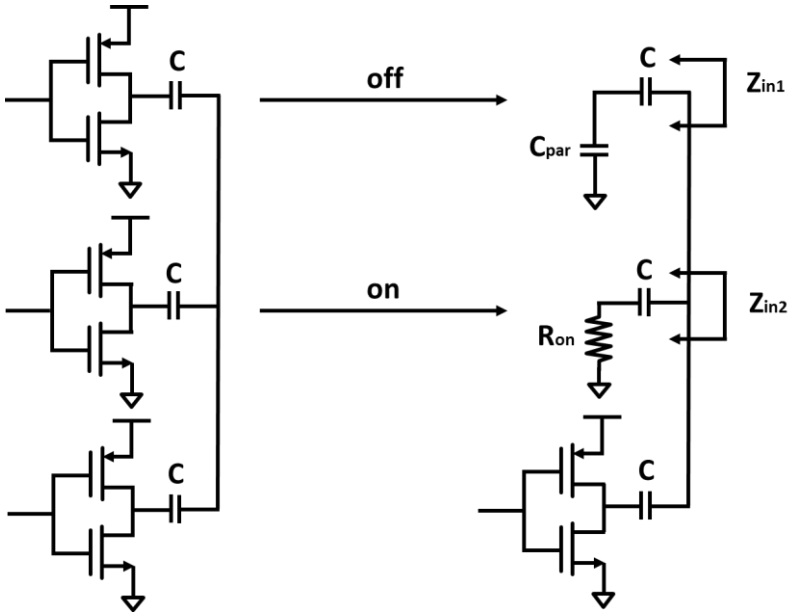

Figure 3.21. SCPA power back-off model.

is on. The output impedance Z_{in1} for the top PA unit has two capacitors C and C_{par} in series, and the output impedance Z_{in2} for the middle PA unit is C and R_{on} in series. Thus, if a small capacitor C is chosen, Z_{in1} and Z_{in2} will roughly be the same. So the output matching network for the SCPA under power back-off will be identical to matching network when the PA is operated at its peak output power. Assuming each PA unit generates an identical power output, the output power of the SCPA will be proportional to the number of stages turning on, making the SCPA very linearly related to the control codes.

3.4.3 *HRPA vs. Filter*

The primary benefit of using this harmonic-reject power amplifier approach is the possibility of eliminating the need for any front-end filter or discrete-component harmonic trap at the transmitter output. However, there are issues with respect to utilizing the HRPA technique, mainly the output power of SC-HRPA will drop after harmonic rejection is enabled. Although the output power and efficiency performance maybe degraded, there is likely a net efficiency win because the HRPA will eliminate the need for an external filter (or trap), the removing the insertion loss of a filter.

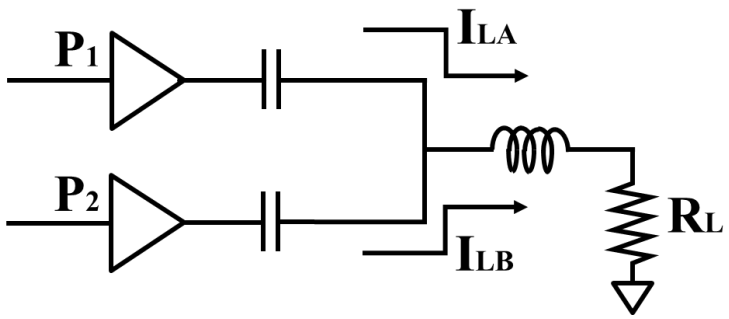

Figure 3.22. Traditional SCPA current flow without a harmonic rejection function.

Figure 3.22 shows the current flow when P_1 and P_2 are in phase and on at the same time. P_1 and P_2 are delivering I_{LA} and I_{LB} separately to the load, and drawing I_{LA} and I_{LB} from the power supply at the same time (assuming no power loss from the switch).

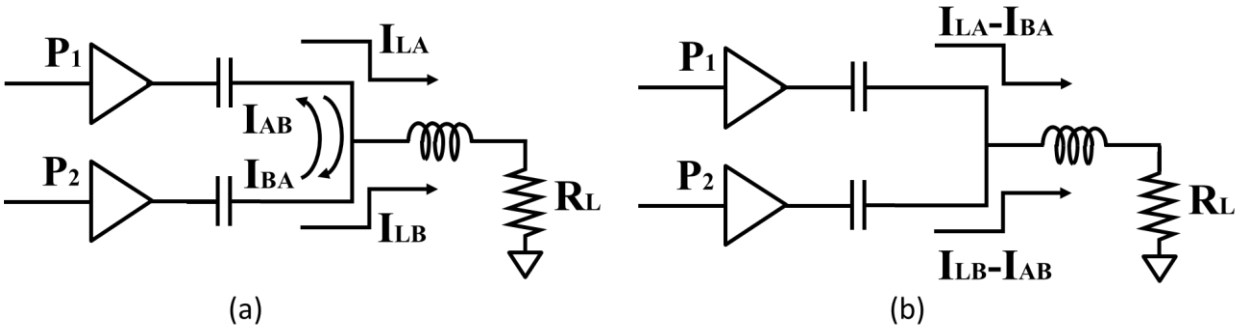

Figure 3.23. SCPA current flow with harmonic rejection, (a) before superposition, (b) after superposition.

When the SCPA is configured to realize a harmonic rejection function, P_1 and P_2 will be switch on and off at different times, therefore generating a mutual load current I_{AB} and I_{BA}. This is attributed to the fact that the load is purely passive, allowing the use of the superposition principle. Using superposition is equivalent to P_1 and P_2 delivering I_{LA}-L_{BA} and I_{LB}-I_{AB}, separately to the load. Still assuming the PA does not have power loss, so ideally P_1 and P_2 are only drawing I_{LA}-I_{BA} and I_{LB}-I_{AB} from the load. To sum up, after harmonic rejection is implemented, the PA is delivering less current to the load, but at the same time drawing less current from the power supply. If the original efficiency for the PA is 100%, the HRPA sees 0% efficiency drop.

A transmitter which uses a filter to eliminate harmonics at the output, the efficiency and output power scenario is quite different, if the filter has YdB insertion loss, the PA output power will drop YdB, however the PA is still drawing same amount of power from the power supply, so the insertion loss will directly hurt the PA efficiency.

The efficiency drop of the SC-HRPA after harmonic rejection is implemented can be calculated as follows, assuming the PA originally has an efficiency of X, and the power deliver to the load is Pout, so the power draw from the power supply is:

$$P_{total} = \frac{P_{out}}{X} \tag{3.64}$$

The amount of the output power drops after harmonic rejection is enabled depends on the phase and gain ratio on each of the individual paths. Here assuming a phase shift of Φ°/0/- Φ° and a gain ratio of 1/A/1 is applied, the P'_{out} after harmonic rejection will be:

$$P'_{out} = P_{out}(\frac{2\cos(\Phi) + A}{2 + A})^2 \tag{3.65}$$

The efficiency for the whole HRPA system after plugging 3.64 and 3.65 will be:

$$PAE = \frac{P'_{out}}{P'_{totoal}} = \frac{P'_{out}}{P_{total} - (P_{out} - P'_{out})} = \frac{P_{out}(\frac{2\cos(\Phi) + A}{2 + A})^2}{\frac{P_{out}}{X} - (P_{out} - P_{out}(\frac{2\cos(\Phi) + A}{2 + A})^2)} \tag{3.66}$$

P_{out} can be cancelled here, so the system efficiency is only dependent on Φ, A and the original PA efficiency.

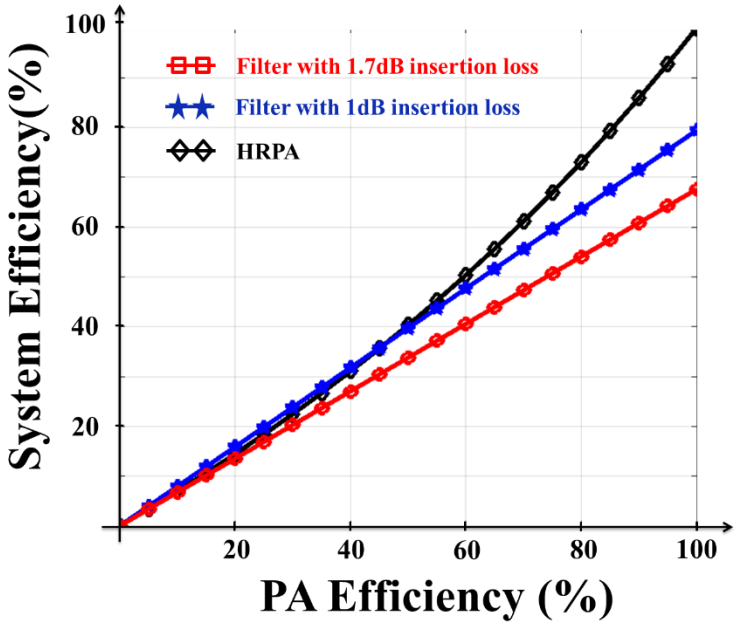

Figure 3.24. PAE of HRPA vs. Filter.

$$PAE = \frac{(\frac{2\cos(\Phi) + A}{2 + A})^2}{\frac{1}{X} - (1 - (\frac{2\cos(\Phi) + A}{2 + A})^2)} \tag{3.67}$$

If choosing Φ=64, and A=1.23, the efficiency of the HRPA and the filter-based PA system is shown in Figure 3.24. So when the PA original efficiency is high, the HRPA has a superior advantage over a filter based PA system.

Chapter 4. HRPA IMPLEMENTATION

4.1 TOP LEVEL CIRCUIT DIAGRAM

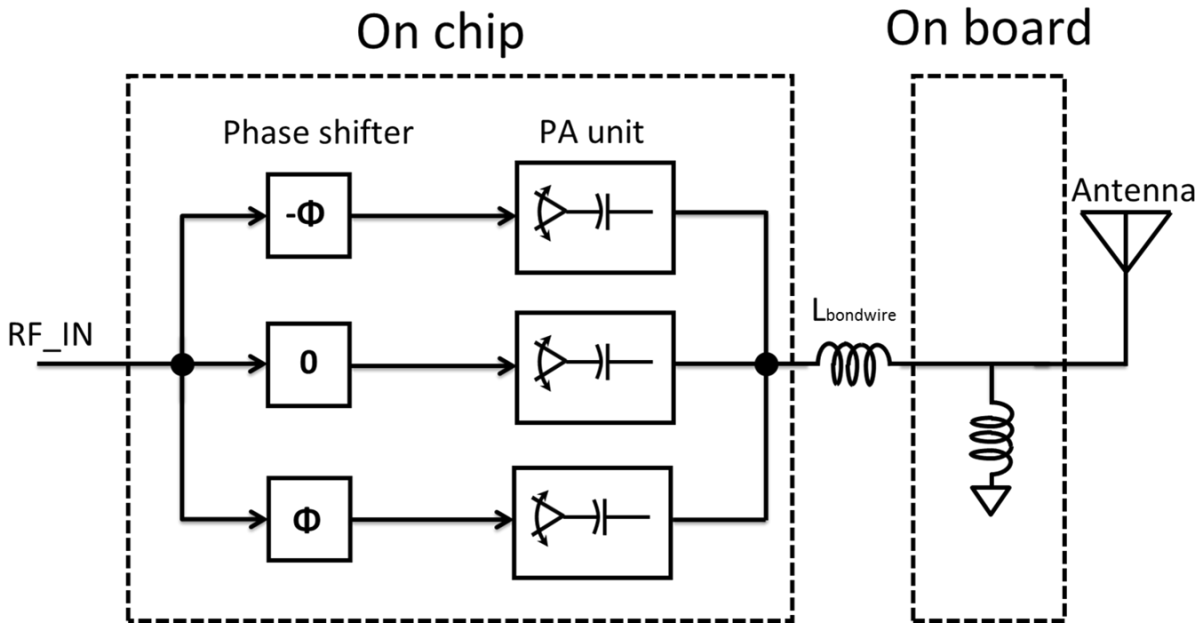

Figure 4.1. HRPA top level circuit diagram.

The HRPA chip integrates the phase-shifters, pre-drivers and PA output drivers. The phase shifter is embedded with the PA pre-driver stage to minimize the power consumption and area. Both the coarse and fine phase tuning are realized based on RC inverter delay while coarse tuning is

achieved by adjusting R, and fine tuning is done by adjusting C. The design of the PA output driver is a Class-D output stage as in[12]. A single discrete inductor is used with a bond-wire to form an L-match network (Fig. 4.1).

4.1.1 *Phase shifter*

The proposed HRPA requires a phase shifter to rotate the input signal in RF domain. The HRPA system requires the phase shifter to have the following two functions. First, the ability to do coarse

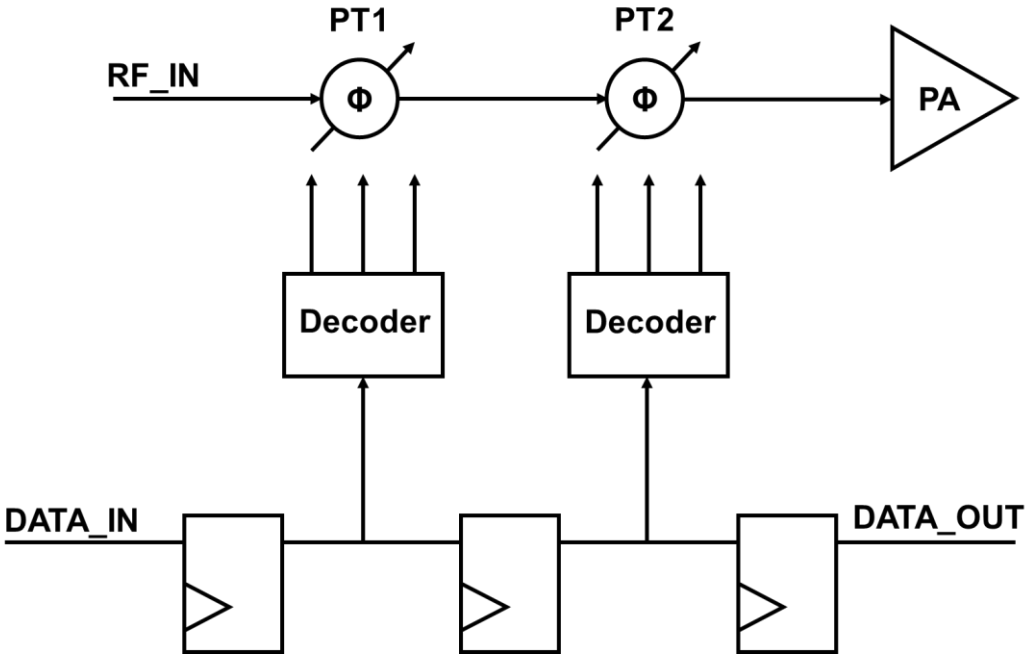

Figure 4.2. Phase shifter top-level diagram.

tuning. So the phase delay on three paths needs to tune from 0/0/0 to 0/64/128 degrees to achieve $2^{nd}/3^{rd}/4^{th}$ order harmonic rejection, respectively. Second, the phase shifter needs to have fine tuning ability with a good resolution to compensate for any mismatch between the three paths. In addition, there is the additional desire to minimize the area and overall complexity the phase shifter introduces to the whole PA.

A phase tuning structure (Figure 4.2) is proposed here. PT1 is the phase shifter for coarse tuning and PT2 is the phase shifter for fine tuning. They are both digitally controlled. The control bits are

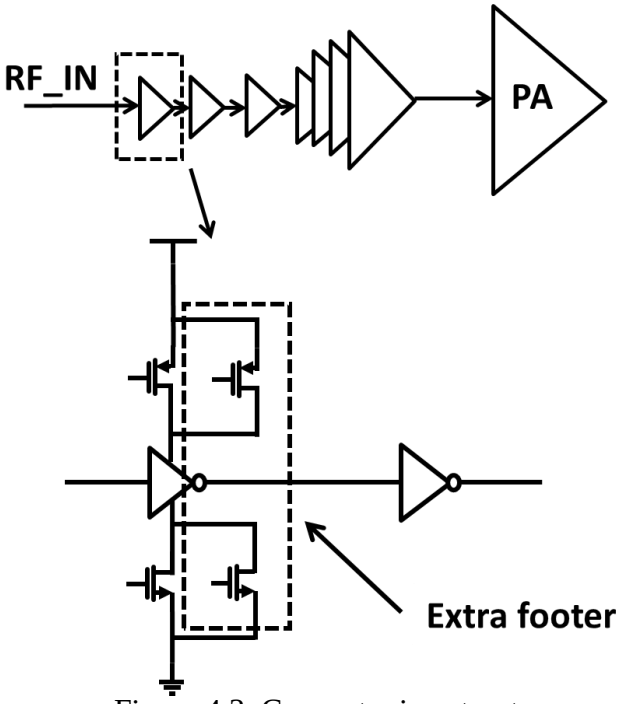

Figure 4.3. Coarse tuning structure.

scanned in with a scan chain and later decoded with two binary-to-thermal decoders to control two phase shifters separately. The output of the phase shifter feeds into each of the PA drivers. The proposed phase shifter structure will integrate the phase shift function into the pre-driver to save the chip area.

Since the job for coarse tuning is to adjust the phase to $2^{nd}/3^{rd}/4^{th}$ cancellation mode, the coarse tuning does not need to be very linear. The only requirement is to tune to the specific degree to achieve cancellation, which is 64/128 degree in this case. The proposed structure uses footer transistor (Figure 4.3) to generate the coarse delay. The coarse tuning is put at the beginning of the driver because of the desire to keep the size of the transistors small in the early stages of the pre-driver. So less chip area is needed to achieve the same tuning range as compared to using footers for latter stage.

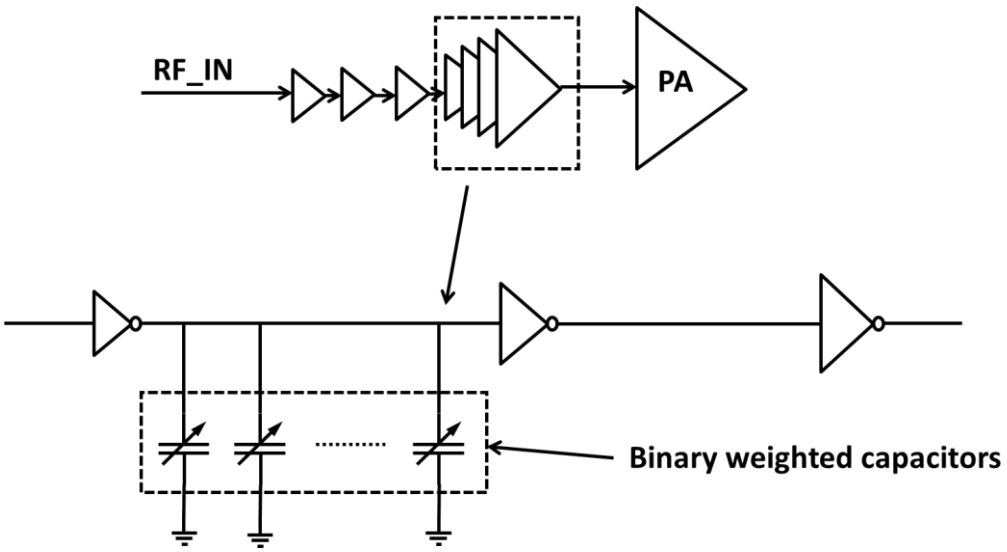

Figure 4.4. Fine phase tuning circuit topology.

Fine tuning of the phase needs to have a good INL and DNL performance. As such, the good matching properties associated with tuning via a capacitor array is chosen here to provide a fine adjust the phase between the difference signal paths. A fine resolution can be achieved by putting the fine tuning stage at the latter stage of the driver. The resolution can be roughly defined as the ratio of the capacitor in the capacitor banks to the input capacitance of the next driver stage. Therefore, later stage transistors have larger size so the resolution is better. The capacitor bank is implemented with the gate capacitance of MOSFET to decrease the chip area and provide better matching.

4.1.2 *Output matching network*

To deliver a higher output power, the output matching network needs to transform the output impedance to a smaller value. L matching network is a simple and effective method to realize

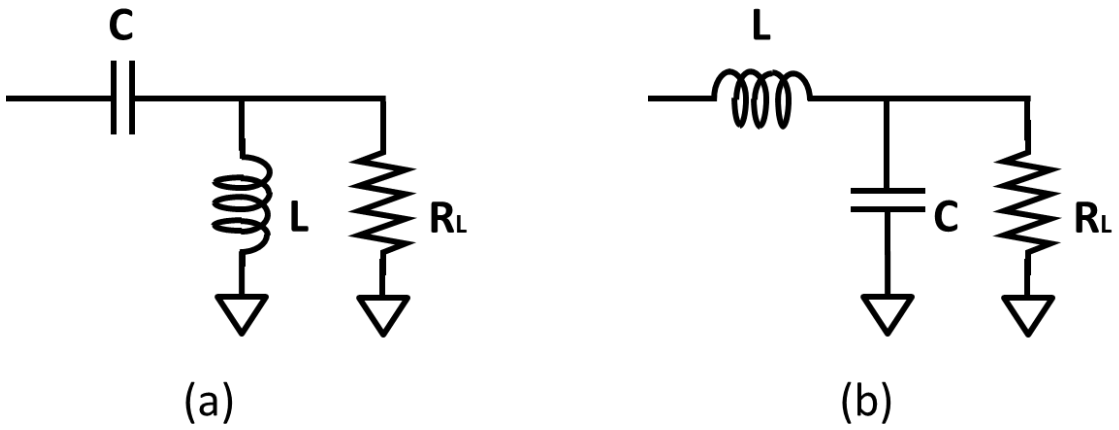

Figure 4.5. Types of L matching networks.

impedance transformation. There are four types of L matching networks, and two of them (Figure 4.5) have the ability to transform the output impedance to a smaller value.

The matching network is added on board. Before the matching network, the PA first sees an output capacitor and a bond-wire inductor. The capacitor and the bond-wire inductor can be used as part of the L matching network to reduce the number of the extra off-chip components. The capacitor value is selected to be a 100fF to improve the isolation and linearity performance as analyzed before. The value of the bond-wire inductor is determined by the length of the bond-wire, which can be roughly estimated as 1nH/mm. Thus, there are now two options to realizing the match, a large bond-wire inductor could be used to form L matching network (Figure 4.5(b)), or selecting a small bond-wire inductor to create L matching network (Figure 4.5(a)).

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{4.68}$$

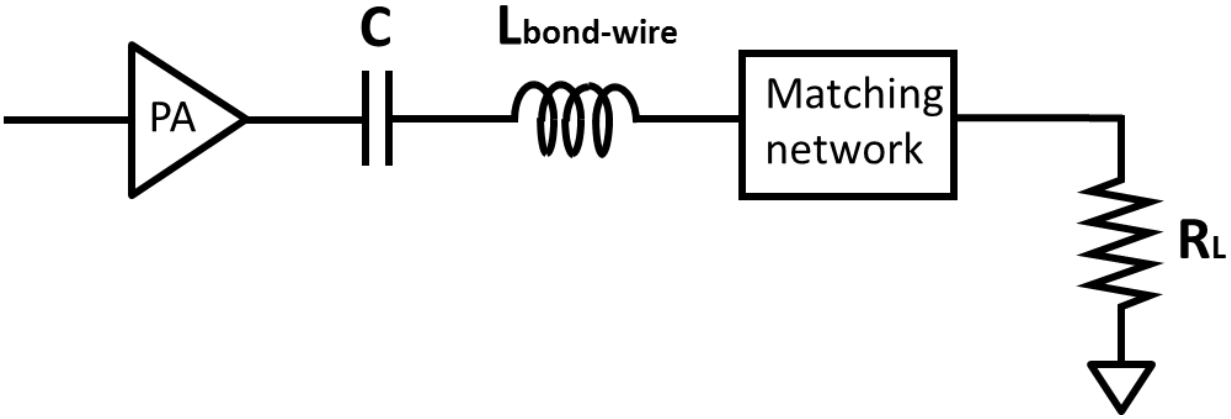

Figure 4.7. HRPA matching network

To resonate out the output capacitor (100f*41 = 4.1p) at 915MHz the inductor value will be 7.6nH.

The 7.6nH is comprised of the bond-wire inductance and the extra load inductance.

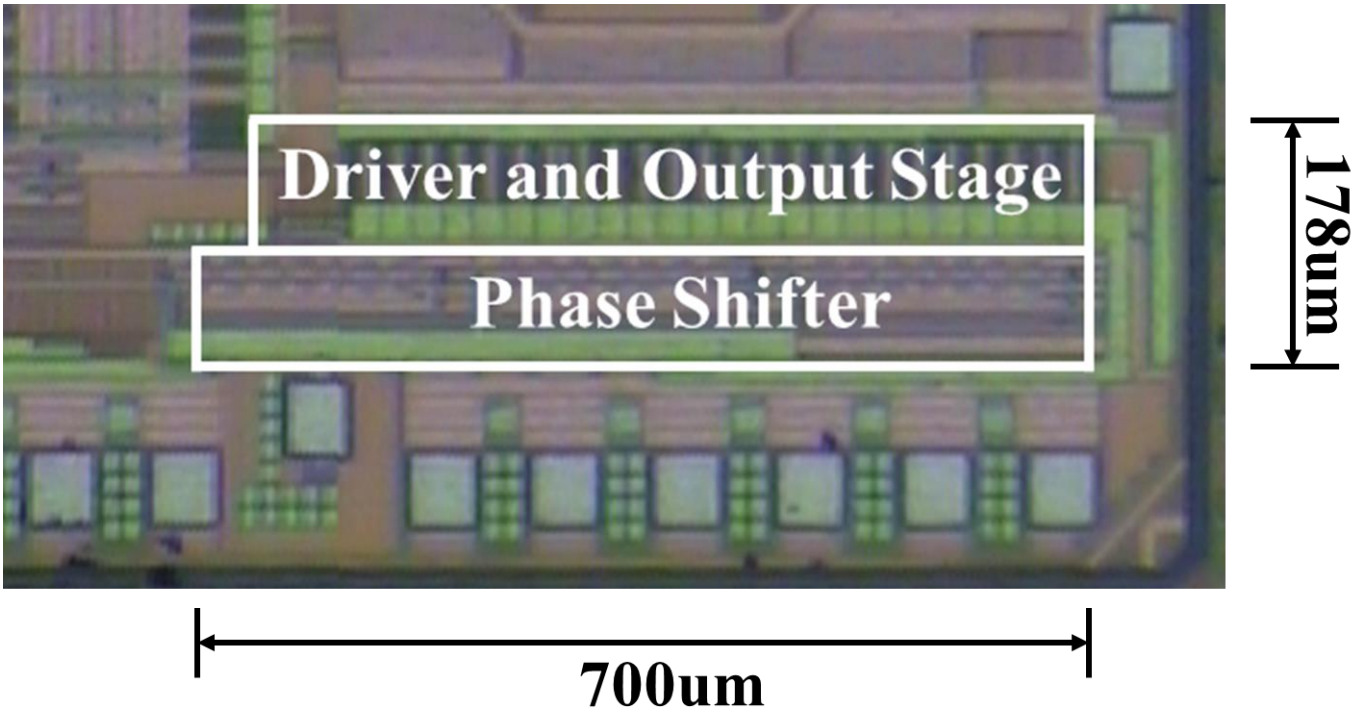

Figure 4.6. HRPA die photo.

4.1.3 *HRPA Die Photo*

The proposed PA was fabricated in a 40 nm 6-metal-layer TSMC CMOS process, and occupies 178 um×700um active area. The die photo is shown in **Error! Reference source not found.**. The die is wire-bonded directly to the test-board using chip-on-board packaging.

Chapter 5. RESULT

5.1 MEASUREMENT SETUP

5.1.1 *Test board Design*

A test board was fabricated to test the functionality for the proposed single-end HRPA. The HRPA has three I/O interfaces, RF input, RF output and digital control input. The RF input of the chip was connected to an SMA connector via 50Ω on-board transmission line. The RF output of the chip was first attached to an on-board matching network, and then connected to the SMA connector via 50Ω on-board transmission line. The matching network was put as close to the chip as possible

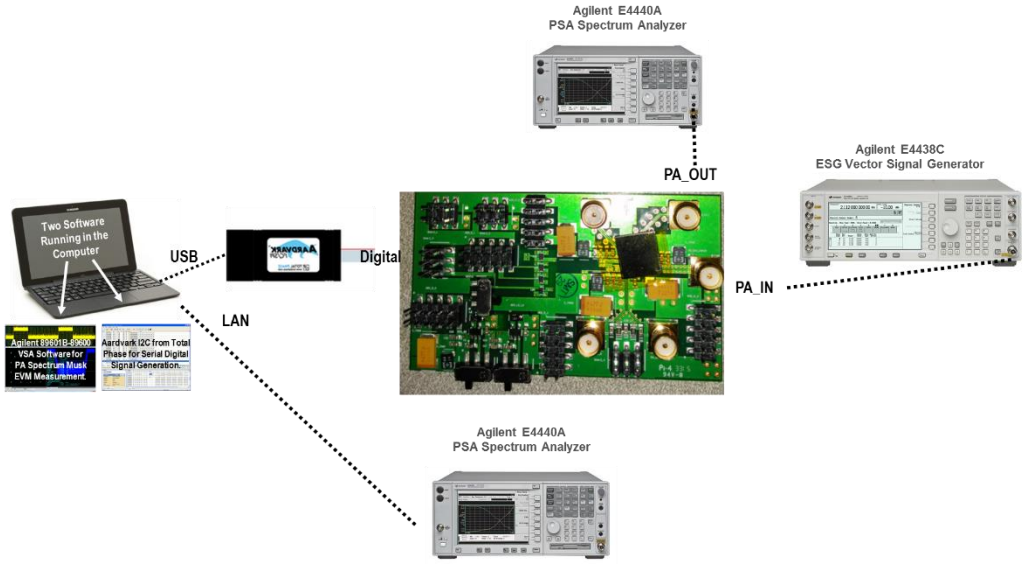

Figure 5.1. In lab HRPA testbench.

to eliminate the mismatch between the output of the chip to the matching network. An Aardvark serial IO writer (Total Phase, Inc.) is used to provide digital input to the shift register on-chip. The board was manufactured in a four-layer board design with a signal/V_{dd}/ground/signal layers. Arrays of by-pass capacitors are put as close to the chip as possible to provide decoupling. Ground and power planes for the PA are made as wide as possible and with similar shape. Vias were put near the on-board transmission line to provide a good ground connection. The RF input of the PA was provided by an Agilent ESG Vector Signal Generator (E4438C), and the output spectrum was measured with Agilent PSA Spectrum Analyzer (E4440A).

5.2 MEASUREMENT RESULTS

5.2.1 *Phase shifter*

The HRPA has three different paths, and each path has its own phase tuning. The performance of the phase shifter on each path was measured when the other two were turned off. The output of

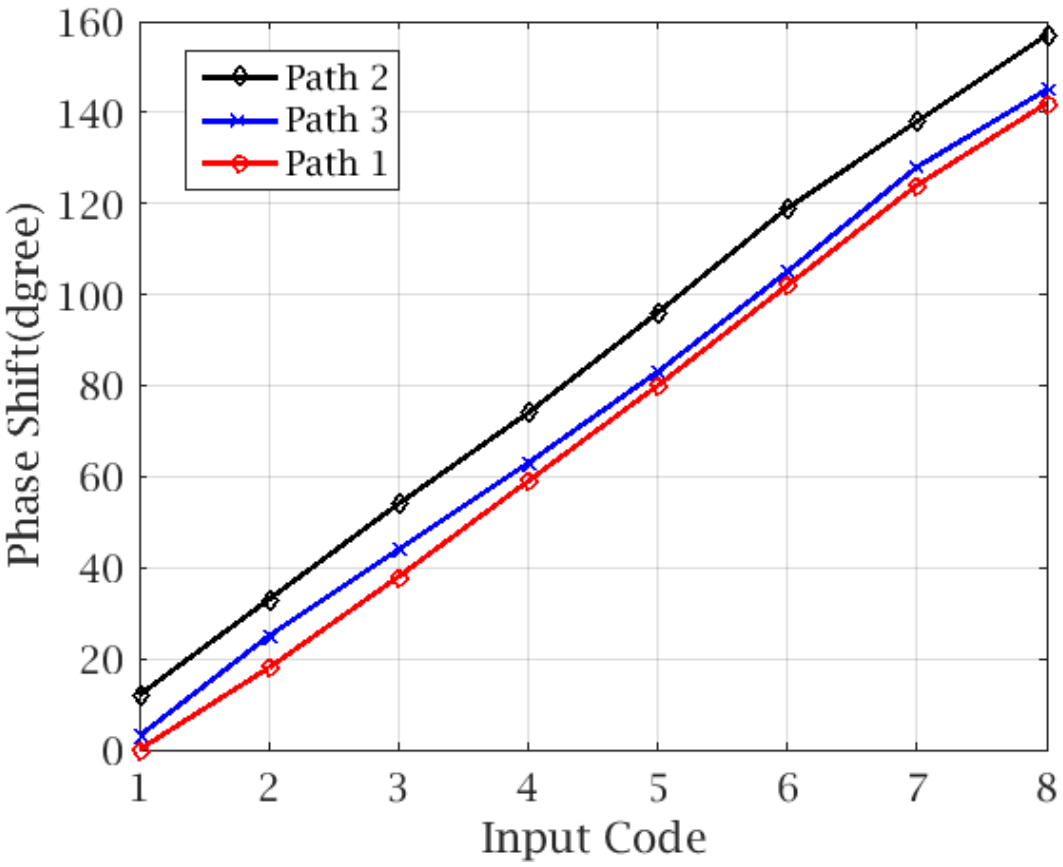

Figure 5.2. Coarse tuning performance. Output phase relationship vs. tuning code.

the PA was fed into Agilent digital storage oscilloscope (DSO-X 92504A) to show the phase information of the PA output. By varying the input control bits, the phase difference can be read on the oscilloscope. The coarse tuning is controlled by three digital bits, coarse tuning range for the phase shifter is shown in Figure 5.2. Both paths 1 and 3 deliver the same output power and are represented with red and blue color, respectively. Path 2 delivers 1.23 times output power relative to paths 1 and 3, and the tuning range for path 2 is represented with black color line. The tuning

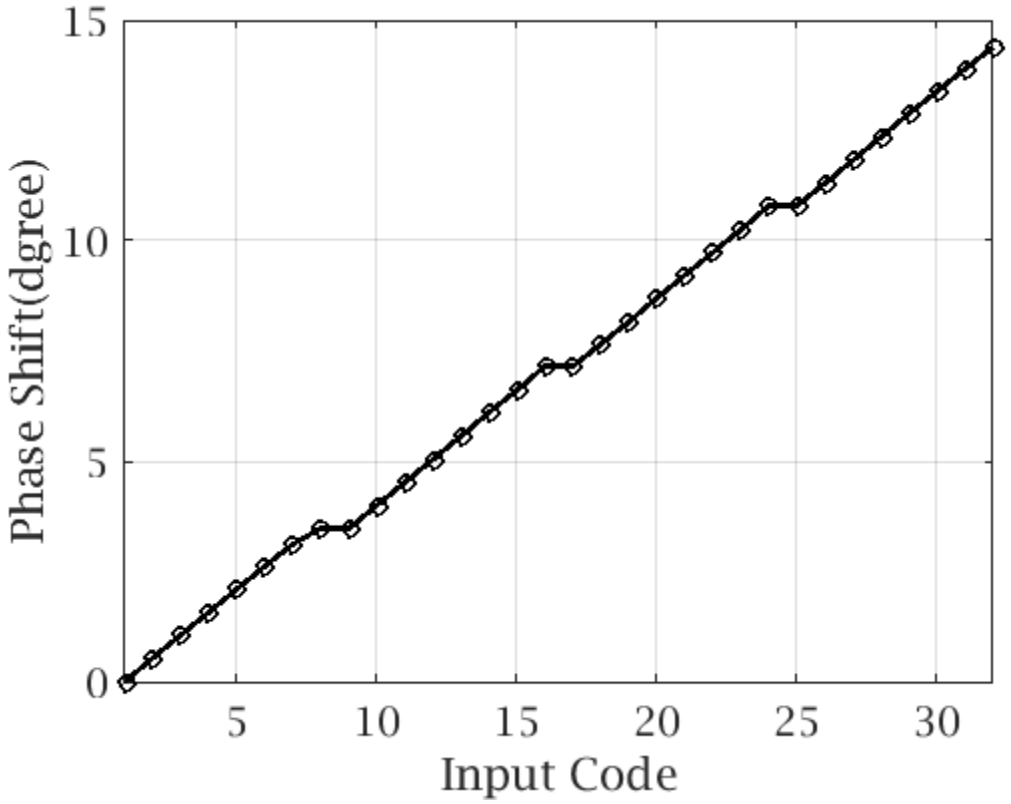

Figure 5.3. Fine tuning performance.

range for the three paths are 142, 145, 142 degrees, as such they are almost identical. This tuning range is wide enough to achieve good $2^{nd}/3^{rd}/4^{th}$ harmonic cancellation performance. The phase shifter for both path 1 and path 3 drives 12 PA unit cells and path 2 drives a 15 PA unit cell. The loading capacitance varies depending on the driver stage, and thus this will generate a phase difference between paths 1 and 2 of approximately 12-15 degrees. Any phase difference between paths 1 and 3 are purely attributed to layout mismatch.

The fine tuning performance (Figure 5.3) shows that there are total 32 input codes corresponding to roughly a 14 degree phase shift. Some codes generate the same phase shift due to the dead zone of the binary to thermal decoder.

5.2.2 *Output power, efficiency and linearity of the HRPA*

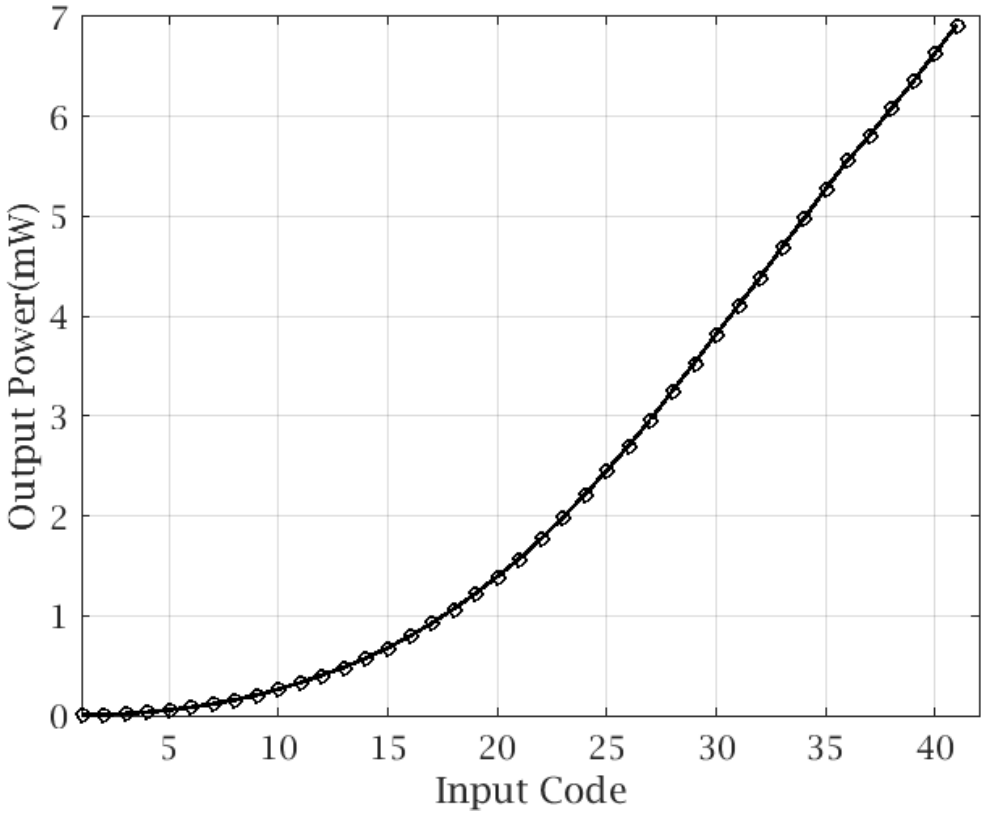

Figure 5.4. Output power of SCPA corresponding to input code.

The analysis given in Section 3.4 shows the output power of the SCPA has a linear relationship with the input codes due to the fact that the loading condition does not change as the PA goes into the power back-off mode. This can be proven by Figure 5.4., where the output power is larger than 1mW, and the output power becomes very linear with the input codes. The output power is not very linear as the input code is made smaller. This is mainly caused by the comparatively large R_{on} of the switch. When more cells are turned on, the effect of the impact on R_{on} become less. The center frequency for this PA is 970MHz and the peak output power is 8.9dBm with a peak drain efficiency 43.6 %(Figure 5.6). The output power of the PA increases by raising the supply voltage. The peak drain efficiency of 47.7% is achieved with a supply voltage of 1.1V (Figure 5.5).

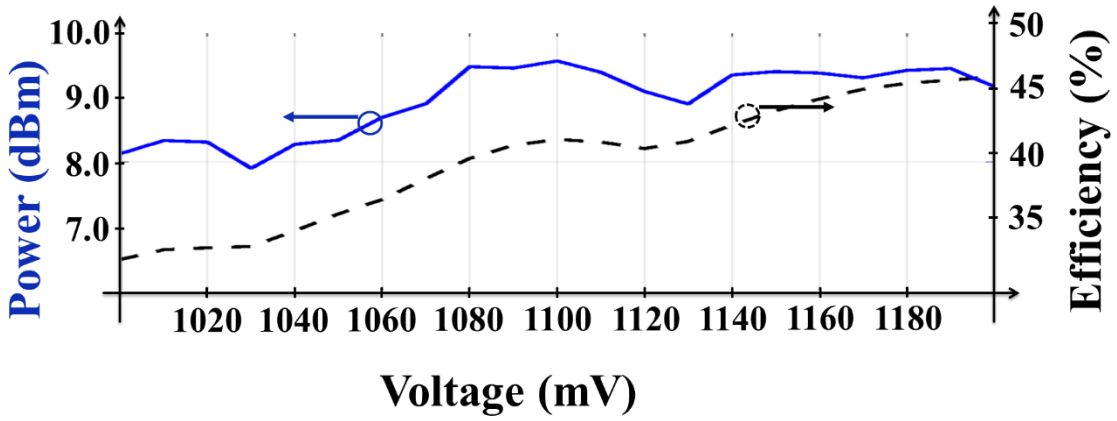

Figure 5.5. SCPA output power and drain efficiency with different supply voltages.

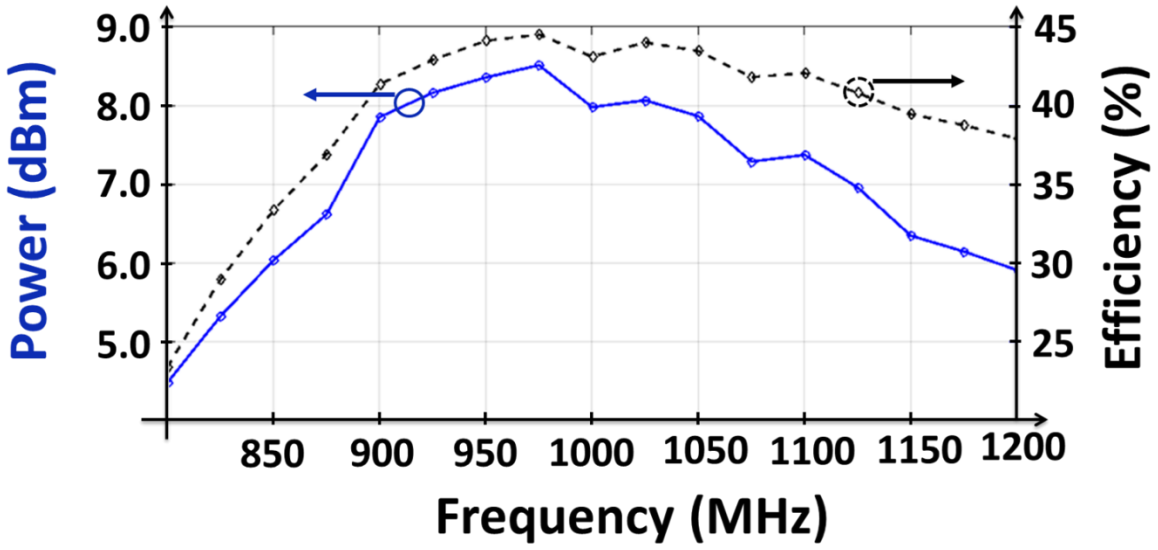

Figure 5.6. Output power and drain efficiency of SCPA at different frequencies.

5.2.3 *Harmonic cancellation performance*

The harmonic rejection PA achieves 48dB, 17dB, and 24dB cancellation on $2^{nd}/3^{rd}/4^{th}$ harmonics respectively. The $2^{nd}/3^{rd}/4^{th}$ harmonics after cancellation is -60/-39/-37 dBm and -65/-44/-42 dBc. The fundamental power drops around 2dB (Figure 5.7). The proposed HRPA is able to provide more than 20dB cancellation over 35MHz frequency band, with the second order harmonic being

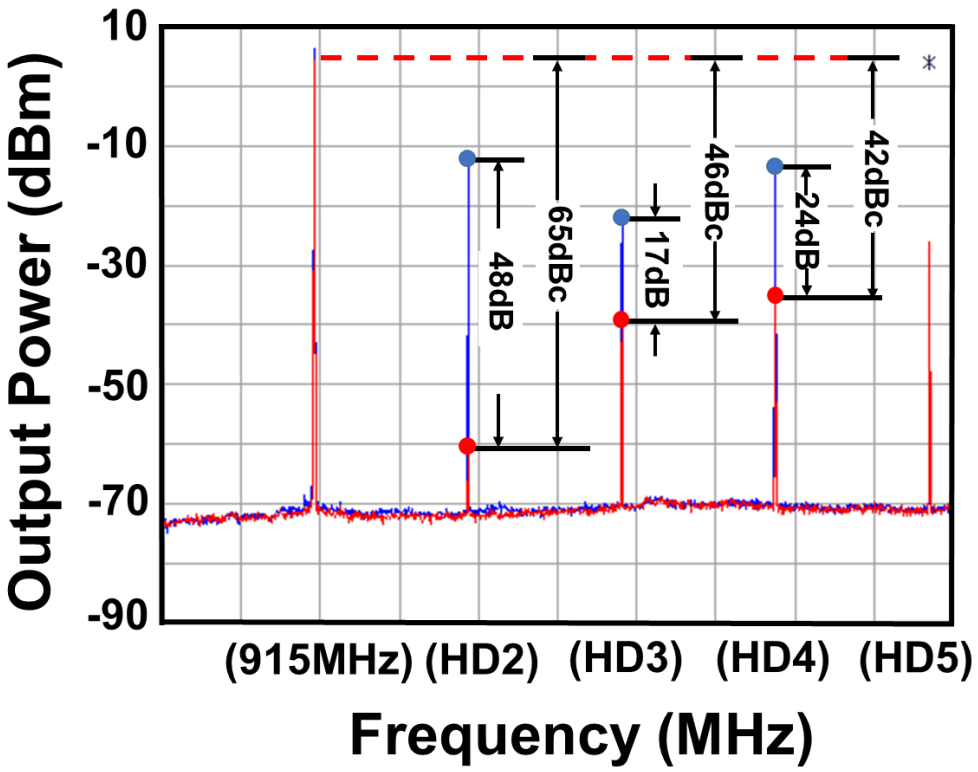

Figure 5.8. Transmit spurious output spectrum.

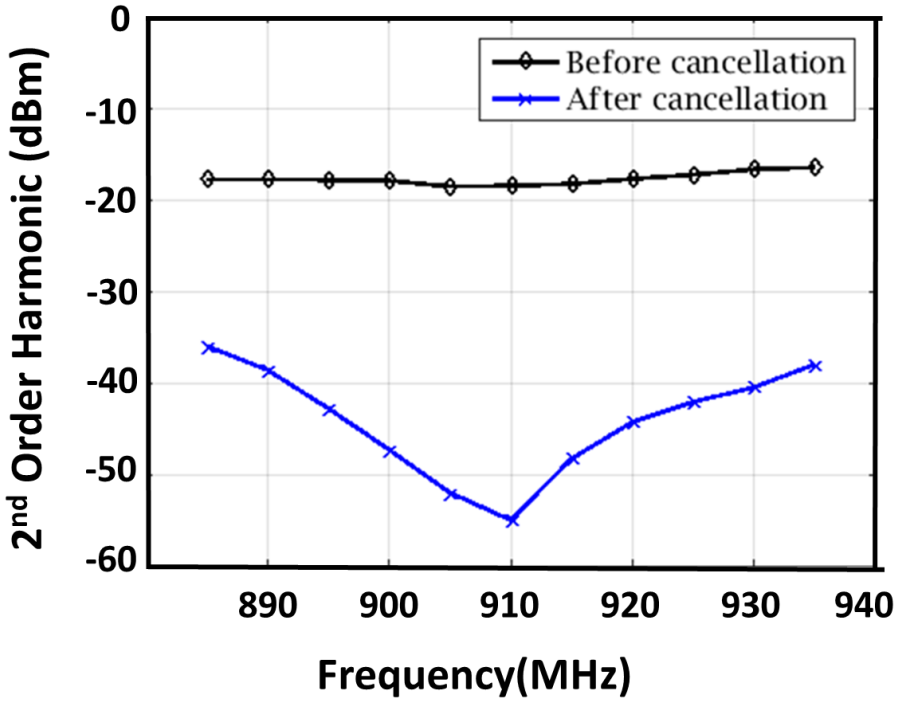

Figure 5.7. 2nd order harmonic cancellation vs. frequency.

less than -40dBm to meet the FCC requirements (Figure 5.8). Although the tuning range of the

phase shifter will likely be dependent on variations in the supply voltage, the proposed HRPA is still able to suppress the second order harmonic by as much as -40dBm over a voltage range from 1.1V to 1.2V. This is achieved by changing the code three times when the supply voltage changes (Figure 5.9).

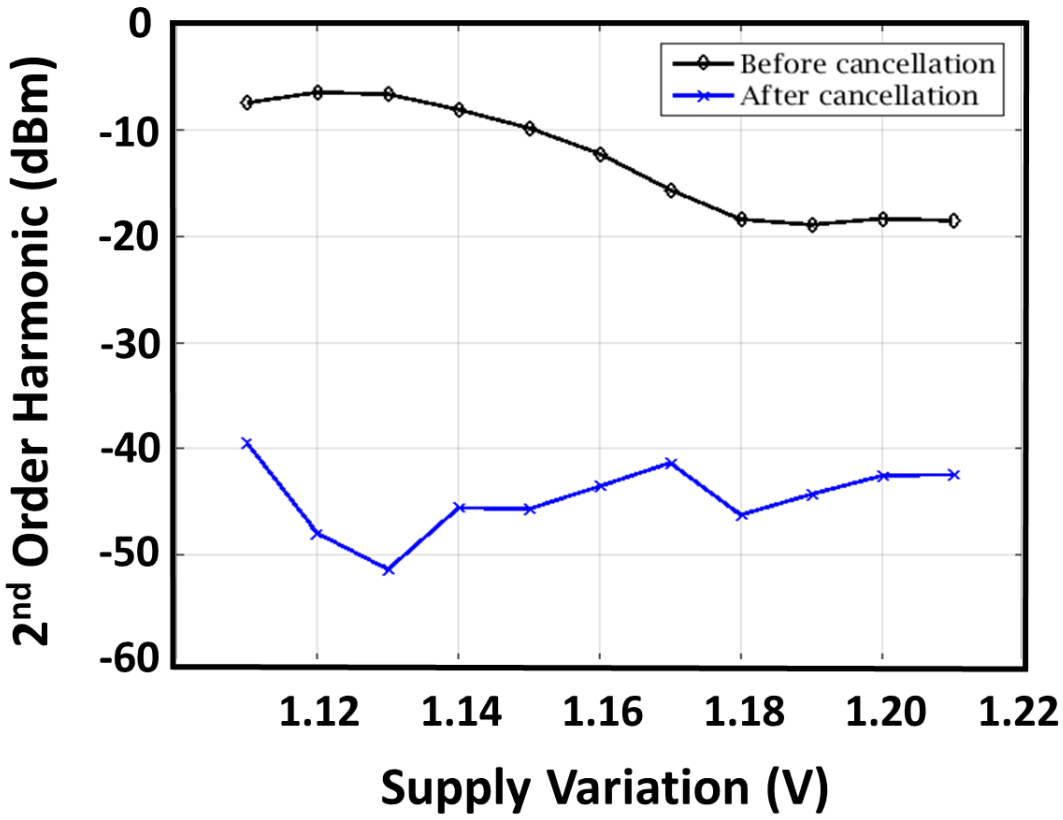

Figure 5.9. Cancellation vs. supply voltage.

5.2.4 *Measurement Results using a BPSK modulation signal*

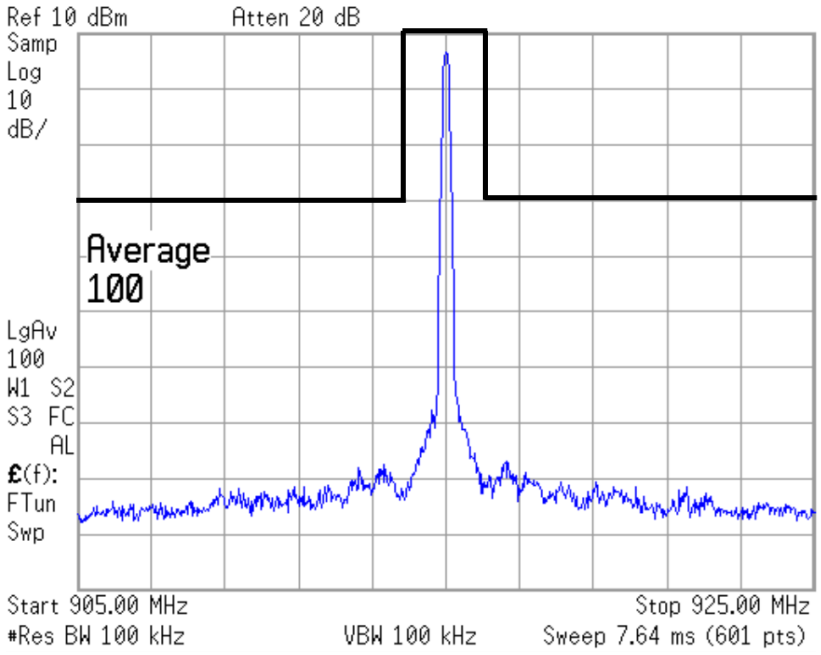

Figure 5.10. HRPA before harmonic rejection in-band measured output spectrum with 802.15.4 mask (RBW = 100 kHz).

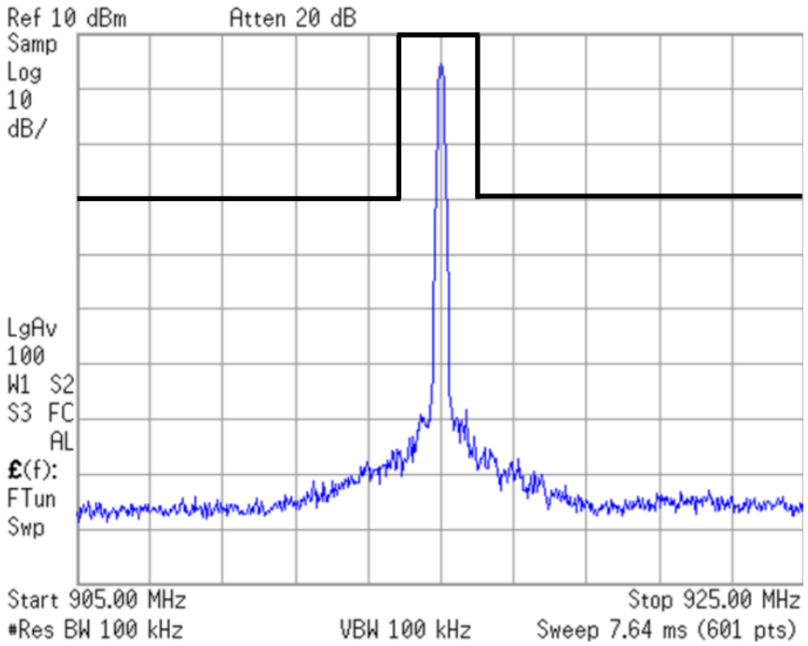

Figure 5.11. HRPA after harmonic rejection in-band measured output spectrum with 802.15.4 mask (RBW = 100 kHz).

The spectrum of the HRPA is also measured with a resolution bandwidth (BW) of 100 kHz according to ZigBee standard [1]. The RF input is a BPSK modulated signal utilizing a raised cosine filter with $\alpha = 1$. This PA successfully produces a modulated spectrum that falls within the required modulation mask (Figure 5.10, 5.11), as outlined by the ZigBee standard requirements

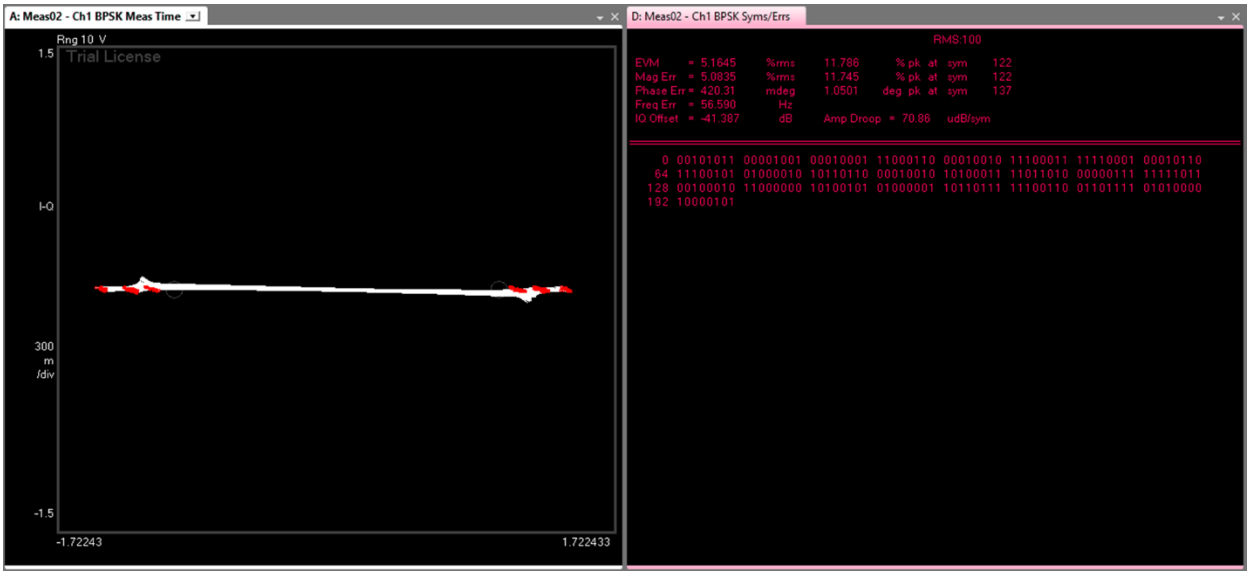

Figure 5.13. EVM of HRPA before harmonic rejection.

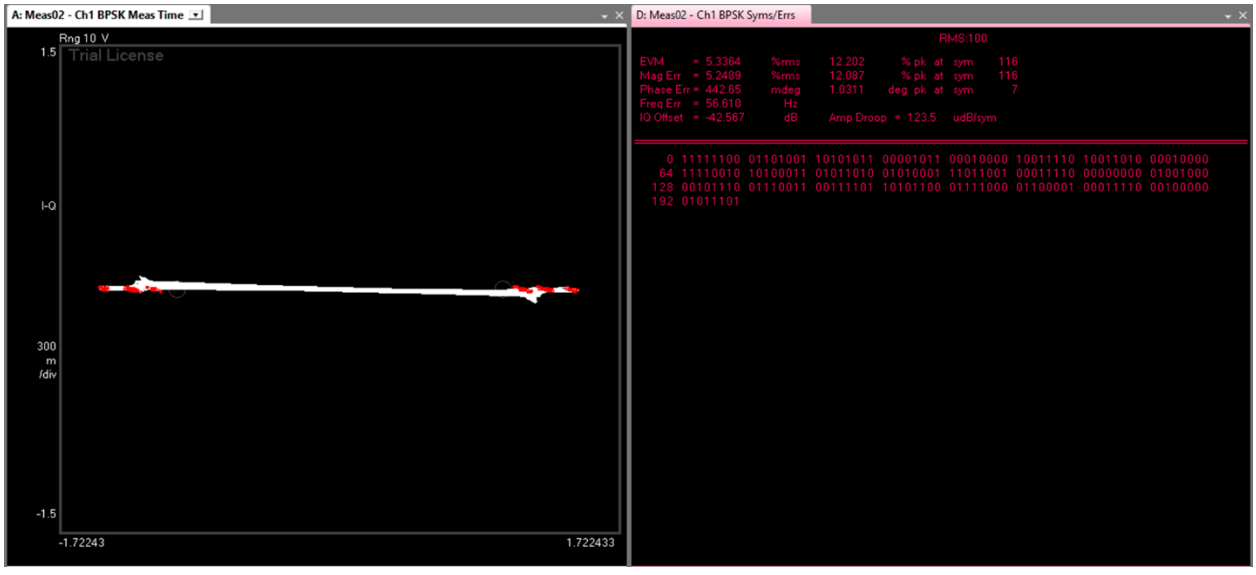

Figure 5.12. EVM of HRPA after harmonic rejection.

[1]. The Envelope Vector Magnitude (EVM) is tested with Keysight VSA 89600, and before harmonic rejection is 5.1% and after is 5.3%, which also meets the standard [1].

5.3 COMPARISON TABLE

Table 5.1. Comparison table of other Integrated Harmonic-Rejection Techniques.

Harmonic Rejection	T. Sano' 2015 ISSCC	A. Ba' 2014 RFIC	F.Jonas' 2010 ESSCIRC[7]	This Work
Architecture	Conduction Angle Calibration	Conduction Angle Calibration	Harmonic Reduction	HR SCPA
Technology/VDC	40nm/1.1V	40nm/1.0V	90nm/1.2V	40nm/1.1V
Output Power (dBm)	0	1.2	5.3	8.9
Frequency(GHz)	2.4	2.4	0.9	0.9
Drain Efficiency (%)	-NA-	39	62	43
Num. of Off-chip Components	No	3	3	1
HD2 (dBc)	-52.3	-50	-46.3	-65
HD3 (dBc)	-48	<-50	-45.3	-46
HD4 (dBc)	-NA-	<-50	<-55.3	-42

5.4 CONCLUSION

A feed-forward, switch-capacitor HRPA was fabricated in 40nm TSMC CMOS process with the ability to cancel the $2^{nd}/3^{rd}/4^{th}$ order harmonics by 48dB, 17dB, and 24dB, respectively. This compact solution requires a single off-chip inductor with all other circuitry integrated on-chip. This solution is well suited for ZigBee applications due to the low power and small-form factor. This approach is also well-suited for future Internet of Things (IoT) applications.

5.5 FUTURE WORK

The proposed HRPA can be well embedded into a full duplex system[13], [14], and maybe future expanded in a mm-Wave and IoT applications[15].

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