

A Single-Chip Digitally Calibrated 5.15–5.825-GHz 0.18- μm CMOS Transceiver for 802.11a Wireless LAN

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Abstract—The drive for cost reduction has led to the use of CMOS technology in the implementation of highly integrated radios. This paper presents a single-chip 5-GHz fully integrated direct conversion transceiver for IEEE 802.11a WLAN systems, manufactured in 0.18- μm CMOS. The IC features an innovative system architecture which takes advantage of the computing resources of the digital companion chip in order to eliminate I/Q mismatch and achieve accurately matched baseband filters. The integrated voltage-controlled oscillator and synthesizer achieve an integrated phase noise of less than 0.8° rms. The receiver has an overall noise figure of 5.2 dB and achieves sensitivity of -75 dBm at 54-Mb/s operation, both referred to the IC input. The transmit error vector magnitude is -33 dB at -5 -dBm output power from the integrated power-amplifier driver amplifier. The transceiver occupies an area of 18.5 mm².

Index Terms—5 GHz, 802.11a, digital calibration, direct conversion, orthogonal frequency division multiplexing (OFDM), RF CMOS, RF transceiver, system-on-a-chip (SOC), wireless, wireless LAN (WLAN).

I. INTRODUCTION

INCREASING demand for higher capacity in the growing wireless LAN (WLAN) market currently dominated by IEEE 802.11b-based systems has led to the introduction of a new generation of WLAN standards using more spectrally efficient modulation techniques. Ratified in 1999, the IEEE 802.11a [1] operates in the 5-GHz unlicensed national information infrastructure (UNII) band (5.15–5.35 GHz, 5.725–5.825 GHz) and is based on orthogonal frequency division multiplexing (OFDM). It supports data rates from 6 to 54 Mb/s compared with 1–11 Mb/s offered by the incumbent 802.11b. Operation at 5 GHz offers the additional advantage of less interference compared with the 2.4-GHz ISM band, where in addition to 802.11b, other band users include microwave ovens, Bluetooth systems, vintage 802.11 FH or DSSS systems, and cordless phones.

These advantages come at a cost, as OFDM-based systems pose significant implementation challenges requiring low in-band phase noise, high linearity, and accurate quadrature matching [2]. For example, in order to meet the transmitter error vector magnitude (EVM) specification for the 54-Mb/s mode with a 3-dB implementation margin, system simulation shows that an I/Q mismatch of $1.5^\circ/0.2$ dB, an integrated phase noise error of 1° rms, and operation at 8-dB backoff from the transmitter 1-dB compression point are required.

In addition to tight performance constraints, pricing pressures impose low-cost highly integrated implementations of radio systems. To address this need, the continuous trend toward low-cost integration has driven the introduction of innovative single-chip architectures in CMOS technologies as inexpensive alternatives to the traditional superheterodyne bipolar implementations [3]–[6] operating at frequencies up to 5 GHz [7]–[9]. However, such architectures suffer from well-documented shortcomings [10] that may limit their applicability.

This paper presents the detailed implementation of a single-chip 5-GHz direct conversion transceiver [11], which overcomes such limitations by means of the overall system design. The transceiver is part of a two-chip solution implementing both PHY and MAC for 802.11a. Well-known problems of direct conversion are addressed by digital calibration techniques, empowered by the new transceiver architecture and controlled by the companion baseband processor (BBP), as described in Section II. Section III presents circuit design details, and measurements results are given in Section IV. Overall conclusions are discussed in Section V.

II. ARCHITECTURE

A. Direct Conversion Imperfections

Although attractive as a highly integrated solution, direct conversion suffers from a variety of problems also shared by other integrated architectures such as low-IF [5] or wide-band-IF [4], which are further aggravated by using CMOS technology [10].

On the receive side, the most common problem is the presence of dc offsets, both static and time-varying [12]. In IEEE 802.11a, even though the downconverted I/Q signal occupies bandwidth from 150 kHz to 8.3 MHz, the maximum 40-ppm frequency mismatch allowed between transmitter and receiver may

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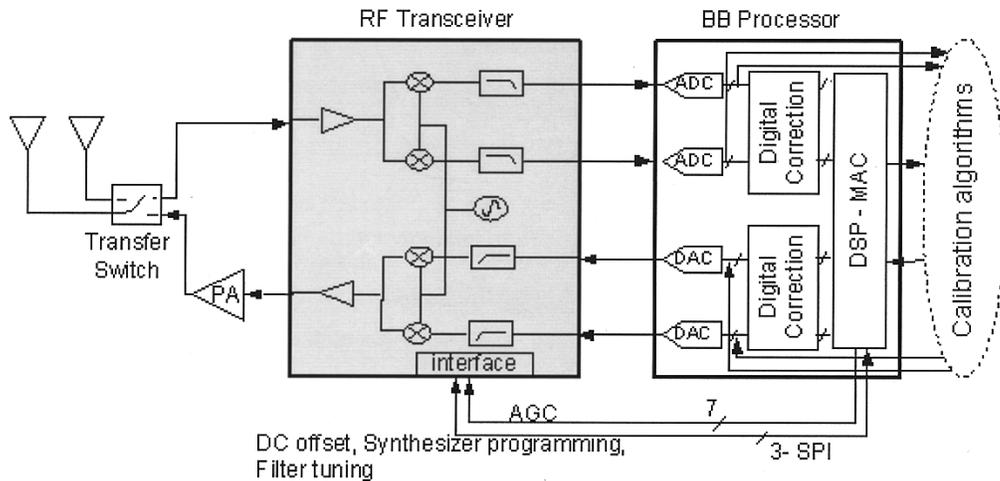


Fig. 1. System architecture.

shift the signal around dc, thus prohibiting ac coupling without using complex analog frequency correction techniques. Static dc offset is the result of component mismatches in the signal path and local oscillator (LO) leakage at the inputs of the mixer and the LNA due to finite on-chip isolation. The leakage signal after mixing with the LO produces a dc component at the baseband input, which depends on the frequency and power of the LO signal. Since static dc offset may be large enough to saturate the baseband receive chain, it needs to be cancelled in the analog domain.

In direct conversion receivers, time-varying dc offsets can be the result of self-mixing due to leakage of single-tone (CW) or frequency-modulated (FM) interference to the LO port. Similarly, second-order distortion applied to CW or FM interference results in dc offset, which varies with the frequency and the power level of the received signal. Since strong interference is not usually present in the 802.11a operating bands, the dominant mechanism causing time-varying dc offsets is self-mixing of the LO signal leaking to the antenna and reflected back from environment [12]. At 5-GHz carrier frequency, due to high attenuation and absorbance of reflected signals, such time-varying dc offsets are small (10–50 mV for a 2-V_{pp} signal) compared with the static dc offsets and the overall dynamic range of the receiver, thus they can be tracked and removed by digital signal processing (DSP) after analog-to-digital conversion.

Direct down/upconversion from/to 5 GHz requires quadrature LO generation at the RF carrier frequency, which may result in large gain and phase mismatches. Other significant problems include sensitivity to flicker noise and pulling of the voltage-controlled oscillator (VCO) by the external or on-chip power amplifier (PA). In addition to these architecture-related nonidealities, higher order QAM-OFDM modulation requires tightly matched baseband I/Q filters on both transmit and receive side to avoid degradation of the overall EVM.

Some of the aforementioned problems can be mitigated by careful circuit design and layout, analog autocalibration techniques, or one-time calibration at production testing [13]. Such approaches may require several design iterations and be highly sensitive to process variations, thus degrading yield and

increasing overall cost, which may cancel the advantages of using CMOS integrated architectures.

B. Overall System Architecture

The overall system architecture introduced by this work is shown in Fig. 1 and consists of the RF transceiver plus a companion BBP. A key principle used is the compensation of transceiver nonidealities using computing resources of the BBP. The first component of the system is the RF transceiver, which is described in detail in this paper. The second component is the BBP with the capability of real-time digital pre-distortion and post-distortion, which is needed for compensation of transmitter (TX) and receiver (RX) I/Q mismatch and TX LO leakage. The BBP can also simultaneously send I/Q stimuli to the transceiver via its digital-to-analog converters (DACs) and receive I/Q signals via its analog-to-digital-converters (ADCs) that can be subsequently processed. This enables the measurement of analog imperfections of the transceiver during a calibration phase, using built-in loop-back connections shown in the detailed block diagram of Fig. 2. The third component of the system is the calibration algorithms, which compute the necessary correction parameters for the analog imperfections. These algorithms are implemented either on the digital companion IC or in software on the host processor.

The RF transceiver employs direct conversion on both transmit and receive side. The phase-locked loop (PLL) frequency synthesizer operates at half the carrier frequency to avoid VCO pulling from the transmitted RF signal. Calibration switches SW6–SW7 are used for TX/RX I/Q mismatch measurement. Switches SW1–SW5 enable measurement of frequency response of the baseband filters, which are tuned to the desired cutoff by on-chip 8-bit DACs. DC offset is corrected at the output of the RX mixers by two independent 8-bit current-steering DACs.

C. Digital Calibration

Transceiver calibration is essential in compensating for the following transceiver nonidealities: receiver static dc offsets,

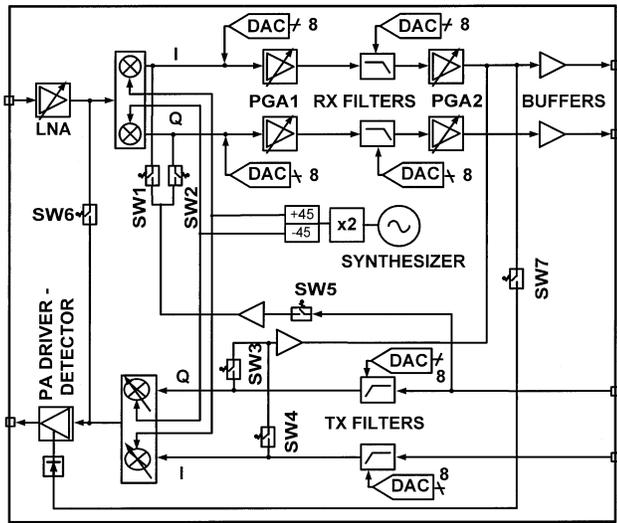


Fig. 2. 5-GHz RF transceiver block diagram.

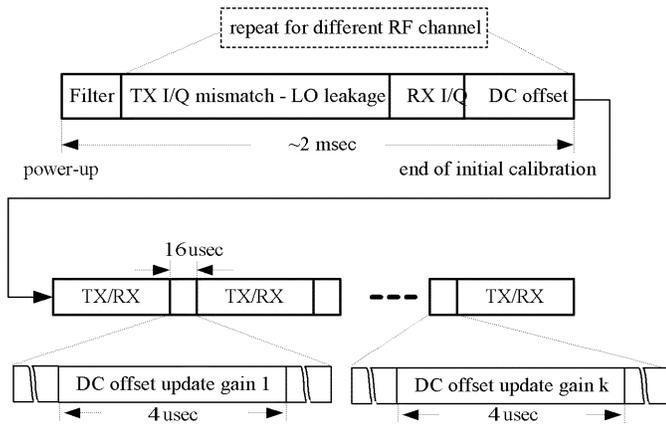


Fig. 3. Power-up and interframe calibration timing.

transmit and receive I/Q mismatch, transmit LO leakage, and filter cutoff frequency mismatch. During the initial power-up calibration cycle shown in Fig. 3, compensation parameters are computed and stored.

The static dc offset is initially measured by averaging the received I and Q signals while in receive mode. By adjusting the current of the dc offset correction DACs at the outputs of the receive mixers, the I and Q dc offset is minimized for different receive gain settings and a corresponding lookup table is programmed on the RF transceiver. Since LO leakage is typically a function of the carrier frequency, this procedure is repeated at different RF channels. To compensate for temperature drifts, static dc calibration is repeated periodically for the highest gain modes at the channel in which the transceiver operates. In 802.11a systems, consecutive frames are received or transmitted with a 16- μs turnaround time, which allows for short dc offset calibration cycles even in continuous reception or transmission of frames, as shown in Fig. 3. The short duration of 802.11a frames ensures that fast temperature drifts can be tracked.

Transmit and receive I/Q gain and phase mismatch compensation parameters are measured during the power-up calibration

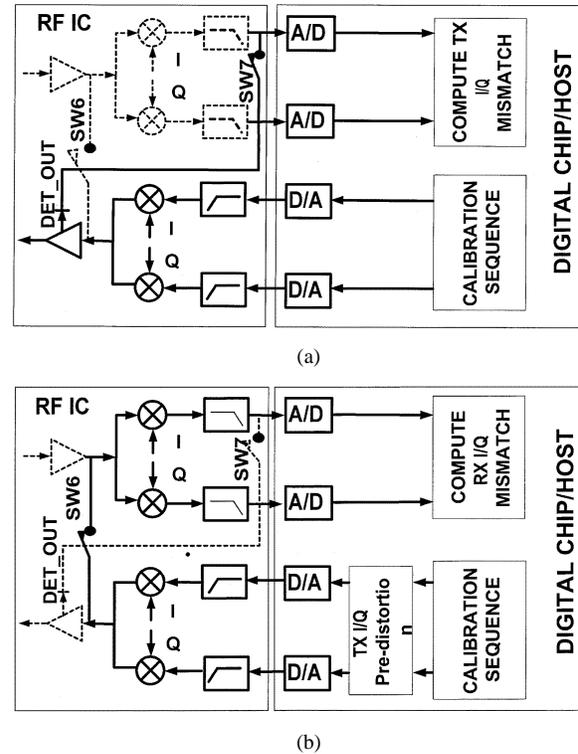


Fig. 4. (a) TX I/Q mismatch measurement. (b) RX I/Q mismatch measurement.

cycle. Since I/Q mismatch is also RF channel dependent, calibration has to be repeated for different channels. The measurement is done in two phases. First, the digital companion chip transmits a calibration waveform, which is subsequently upconverted to RF and amplitude demodulated by an on-chip envelope detector [Fig. 4(a)]. By closing switch SW7, the envelope of the RF signal is digitized by the I-ADC of the digital chip and is used to jointly estimate transmit I/Q mismatch and LO leakage [14]. Once estimated, LO leakage and I/Q mismatch can be removed by digital pre-distortion during normal transmit operation.

In the second phase of this procedure, shown in Fig. 4(b), the digital chip transmits a calibration waveform, which is upconverted to RF. During this phase TX I/Q mismatch is compensated using the parameters acquired at the previous phase. By closing switch SW6, the RF signal is looped back to the input of the quadrature demodulator, downconverted to baseband, and digitized by the receive I/Q ADCs. The principle of the RX I/Q mismatch measurement lies in transmitting a constant amplitude signal with rotating phase in the I/Q plane. Once demodulated, if receive I and Q paths are perfectly matched, the demodulated signal appears as a perfect circle, when plotted in I/Q coordinates. However, in the presence of gain and phase mismatch, the demodulated signal appears as an ellipse (Fig. 5). By analyzing the properties of this ellipse, the receive I/Q mismatch can be accurately measured. When the transceiver is in receive mode, the acquired I/Q mismatch is removed using digital post-distortion. During the initial I/Q mismatch calibration procedure, the external RF switch is disconnected from the antennas and the PA is powered down, to avoid violating spectral emission limitations.

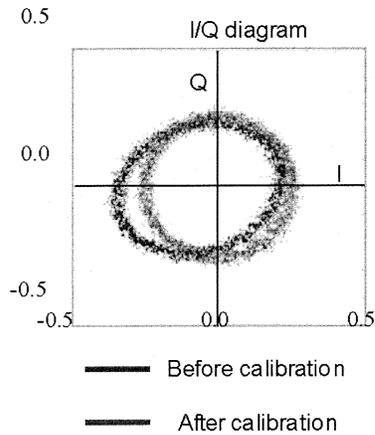


Fig. 5. Received I/Q plot signal before and after RX I/Q mismatch calibration.

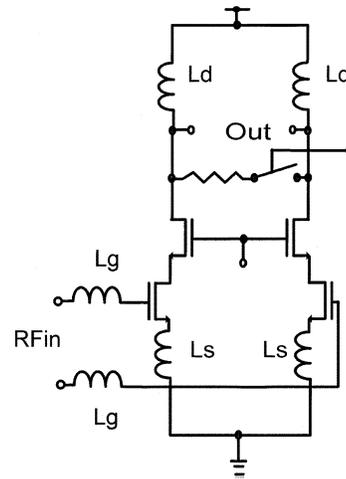


Fig. 7. LNA.

III. CIRCUIT IMPLEMENTATION

Both transmitter and receiver employ fully differential signal paths to reduce second order distortion and minimize substrate and supply coupling. Integrated inductors are extensively used for matching and tuning of RF circuits. They are realized using the thick sixth metal layer option of the available CMOS process which helps achieve a quality factor Q of 10 at 5 GHz. MIM capacitors are used for coupling between RF stages and bypass and filtering of supply and bias nodes. To achieve better isolation, substrate tap rings tied directly to the exposed grounded cavity of the MLF package are used.

A. Receiver

The fully balanced low-noise amplifier (LNA) shown in Fig. 7 uses the nMOS common-source cascode topology with inductive degeneration provided by on-chip spiral inductors (L_s). Input matching is achieved by bondwire and package inductances (L_g), which result into lower loss and reduced area compared with on-chip matching schemes. S_{11} lower than -8 dB is achieved in the 5.15–5.825-GHz range with a typical value of -12 dB at frequencies between 5.15 and 5.35 GHz. Two different gain settings of 18 and 10 dB can be selected by resistive loading of the output. This approach helps reduce variations in input impedance. The LNA is optimized for operation at 5.15–5.35 GHz. Measurements from a replica standalone structure with an off-chip matching network indicate that it achieves a noise figure (NF) of 3 dB and an input third-order intercept point (IIP3) of 4 dBm. The NF in the 5.725–5.825-GHz band is 4.5 dB.

The output of the LNA is demodulated directly into baseband by a quadrature demodulator. Since in direct conversion receivers the output of the RF mixers is a baseband signal, flicker noise from the switching pair may severely impact the received signal-to-noise ratio (SNR) [15]. To reduce this effect, the mixer topology shown in Fig. 8 is used. The circuit uses nMOS devices to convert the input RF signal into current, which is subsequently folded into a pMOS switching pair. This structure presents inherently lower flicker noise at the output. The high conversion gain achieved by the input transconductance stage

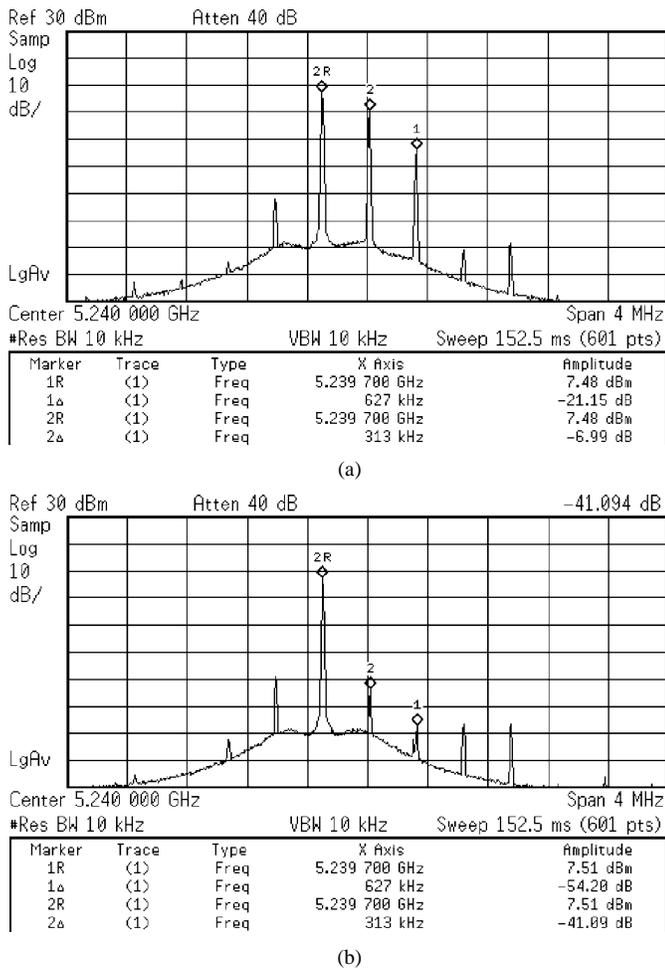


Fig. 6. Transmit single-sideband spectrum. (a) Before I/Q mismatch calibration. (b) After I/Q mismatch calibration.

Fig. 6 shows the measured spectrum of an upconverted single-sideband tone before and after transmit I/Q mismatch calibration, which achieves LO leakage of -41 dBc and unwanted sideband suppression of 54 dB.

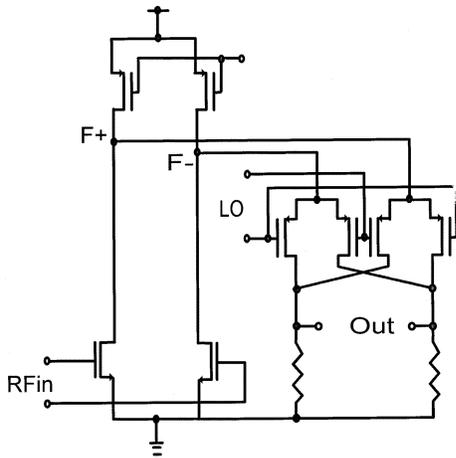


Fig. 8. Quadrature demodulator mixer cell.

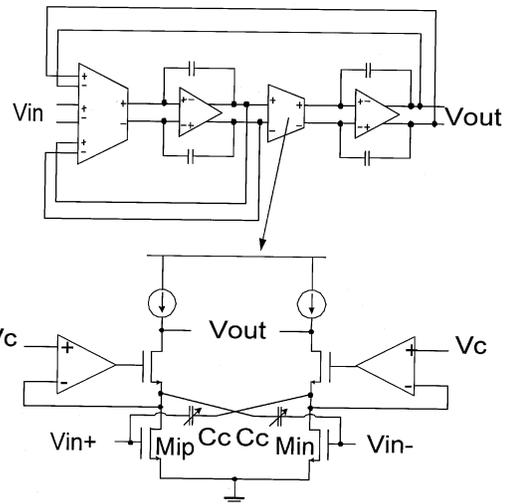


Fig. 10. Baseband filter biquad and transconductor.

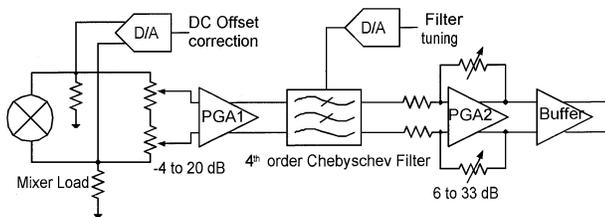


Fig. 9. Baseband path.

helps minimize the contribution of the pMOS current sources in the overall NF. Special care is taken to minimize the capacitance in nodes $F+$ and $F-$ in order to reduce signal loss. An operational-amplifier-based feedback circuit stabilizes the output common-mode voltage. Extrapolation from the overall RX path measurements indicate that the mixer achieves 10 dB of gain, a double-sideband NF of 12 dB, and an IIP3 of -5 dBV.

The baseband path of the receiver shown in Fig. 9 consists of two digitally programmable gain amplifiers (PGA), a low-pass filter, and an output buffer. To achieve optimum noise/linearity performance, the two PGAs are located before and after the RX channel-select filter. The first PGA employs a pMOS low-noise high-dynamic-range differential pair amplifier with a resistive attenuator at its input, while the second one is an operational-amplifier-based feedback gain stage. The composite gain varies from 2 to 53 dB, programmable in 3-dB steps by an external 6-bit word provided by the baseband processor.

Baseband channel selection is performed by fourth-order Chebyshev filters with 0.5-dB ripple and 9-MHz nominal bandwidth. The filter is implemented as a cascade of two biquads using G_m -OTA-C integrators, as shown in Fig. 10 [16]. The operational transconductance amplifier (OTA) is a simple differential pair, while the transconductor cell is based on the regulated cascode topology shown in Fig. 10 [17]. The transconductance is set by a tuning voltage V_c , which is applied to the drain of the input transistors M_{ip} and M_{in} operating in the triode region. The tuning voltage is generated by an on-chip 8-bit DAC controlled by the digital chip. The DAC uses a proportional-to-absolute-temperature (PTAT) current biasing scheme to compensate for transconductance temperature drifts after the initial filter tuning during the powerup procedure.

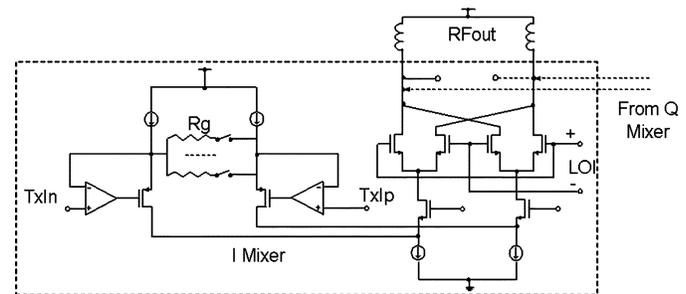


Fig. 11. TX mixer.

Finally, the feedforward MOS capacitor array C_c can be used for controlling the quality factor Q of the filter.

During transceiver calibration, the frequency responses of both I and Q receive baseband paths are independently measured and corrected. The I path is measured from the feedback path formed by switches SW5 and SW1 to the Q path from SW5 and SW2. A calibration sequence [18] generated digitally is used to set the bandwidth to 9 MHz. Measurements show that matching better than 1% can be achieved between the I and Q filters by using the above tuning scheme. The overall tuning range of the passband is 5–15 MHz. The output of the receiver is digitized by dual 10-bit 40-MHz ADCs on the digital companion chip.

B. Transmitter

In the transmit path, the baseband I/Q signals are generated by dual 10-bit 40-MHz DACs in the companion digital chip. The transmit baseband filters are identical to the ones used in the receiver and can be calibrated digitally by measuring their frequency response through the feedback path formed by switches SW3 and SW4. The signal is directly upconverted to RF by a programmable gain modulator (PGM) based on the Gilbert-type mixer shown in Fig. 11. To achieve the required linearity, the modulator input voltage is converted into a current across the degeneration resistors R_g by a negative feedback loop that employs a high gain-bandwidth operational amplifier. The current is then folded via a cascode current source to drive the mixer

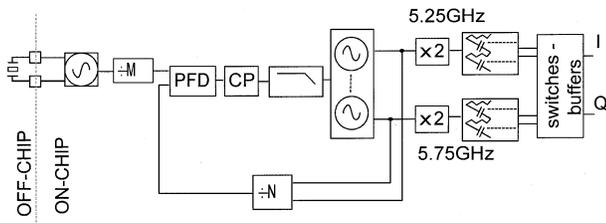


Fig. 12. Synthesizer block diagram.

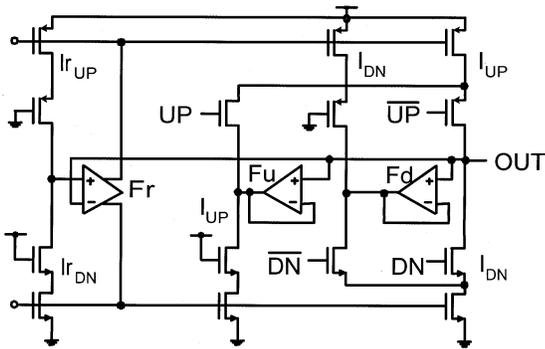


Fig. 13. Charge pump.

switches. The output of the I and Q mixers is summed by a pair of integrated inductors in order to drive the RF output amplifier. Gain programmability is achieved by adjusting the input transconductance stage using a switchable resistive ladder. The modulator provides 27 dB of gain control in 3-dB steps and achieves an IIP3 of 20 dBm at maximum gain. Finally, the RF output driver amplifier is a single-stage differential pair, inductively degenerated to improve linearity. It can achieve an output P-1-dB compression point of 5 dBm when driving a 50- Ω differential load, enabling the transmitter to deliver an EVM of -33 dB at -5 -dBm output power.

C. Synthesizer

The main challenge in designing a frequency synthesizer for an OFDM-based transceiver lies in reducing the in-band integrated phase noise, which degrades the overall EVM by introducing intersubcarrier interference [2]. In a CMOS integrated PLL, phase noise is typically dominated by the on-chip VCO. A common design technique to minimize the phase noise of the VCO is to make the PLL loop bandwidth as wide as possible. The optimal loop bandwidth is usually the limit where phase noise contributions from other sources, such as the prescaler, charge pump, and loop filter, equal the contribution from the VCO [19]. A second design challenge in the direct conversion architecture is minimization of LO pulling from the external or on-chip PA.

The implemented synthesizer shown in Fig. 12 is an integer- N wide-band PLL using a third-order passive loop filter. As confirmed by measurements, operation of the VCOs at half the carrier frequency minimizes pulling. Two different VCOs are used, centered at 2.6 and 2.9 GHz, followed by Gilbert-cell-based doublers and integrated second-order polyphase filters for quadrature signal generation. Active RF switches select the appropriate LO. The programmable

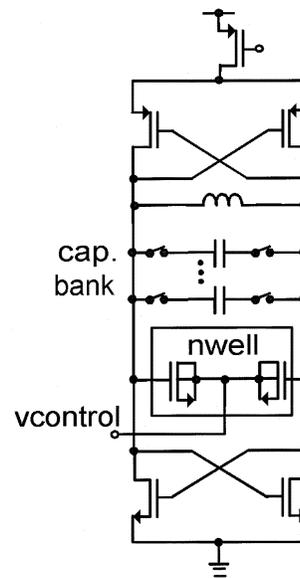


Fig. 14. VCO.

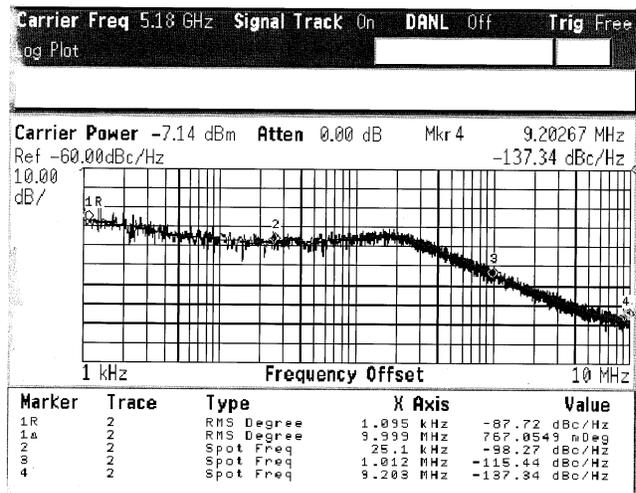


Fig. 15. Synthesizer phase noise plot at 5.18 GHz.

500/100-kHz loop bandwidth is optimized separately using 10 and 2.5 MHz reference frequencies for the 5.15–5.35-GHz and 5.725–5.825-GHz bands, respectively.

The charge pump shown in Fig. 13 uses the feedback amplifier F_r to eliminate mismatch between up and down currents, while amplifiers F_u and F_d replicate the dc output voltage to the dummy current switches. This technique helps achieve spurs below -65 dBc at 10-MHz offset for the 5-GHz band. The programmable divider in the feedback loop is formed by cascaded 2/3 divider stages giving division ratios of 2^n to $2^{n+1}-1$ where n is the number of stages used. Eight divider stages are used in the 5.15–5.35-GHz band to achieve division ratios between 256 and 511, while ten divider stages are used in the 5.725–5.825-GHz band to achieve ratios between 1024 and 2047 [20].

Both VCOs use the topology shown in Fig. 14. The circuit uses a complementary pair of negative resistor structures, which results in reduced flicker noise upconversion [21]. Fine tuning is achieved by accumulation-mode MOS varactors, while a switched capacitor bank provides extra tuning range to

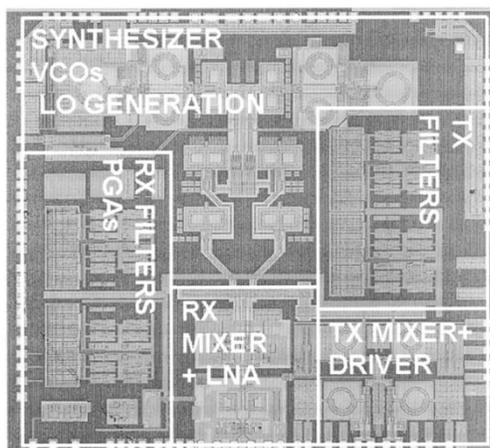


Fig. 16. Chip microphotograph.

TABLE I
MEASURED TRANSCEIVER PERFORMANCE SUMMARY

Parameter	Value
Power Supply	1.8 V / 3.3V I/O
TX mode power dissipation	302 mW
RX mode power dissipation	248 mW
RX Chain path noise Fig. (chip input)	5.2 dB
RX Chain path max/min gain	79 / 20 dB
RX path P-1dB (min gain)	-20 dBm
Integrated Phase noise (1 kHz to 10 MHz– DSB)	0.8°
Phase noise at 1MHz offset	-115 dBc/Hz
Supported bands	5.15–5.35 GHz 5.725–5.825 GHz
TX output P-1dB (chip output)	6 dBm
Technology	1P6M CMOS 0.18 μ m
Sensitivity at 54 Mb/s (chip input)	-75 dBm
Required sensitivity at 54 Mb/s [1]	-65 dBm
TX EVM at 54 Mb/s (chip output)	-33 dB (Pout = -5 dBm)
Required TX EVM at 54 Mb/s [1]	-25 dB
Adjacent channel rejection at 54Mb/s	+17 dB
Required adjacent channel rejection at 54Mb/s [1]	-1 dB
Alternate adjacent channel rejection at 54Mb/s	+22 dB
Required alternate adjacent channel rejection at 54Mb/s [1]	+15 dB
Die Size	4.5mm x 4.1mm
Package	MLF-64

absorb process variations. The synthesizer achieves phase noise of -115 dBc/Hz at 1-MHz offset and integrated phase noise of 0.8° from 1 kHz to 10 MHz (Fig. 15) for the 5.15–5.35-GHz band and 1.7° in the 5.725–5.825-GHz band.

IV. MEASURED RESULTS

The transceiver is implemented using a 0.18- μ m 1P6M CMOS process and occupies a total silicon area of 18.5 mm^2 . A die microphotograph is shown in Fig. 16. The setup used to evaluate the transceiver performance consists of the RF evaluation board under test and a mixed-signal test board that includes

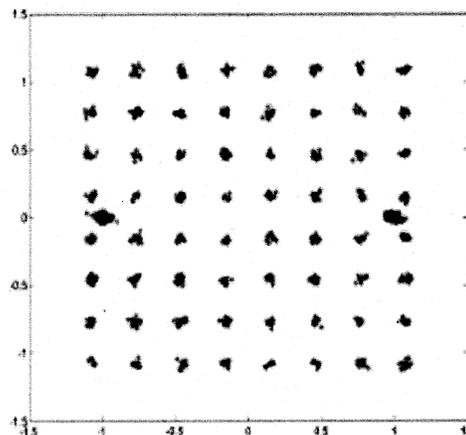


Fig. 17. Received constellation for 54 Mb/s for -55 dBm input.

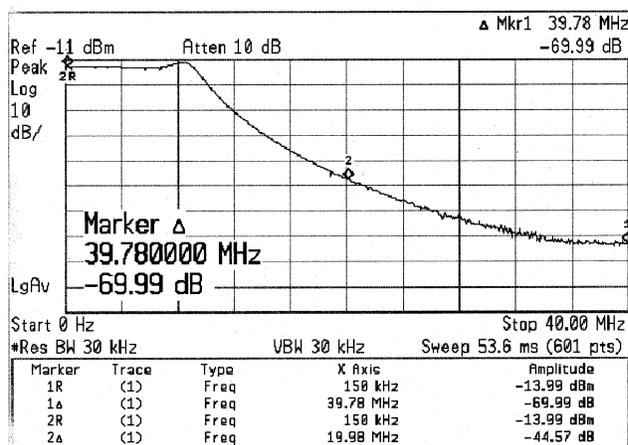


Fig. 18. Receive chain frequency response.

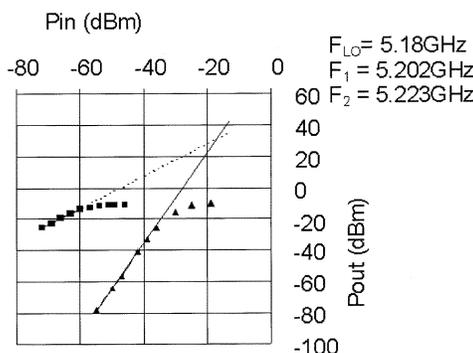


Fig. 19. Receiver IIP3—maximum gain.

dual 10-bit 40-MHz ADCs and DACs, two field-programmable gate array chips (FPGAs) implementing in real-time the 802.11a preamble detector and a digital acquisition system used to transfer data to/from a personal computer. All calibration routines and the modulator/demodulator including a soft Viterbi decoder were implemented in software. The system was designed to interoperate with 802.11a measurement systems in bursts of a few seconds long, so that the real-time performance of the RF transceiver can be evaluated.

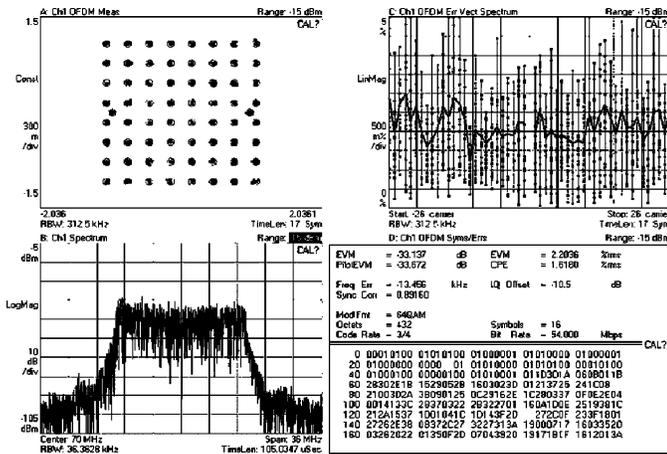


Fig. 20. Transmitter EVM at -5 -dBm output power.

Typical measurement results are summarized in Table I. Performance numbers do not include losses of the external components of the evaluation printed circuit board. The receiver achieves a NF below 5.2 dB measured at the IC input for the entire range of the 5.15–5.35-GHz band. For the 54-Mb/s mode, the sensitivity for 10^{-5} bit-error rate (BER) is -75 dBm at the LNA input. The received constellation for the 54-Mb/s mode operating in the 5.24-GHz channel, shown in Fig. 17, achieves an EVM of -34 dB for -55 -dBm input power. The overall frequency response of the receiver from the input of the LNA to the output of the receive buffers is shown in Fig. 18. Receive IIP3 is -8 dBm at minimum gain and -18 dBm at maximum gain, as shown by the two-tone test in Fig. 19. Low intermodulation at high gain and careful planning for distribution of gain and filtering in the receive chain help achieve an adjacent channel rejection of $+17$ dB at 54 Mb/s compared with the -1 dB required by the standard.

Due to the low in-band integrated phase noise and the low residual I/Q mismatch achieved by digital calibration, the EVM is reduced to -33 dB when the transmitter operates at -5 -dBm output power in the 54-Mb/s mode (Fig. 20). Fig. 21 illustrates the impact of accurate calibration and low integrated phase noise in the TX EVM, as measured at chip output power of -5 dBm. TX I/Q mismatch was modified by digital pre-distortion as explained in Section II, and the corresponding sideband rejection was measured. Integrated phase noise was modified by programming the current of the charge pump and by changing the PLL loop filter. Fig. 21(a) shows that low integrated phase noise can improve the overall EVM of the chip by 3–4 dB, as shown by the difference of the plots corresponding to 0.8° and 1.4° . Given that typical IC processes can achieve a sideband rejection of 35 dB [22], digital calibration I/Q can improve EVM performance by at least 2 dB. Fig. 21(b) shows the impact of filter matching; a cutoff frequency mismatch of 2% between I and Q in the fourth-order Chebyshev filters used in the TX path may degrade EVM by more than 3 dB. Given that the overall TX EVM depends on both the transceiver performance and the external PA, these results indicate that calibration enables the overall system to operate at higher output power while meeting the 802.11a requirement of -25 -dB EVM or that for a given output power,

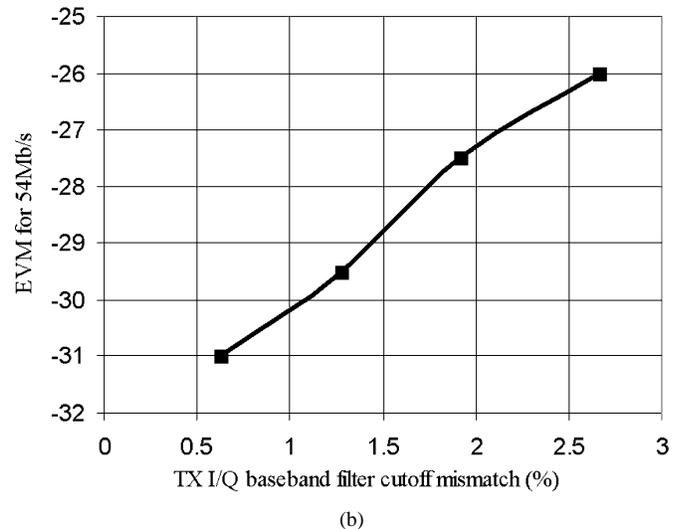
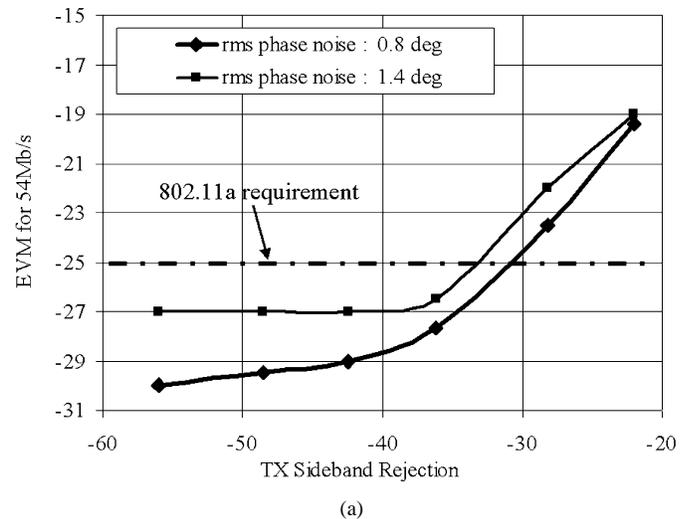


Fig. 21. Measured TX EVM performance. (a) As a function of TX I/Q mismatch and phase noise. (b) As a function of I/Q baseband filter cutoff mismatch.

a more power-efficient PA can be used. Measurements with an external PA demonstrate that the TX EVM specification of -25 dB can be met at 16-dBm output power.

V. CONCLUSION

A fully integrated 802.11a direct conversion transceiver has been implemented in a $0.18\text{-}\mu\text{m}$ CMOS technology. The transceiver features state-of-the-art noise figure and phase noise performance. By taking advantage of an innovative architecture utilizing free system computing resources, direct conversion and CMOS-process-related imperfections are corrected and the transceiver exceeds standard specifications by a wide margin, as indicated by detailed experimental results. Common techniques usually employed to compensate such nonidealities rely on purely analog techniques and calibration during production testing, which may increase cost and lower overall yield. The technique presented in this paper promises to improve the reliability and yield of CMOS RF transceivers, making CMOS a viable IC process option for state-of-the-art cost-effective radios.

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