17.8 A 5th-Order Continuous-Time Harmonic-Rejection G_mC Filter with In-Situ Calibration for Use in Transmitter Applications

Jacques C. Rudell, Ozan E. Erdogan, Dennis G. Yee, Roger Brockenbrough, Cormac S. G. Conroy and Beomsup Kim

Berkäna Wireless, Campbell, CA

The advent of sub-micron CMOS processes has ushered in a new generation of highly integrated, low-cost communication systems for a variety of applications from single-chip wireline Gigabit Ethernet transceivers to monolithic wireless front-ends. Reduced form factor and lower cost are two of the well known benefits of integration in CMOS. However, additional benefits are derived through the integration of a mixed-signal system in CMOS, by allowing new digital calibration techniques to enhance the analog circuit and system performance. As an example of these concepts, this paper presents a continuous-time filter with a new, in-situ filter calibration method. The intended application of this filter is to suppress all higher-order harmonics generated by both a modulator and feedback mixer within a GSM offset-PLL (OPLL) transmitter [1]. This paper describes the OPLL filtering requirements, the implementation of the filter, followed by a description of the filter tuning technique along with measured results.

A key block of any OPLL is the harmonic-rejection filters which precede the PFD shown in Fig. 17.8.1. Specifically in the GSM standard, the modulation mask is greatly influenced by these filters, particularly the requirement of -60dBc, 400kHz offset from the carrier. The filter attenuates unwanted energy produced at all the higher-order harmonic frequencies generated by the mixing of LOs in the OPLL reference and feedback paths. These harmonics, if left unfiltered, would pass through the hard non-linearity associated with the PFD, intermodulate, and create undesired energy in the wanted signal band. This is illustrated with the 3^{rd} and 5^{th} harmonics in Fig. 17.8.1.

Based on system simulations, the filter is implemented as a cascade of one real pole followed by two biquad stages where all poles are realized with a differential G_m -C approach, as shown in Fig. 17.8.2. The filter must be tunable from 60 to 150MHz with 5% tuning accuracy. Each capacitor is tunable with a fixed base capacitance of 250fF in parallel with a 6b capacitor array, binary weighted with an LSB of 25fF. Coarse filter band selection is realized by varying the degeneration resistance through a 3b resistor array in all Gm stages, Fig. 17.8.2.

All the capacitors are equal in size with the same capacitor settings in each array. Therefore, the frequency response is defined by the ratio between G_m stages within the biquad. To ensure good matching between G_m cells and an accurate biquad Q over temperature and process, a unit G_m cell is created. A different transconductance from the unit cell is derived by scaling all devices by a factor of α , where α corresponds to the ratio between the desired value of G_m to the unit G_m , Fig. 17.8.2.

This paper provides a salient approach to filter tuning applicable to a broad class of filter applications. In this tuning approach, prior to normal TX operation, the filter biquads are reconfigured, creating positive feedback and transforming the filter into an oscillator, as shown in Fig. 17.8.3. The output of this oscillator is then digitized with an inverter and a set of counters are used to estimate the oscillation frequency relative to an accurate crystal reference. A closed-form solution may be obtained for the oscillation frequency of the filter by evaluating the configuration in Fig. 17.8.3, to find the frequency at which the phase through the loop equals 360° . For this configuration, the loop gain when the phase reaches 360° is much greater than 1, thus satisfying the condition for oscillation. The oscillation frequency ω_{osc} is given in Fig. 17.8.3 and is dependent exclusively on values of G_m and C in the filter. Therefore, an estimate of component values over process and temperature can be obtained given that a ratio between the oscillation frequency and the filter –3dB frequency exists; this ratio is approximately 1.5.

Prior to normal TX operation, this filter is calibrated. Switch SW1 is opened while switches SW2 are closed. The oscillation frequency of the filter is then measured by counting the number of rising edges produced by the oscillator during a fixed period, as determined by another counter clocking off a crystal reference source. With an estimate of the oscillation frequency, all the capacitors in the filter are adjusted. The process of measuring the oscillation frequency and tuning the capacitors is then repeated through a method of successive approximation until the targeted oscillation frequency, and ultimately the filter corner frequency, for a targeted IF is achieved. SW1 and SW2 are then set for normal filter operation.

This tuning approach differs from previous master-slave methods [2] which require extra hardware and rely on matching between the tuning element and the filter components. Other attempts at in-situ filter tuning require additional hardware to generate calibration tones injected into the filter [3]. Two primary advantages exist for this filter tuning method. First, the filter is being tuned in situ. Stated differently, the devices being tuned are the same elements which will be used by the filter during normal operation. Second, a relatively small amount of digital hardware is required to tune this filter, thus minimizing the calibration hardware and chip area.

Figure 17.8.4 shows the measured filter frequency response, the filter tuning range, BW resolution of 2%, and demonstrates the filter capability of retuning over temperature, and returning to the targeted BW. In Fig. 17.8.5, the TX output spectrum is shown when the filter is in the narrowest BW setting, widest BW, and the ideal target BW after calibration. Note that in the widest BW setting, the modulation mask is degraded due to intermodulation. The modulation mask is met with margin in the narrowest BW state, but the wideband OPLL noise is higher than the attenuation of the desired signal if the filter BW is too narrow. Finally, Fig. 17.8.6 illustrates the tradeoff between the modulation mask performance at 400kHz offset and the inband integrated OPLL phase noise as a function of the filter capacitor tuning codes, where a low number on the x-axis corresponds to the widest filter BW. The post calibration filter setting is marked and represents the optimal setting for the overall TX performance. This filter is integrated with the entire transmitter in a 0.18µm CMOS technology. Die micrograph with a summary of data is shown in Fig. 17.8.7.

Acknowledgements:

The authors thank Julian Tham, Ham Lenh and Jin-Su Ko for their contributions.

References:

[1] T. Yamawaki et al., "A 2.7-V GSM RF Transceiver IC," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2089-2096, Dec., 1997.

[2] M. Banu and Y. Tsividis "On-Chip Automatic Tuning for a CMOS Continuous-Time Filter," *ISSCC Dig. Tech. Papers*, pp. 286-287, Feb., 1985.

[3] H. Khorramadabi et al., "Baseband Filters for IS-95 CDMA Receiver Applications Featuring Digital Automatic Frequency Tuning," *ISSCC Dig. Tech. Papers*, pp. 172-173. Feb., 1996.

2005 IEEE International Solid-State Circuits Conference

0-7803-8904-2/05/\$20.00 ©2005 IEEE

Authorized licensed use limited to: University of Washington Libraries. Downloaded on December 3, 2009 at 17:03 from IEEE Xplore. Restrictions apply.



Authorized licensed use limited to: University of Washington Libraries. Downloaded on December 3, 2009 at 17:03 from IEEE Xplore. Restrictions apply.

17

Reference Path HR Filter HR Filter	
Filter Performance	
Minimum Filter BW	48MHz
Maximum Filter BW	184MHz
Filter resolution Max. BW	3.1MHz (2 %) @ 151MHz
Filter resolution Max. BW Filter resolution Min. BW	3.1MHz (2 %) @ 151MHz 701kHz (1.5%) @ 48MHz
Filter resolution Min. BW	701kHz (1.5%) @ 48MHz
Filter resolution Min. BW IIP3	701kHz (1.5%) @ 48MHz 7dBV
Filter resolution Min. BW IIP3 Filter Input Noise inferred from TX measurement	701kHz (1.5%) @ 48MHz 7dBV 9.3µV _{RMS} (30kHz BW)
Filter resolution Min. BW IIP3 Filter Input Noise inferred from TX measurement Worse Case Calibration Time	701kHz (1.5%) @ 48MHz 7dBV 9.3μV _{RMS} (30kHz BW) 90μs
Filter resolution Min. BW IIP3 Filter Input Noise inferred from TX measurement Worse Case Calibration Time Measured Rejection at 3 rd and 5 th Harmonic	701kHz (1.5%) @ 48MHz 7dBV 9.3μV _{RMS} (30kHz BW) 90μs 45dB (or greater)

Figure 17.8.7: Filter die micrograph and data.

601 • 2005 IEEE International Solid-State Circuits Conference 0-7803-8904-2/05/\$20.00 ©2005 IEEE. Authorized licensed use limited to: University of Washington Libraries. Downloaded on December 3, 2009 at 17:03 from IEEE Xplore. Restrictions apply.		