A 12 bit 200 MS/s Zero-Crossing-Based Pipelined ADC With Early Sub-ADC Decision and Output Residue Background Calibration

Soon-Kyun Shin, Member, IEEE, Jacques C. Rudell, Senior Member, IEEE, Denis C. Daly, Member, IEEE, Carlos E. Muñoz, Member, IEEE, Dong-Young Chang, Member, IEEE, Kush Gulati, Member, IEEE, Hae-Seung Lee, Fellow, IEEE, and Matthew Z. Straayer, Member, IEEE

Abstract—A 12 bit 200 MS/s analog-to-digital converter (ADC) applies techniques of zero-crossing-based circuits as a replacement for high-gain high-speed op-amps. High accuracy in the residue amplifier is achieved by using a coarse phase in ZCBC followed by a level-shifting capacitor for fine phase. Sub-ADC flash comparators are strobed immediately after the coarse phase to achieve a high sampling rate. The systematic offset voltage between the coarse and fine phase manifests itself as systematic offset in the sub-ADC comparators. This offset is caused by the coarse phase undershoot and the fine phase overshoot. In this work, the offset is cancelled with background calibration by residue range correction circuits in the following stage’s sub-ADC. In addition, the sub-ADC’s random comparator offset is calibrated with a discrete-time charge-pump based background calibration technique. The reference buffer, bias circuitry, and digital error correction circuits are all integrated on a single chip. The ADC occupies an area of 0.282 mm² in 55 nm CMOS technology and dissipates 30.7 mW. It achieves 64.6 dB SNDR and 82.9 dBc SFDR at 200 MS/s for a FOM of 111 fJ/conversion-step. The SNDR degrades gracefully above the designed sampling frequency to 62.9 dB at 250 MS/s, and remains above 50 dB at 300 MS/s.

Index Terms—ADC, CMOS, 55 nm, pipelined, 12 bit, 200 MS/s, zero-crossing based circuits (ZCBCs).

I. INTRODUCTION

Analog-to-Digital converters (ADCs) are a fundamental building block in modern integrated circuits which serve to process and convert real-world analog signals into a format where digital signal processing and computation may take place. As CMOS processes continue to scale, the increased device cutoff frequency and the associated smaller parasitic capacitance allow more power-efficient and faster logic which improves the performance of the digital electronics, allowing more sophisticated and larger systems on a single chip. However, these same scaling properties fundamentally challenge the design of analog integrated circuits because of lower intrinsic transistor output resistance, lower power supply voltages, increased leakage currents, and higher device variability. In short, the intrinsic gain associated with a single-transistor stage $(g_{mre})$ decreases with finer geometry CMOS processes. Simultaneously, the available output swing is reduced due to the lower supply voltages which are mandated to address device reliability concerns. Thus, the design of high-gain, low-noise op-amps has become the main bottleneck in many switched-capacitor based circuits.

A parallel trend with respect to ADCs is the demand for higher resolutions and sampling rates. This is all set in the context of ever-present constraint on area and power consumption. Pipeline ADCs, given their area and power efficiency, are an excellent architecture to simultaneously achieve both high sampling rates and high resolution [1]–[5]. However, traditional pipelined ADCs require high-gain op-amps for accurate residue amplification. Recently, proposed calibration algorithms tune the closed-loop gain error using low-gain op-amps to overcome the incomplete settling due to the limited bandwidth, or poor linearity of the residue amplifier [6]–[8]. However, these methods frequently rely on foreground calibration algorithms, normally performed at power-on or during periods of converter inactivity, thus making any sudden environmental changes difficult to track during normal ADC operation. Conversely, background calibration can track offset variation in real time; however, this requires additional power and complexity, as well as potentially slower and less effective calibration results as compared with foreground algorithms. Zero-crossing-based circuits (ZCBCs) are an attractive alternative to op-amp switched capacitor circuits where the op-amp is replaced with a zero-crossing detector (ZCD) and a set of current sources [9]–[20]. A ring amplifier [21] was introduced as another alternate approach for op-amp-based circuit replacement in scaled technologies.

Compared with op-amp based circuits, the ZCBC method has theoretically shown to be more power-efficient because a virtual ground condition is detected by a circuit that fundamentally operates open loop, rather than utilizing a closed-loop op-amp in feedback to force a virtual ground [22]. However, while ZCBC
addresses many of the switched-capacitor (SC) gain stage shortcomings in nanometer technologies, achieving high accuracy amplification, at high speed, has been a significant challenge. For example, one previous ZCBC pipeline ADC implementation has achieved 10.5 bit ENOB but at speed 10 MS/s [13], and another has achieved 11.0 bit ENOB but at only 50 MS/s [15].

This paper describes in more detail the techniques introduced in [19] that allow higher speed ZCBC ADC operation with high resolution. These techniques include a unidirectional dual-ramp residue charging with correlated level-shifting capacitors, an early sub-ADC decision that relaxes the critical timing, and a residue range calibration technique. In addition, the sub-ADC’s comparator offset is calibrated in this work resulting in improved performance compared to [19]. Section II presents techniques of the ZCBC for high-speed and high-resolution ADCs, while Section III discusses the ADC implementation in detail. Measurement results are presented in Section IV, followed by conclusions in Section V.

II. ZCBCs FOR HIGH-PERFORMANCE ADCS

A. Linearity Challenges of High-Speed ZCBC

1) Dual Ramp ZCBC Architecture: Fig. 1 illustrates the basic differences between an op-amp based switched capac-
Fig. 2. Conceptual diagram of a ZCBC ramp. (a) Fast, slow ramp. (b) Dual ramp.

Fig. 3. Simplified schematic of ZCBC with series charging capacitor for fine phase current source and timing diagram with a small residue (dotted line) and a large residue (solid line).

Fig. 4. Effect of level shifting capacitor for the fine phase current source.

In ZCBC, the output ramp is typically generated by charging the capacitors with a current source. The nonlinearity associated with the current source creates an output-dependent overshoot variation which is analogous to the variation of the virtual ground voltage of the op-amp-based circuit with a finite op-amp gain. If the ZCD’s delay is zero, then the sample is taken precisely at the zero-crossing instant, and the sampled output voltage will be accurate. However in practice, the ZCD delay is finite, which results in an overshoot. The magnitude of the output voltage overshoot in ZCD circuits is a function of the output ramp slope \( (dV/dt) \) and the ZCD delay \( T_D \)

\[
V_{ov} = T_D \frac{dV}{dt}.
\]  

(1)

The ZCD overshoot, \( V_{ov} \), has two components: a constant component \( V_{ov1} \) and a signal-dependent component \( V_{ov2} \). The constant component \( V_{ov1} \) is easily corrected or tolerated in most circuits. The variable component \( V_{ov2} \) typically results from the nonlinearity of the output ramp. The current source’s finite output resistance as well as nonlinear parasitic capacitance at the output determines the ramp nonlinearity. If the \( T_D \) is signal-dependent, then this will also affect linearity, however, the \( T_D \) variation is small compared with the ramp nonlinearity. This can be explained by noting that the ZCD sees nearly the same ramp input at the same input common mode regardless of the output residue. Thus, we can treat \( T_D \) as a scalar that only depends on the time-constant of the ZCD.
Two options that reduce the amount of signal-dependent overshoot variation in ZCBC circuits are a current source with higher output resistance, or a faster ZCD. Improvements in the current source linearity can be achieved by using traditional output resistance enhancement techniques such as double or triple cascoding, and gain-boosted cascode current sources. To implement a faster ZCD, the transistors can be biased more aggressively with higher current densities. However, for both of these options, physical transistor properties pose a practical limit to how much improvement can be achieved for a reasonable power consumption.

A third option for reducing the signal-dependent overshoot variation is to lower the ramp rate. As shown in Fig. 2(a), a fast ramp creates larger overshoot as compared to a slow ramp. Therefore, in ZCBC circuits the dual ramp approach relaxes the requirement for the current source output resistance to allow simple cascode current sources [9], [11], [15]. The dual ramp approach consists of coarse and fine phases to create and maintain a slow-fine ramp as shown in Fig. 2(b). The final overshoot of the dual ramp is much smaller than that in a single ramp for a given sampling speed because of the slower fine ramp rate that minimizes the overshoot during this phase. Thus, the dual ramp approach significantly improves the linearity, typically at least proportionally to the reduction in the ramp rate.

In this design, a unidirectional dual ramp is adopted primarily because the fine current source can be turned on much earlier than in the bidirectional dual ramp [15]. This shortens the coarse phase duration, giving the fine current source more time to settle before a zero-crossing event without consuming additional power. In addition, this strategy reduces transient disturbances during the transition from the coarse to fine phase current ramps, ultimately enabling a shorter fine phase. Finally, a unidirectional ramp relaxes the output range requirements for the coarse ramp current source.

2) **Correlated Level Shifting for Fine Phase Current Source:** To improve the op-amp gain and increase output swing, a technique called correlated level shifting (CLS) has been proposed in prior art where a level shifting capacitor samples a coarse output voltage [23], [24]. A similar CLS technique was proposed in ZCBC’s [14], [19], [36]. Unlike the CLS in op-amp based circuits where settling must be interrupted to sample the coarse output voltage, this technique exploits the natural break in timing between the coarse and the fine phases. The coarse output voltage is sampled when the ZCD trips at the end of the coarse phase. Thus, there is no speed penalty for the CLS in ZCBC’s.

The top of Fig. 3 shows a simplified ZCBC schematic in the charge transfer phase with the level shifting capacitor \( C_{LS} \), the coarse current source \( I_1 \), the fine current source \( I_2 \), and switches for the fine phase current source. The two bottom-most plots in Fig. 3 show timing diagrams for the clock signals and waveforms illustrating two extreme cases of output residue voltages, one small and one large. The dotted line waveforms represent a small output residue and are denoted with a ‘S’ subscript, while
a solid line is used for the large output residue waveforms that have an “L” subscript.

It is clear that the differential input voltages to the ZCD ($V_X$) initially depend on the output residue voltage during the preset phase $\Phi_{SP}$. However, at the end of the coarse phase (on the falling edge of $E_1$), both the small and large residue ZCD input waveforms transition from a coarse ramp to a fine ramp at approximately the same undershoot voltage, $V_{us,S}$ and $V_{us,L}$, respectively. The ZCD input voltage is related to the output voltage by the capacitive divider formed by $C_A$ and $C_S$, at the end of the coarse ramp. Also, the output voltages $V_{OS}$ and $V_{OL}$ undershoot the final values ($V_{Ofinal,S}$ and $V_{Ofinal,L}$) by a relatively small and nearly constant amount, shown as $V_{FINE,S}$ and $V_{FINE,L}$. Both waveforms $V_{OS}$ and $V_{OL}$ then ramp in the fine phase and cross zero, and the $E_0$ signals end the charge transfer.

If the fine current source were applied to the output voltage directly, the current source would need to meet the linearity requirements over the entire output residue range, which is quite challenging. By using the CLS technique to connect the fine current source to the output voltage through a series capacitor, the current source output waveforms have a significantly reduced voltage range, as shown in the plot of $V_{LS}$ at the very bottom of Fig. 3. In this case, the maximum output range of the current source is limited to $V_{LS_{final}}$, which is a fraction of the overall residue range. In addition to the reduced range seen by the current source that makes high output impedances straightforward to implement, the variation of output voltage at the current source drain is also drastically reduced.

This concept is further illustrated in Fig. 4 for a PMOS cascode fine ramp current source. Without CLS, the variation in the voltage at the current source output is shown as $\Delta V_{Ofinal}$. With CLS, the voltage trajectory is nearly constant, resulting in near-constant overshoot that is limited by the precision of the coarse phase ($\Delta V_{LS_{final}}$). By way of explanation, after the coarse phase the incomplete settling coupled with the coarse current source’s output resistance, result in slightly different undershoot voltages $V_{us,S}$ and $V_{us,L}$ at the ZCD input. These different undershoot voltages change the amount of voltage provided by the fine ramp $V_{FINE}$, which results in slightly different final voltages $V_{LS_{final,S}}$ and $V_{LS_{final,L}}$ at the zero-crossing instant. Although this figure exaggerates the nonlinearity for purposes of illustration, simulations indicate a linearity improvement of approximately 30 dB by using a fine current source with CLS compared with the variation of a current source without level shifting. CLS therefore allows the same current source to be operated in a way that is much less sensitive to the data-dependent output residue voltage.

Note that there is a capacitive voltage divider between the fine current source output $V_{LS}$ and the output $V_{OUT}$ of corresponding stage. The voltage division ratio is proportional to $C_{LS}$ for small values of $C_{LS}$, and the ratio approaches unity for very large $C_{LS}$. While a small value of $C_{LS}$ has less capacitive loading of the coarse ramp, the fine current source output range is increased and the fine ramp linearity is accordingly degraded. In this design, the size of $C_{LS}$ was selected through simulation to achieve good fine current source linearity by maintaining a modest range for $V_{LS}$ while also balancing the impact of the increased capacitance during the coarse ramp.
B. High-Speed Technique

High speed with ZCBC pipelined ADC’s are challenging because preset, coarse, fine, and sub-ADC decision phases for the dual ramp architecture must be finished within a half clock cycle while maintaining ramp linearity. Here we describe how the following stage’s sub-ADC decision can be made in parallel with the fine phase ramp to relax the timing constraints.

1) Early Sub-ADC Decision: In Fig. 5, the gain stage timing diagram for the proposed early sub-ADC decision are compared with previous ZCBC designs [11], [15] that make the sub-ADC decision after the fine phase. It is clear that, if the following stage sub-ADC decision can be made in parallel to the fine ramp phase, the sub-ADC delay, which takes up 20% of the charge transfer phase, can be removed from the critical timing path in the half-clock period. This allows the sub-ADC design to be relaxed, resulting in a lower-power design with more time to resolve metastability. In addition, the second stage has more time available for charge transfer, which allows for a reduced bandwidth and lower power implementation of stages 2–4. In this work, the sub-ADC decision is moved to just after the coarse phase which saves approximately 400 ps of time (20% of the available half clock period).

Fig. 6 illustrates waveforms for the residue output voltage and the ZCD input voltage for a single sample. \(V_{o1}\) is the output voltage at the end of the coarse ramp phase, which is the voltage that is sampled for the early sub-ADC decision. \(V_{o2}\) is the output voltage at the end of the fine phase after the zero crossing decision that is sampled by the following pipeline stage. Since there is a voltage difference between \(V_{o1}\) and \(V_{o2}\), the sub-ADC must be able to compensate in some way for the voltage difference between the coarse and fine phase output voltages. However, we have already noted in the previous section that in the dual ramp approach there is a nearly constant voltage difference between the coarse and fine phase output voltage. Thus, the voltage difference appears as a fixed systematic offset voltage on all the sub-ADC comparators.

Fig. 7(a) shows the nominal MDAC residue without offset in the sub-ADC decision. The nominal output residue range is from \(-V_{REF}/2\) to \(+V_{REF}/2\) with a stage gain of 4. However, because the sub-ADC decision is made immediately after the coarse decision phase, the output voltage seen by the sub-ADC is lower than the final output by a constant amount, \(V_{FINE}\). This effectively corresponds to a systematic offset on all sub-ADC comparators which causes the residue to shift up as shown in...
Fig. 7(b). In the gray area of Fig. 7(b), the residue extends outside its nominal range. This cuts into the digital error correction range and degrades the available headroom of the coarse current source. To remove this overshoot in the residue voltage, a calibrated systematic offset voltage, $V_{\text{OFFSET}}$, is added to all sub-ADC comparator inputs. This approach keeps the MDAC residue within the nominal range while retaining the speed advantage of early sub-ADC decisions. The offset depends on the ramp rate and ZCD delay, necessitating calibration.

2) Residue Range Background Calibration: As discussed in the previous section, $V_{\text{OFFSET}}$ is a function of the fine ramp rate and ZCD delay, which depend on process, voltage, and temperature. A slow ramp or a fast ZCD delay generates smaller $V_{\text{OFFSET}}$, and conversely a fast ramp or a slow ZCD delay results in bigger $V_{\text{OFFSET}}$. Thus, it requires background calibration to track those changes. Note that the calibration of the offset of the sub-ADC decisions reduces the residue range and improves the linearity.

One possible method to implement the background calibration is to change $V_{\text{OFFSET}}$ in the sub-ADC in the $N$th stage according to the error signal generated from the sub-ADC, in the $N+1$th stage. Fig. 8 shows three cases of residues of $N$th stage that are too low, normal, and too high. A residue voltage of $N$th stage which is either too low, normal, or too high, can be detected using the comparators of the $N$th stage with reference voltages $V_{\text{TOO_LOW}}$ and $V_{\text{TOO_HIGH}}$; shown in Fig. 9. Whenever these threshold voltages are exceeded, an accumulator is incremented or decremented. The accumulator output $D_{\text{OFFSET}}$ is fed back to the reference generation block in the $N$th stage of the sub-ADC, which shifts the reference voltages of the sub-ADC by a systematic offset. This background calibration causes the output residue range to converge to the desired nominal range after several hundred sampling clock periods. A similar residue background calibration was recently proposed in [37]. The realization of the systematic offset generator circuit will be discussed in detail in Section III.
III. CIRCUIT IMPLEMENTATION

A. Architecture

A top-level block diagram of the ADC is depicted in Fig. 10. The ADC consists of four ZCBC stages and a final 4 bit flash. The first stage is composed of a 3.2 bit sub-ADC (eight comparators) and an MDAC with gain of 4. Each of the subsequent stages is scaled down by a factor of 2 relative to the preceding stage except for the fourth stage which is not scaled. The standard redundancy for over range protection is used to relax offset constraints in both the sub-ADC comparators and the residue amplification, and to fold the residue to within $V_{	ext{REF}}/2$ to $-V_{	ext{REF}}/2$. The reference buffer, bias circuits, offset calibration circuits, and digital error correction circuits are all implemented on chip. Since the circuit achieves sufficient charge transfer accuracy as well as capacitor matching at the 12 bit level, linearity calibration is unnecessary, and was not implemented.

B. Pipeline Stages of the ZCBC

A simplified schematic of a ZCBC pipelined ADC stage is shown in Fig. 11, where each stage has a sub-ADC, switch block SW, reference presampling capacitors $C_{R}^{\pm}$, a ZCD, coarse and fine current sources, level shifting capacitors $C_{L}^{\pm}$, sampling capacitors $C_{S}^{\pm}$, and amplification capacitors $C_{A}^{\pm}$.

Reference voltage ringing is a key challenge for all high-speed ADCs due to the inherent bondwire and package inductance when switching occurs. To allow more time for reference settling, the reference voltage is precharged to sampling capacitors.
over an entire half-clock period. This charge is then subsequently added or subtracted during the charge transfer phase based on the sub-ADC’s output using switches SW. With the proposed reference precharge architecture there is approximately a factor of 1.8 penalty in noise gain compared to a conventional architecture. To compensate for this increased noise, additional power is spent to reduce the input referred noise contribution of the ZCD. A similar reference precharging architecture with reduced noise gain penalty was recently reported in [20].

A timing diagram of the charge transfer phase is shown in Fig. 12. The input and reference voltages are sampled on \( C_{S+} \) and \( C_{R\pm} \) during the sampling phase (\( \Phi_1 \)), respectively. In the charge transfer phase (\( \Phi_2 \)), the sub-ADC’s decision is applied to SW such that \( C_{R\pm} \) connects to the sampling capacitor \( C_{S\pm} \) to subtract the proper amount of charge. In the preset phase (\( P_n \)), a short preset pulse \( \Phi_2P \) sets \( V_{OUT+} \) to \( V_{SS} \), and sets \( V_{OUT-} \) to \( V_{DD} \). This ensures the ZCD differential input voltage starts from a negative value at the beginning of the coarse phase (\( P_1 \)). At the beginning of the preset phase, the coarse phase control signal \( E_1 \) and the fine phase control signal \( E_{2D} \) turn on at the same time, to reduce the transient effects, as a result of the coarse and fine phase current sources turning on and off. \( E_1 \) also sets \( V_{LS+} \) to \( V_{SS} \), and sets \( V_{LS-} \) to \( V_{DD} \), until the coarse phase ends.

After the preset pulse \( \Phi_2P \) turns off, the coarse phase begins by the coarse current \( I_1 \) charging \( V_{OUT+} \) and discharging \( V_{OUT-} \) at a fast rate. An intentional offset voltage for the coarse ZCD threshold is introduced to result in an undershoot voltage at the ZCD input of \( V_{us} \). At this time, the sub-ADC in the next stage converts the coarse output voltage \( V_{O1} \) to a digital output. After the coarse phase, \( E_2 \) disconnects the \( V_{LS+} \) node from \( V_{SS} \), and the \( V_{LS-} \) node from \( V_{DD} \), so that the fine current \( I_2 \) begins to charge \( V_{OUT+} \) and discharge \( V_{OUT-} \) through \( C_{LS\pm} \) at a slow rate. When \( V_{X+} \) crosses \( V_{X-} \), the sampling signal \( E_3 \) falls to open the sampling switches. The output voltage \( V_{O2} \) is accurately sampled on the next stage capacitors \( C_{G\pm} \) and \( C_{A\pm} \) at this instant. After a short delay, \( E_{2D} \) turns off the fine current sources.

Because the ZCD has a finite delay, a sample is taken shortly after \( V_{X+} \) crosses \( V_{X-} \). This delay combined with the fine phase ramp rate, produces a nearly constant overshoot. Fig. 13 shows the trajectories of simulated waveforms at the output of the MDAC stage, level shifting node, and input voltage of the ZCD within a half clock cycle. Fig. 14 shows the comparison of simulated output waveforms of a small and large residues at \( V_{O1\_T+} \). The offset voltage, \( V_{F\_N\_E} \), is the difference between the coarse and fine output voltages which remain almost constant. After the fine phase, both \( V_{LS+} \) and \( V_{LS-} \) are pulled up to \( V_{DD} \), to prevent \( C_{LS\pm} \) from floating during the next sampling phase.

Fig. 15 shows the simulated residue voltages resulting from the background residue calibration. This simulation was performed by sweeping the temperature from \(-40^\circ C \) to \( 125^\circ C \) and varying the power supply voltage from 0.9 to 1.1 V. The ADC is initiated at 0.5 \( \mu s \) at which time calibration begins. Fig. 15 shows the residue range converging in around 1.0 \( \mu s \),
which is approximately 200 cycles of sampling clock period. The output residue converges well within the nominal residue range as calibration runs in the background. Note that the calibration values are stored in digital registers and therefore can be held indefinitely regardless of the input signal statistics or activity.

C. Sub-ADC

The basic sub-ADC used in all four gain stages consists of two reference resistor ladders and eight switched-capacitor comparators to realize a nine level (3.2 bit) flash sub-ADC. For each sub-ADC in stages 2–4 that follow a ZCBC, there are two additional comparators to detect if the residue is either too high or too low for the residue background calibration.

In a traditional sub-ADC without an offset voltage, bipolar threshold voltages can be generated from a single resistor ladder. However, in this case the threshold voltages for each polarity are equal in magnitude. Here, we require a constant and systematic offset voltage $V_{\text{OFFSET}}$ to compensate for the early sub-ADC decision. Fig. 16 then shows the reference ladder modifications that generate the differential threshold voltages of the sub-ADC comparators including the $V_{\text{OFFSET}}$ term.

In Fig. 16, two reference voltages $(V_{\text{REF}} - V_{\Delta}, V_{\text{REF}} + V_{\Delta})$ are applied to two parallel resistor ladders. The positive terminals for the threshold voltages are tapped from the first ladder at fractional values of $(V_{\text{REF}} - V_{\Delta}) \ast \{7/8, 6/8, 5/8, \ldots\}$, and the negative terminals for the threshold voltages are tapped from the second ladder at fractional values of $(V_{\text{REF}} + V_{\Delta}) \ast \{1/8, 2/8, 3/8, \ldots\}$. In this way, the full $V_{\Delta}$ is seen in each of the eight differential threshold voltages such that the differential reference voltage of the $i$th comparator $\{i \in \{1, 2, \ldots, 8\}\}$ is given by

\[(V_{\text{REF}} - V_{\Delta})\frac{i}{8} - (V_{\text{REF}} + V_{\Delta})\frac{9 - i}{8}\]

\[= (V_{\text{REF}})\frac{2i - 10}{8} - V_{\Delta}. \tag{2}\]

For example, the eighth comparator threshold is

\[(V_{\text{REF}} - V_{\Delta})\frac{7}{8} - (V_{\text{REF}} + V_{\Delta})\frac{1}{8} = (V_{\text{REF}})\frac{6}{8} - V_{\Delta}. \tag{3}\]
When compared with the nominal threshold voltage for a traditional nine-level sub-ADC of $7/8 \ V_{\text{REF}}$, we find that $V_{\text{OFFSET}} = V_\Delta + V_{\text{REF}}/8$. The choice to include an offset of $V_{\text{REF}}/8$ in all the thresholds was made to relax headroom issues on the lower supply voltage and to bring the resistor ladders closer to differential operation.

Fig. 17 shows the schematic of the offset reference voltage generation circuit (ORVGC). It consists of a two-stage op amp and a current steering DAC ($M_{10-12}$) added to the output stage. ORVGC forces currents, $I_1 + I_C$, on $V_{O_+}$, and $I_S - I_C$ on $V_{O_-}$, where $I_S = I_1 - I_0 - I_2 + I_3 - I_C$. $\Delta$OFFSET code controls $I_C$. The average voltage ($V_{\text{RCM}}$) of the top side of the two resistor ladders is feedback to the inverting input op-amp and changes $I_1$. Thus, $V_{\text{RCM}}$ becomes $V_{\text{REF}}$ with this common mode feedback and these different output currents from ORVGC generate $V_{\text{REF}} + V_\Delta$ on $V_{O_+}$, $V_{\text{REF}} - V_\Delta$ on $V_{O_-}$ through $R_{CM}$, where $V_\Delta = I_{HCM} R_{CM}$. Thus, new reference voltages are generated on top of the resistor ladders which are then provided to all the comparators in the sub-ADC with shifted reference voltages.

D. Sub-ADC Comparator

In [19], it was found that random offset in the gain stage’s sub-ADC comparators increased the residue range, which then increased the charge transfer nonlinearity. Offsets in the final stage FLASH quantizer degraded the noise floor and DNL. To reduce these offset voltages, large devices can be used. However, to reduce offset significantly, the devices must be scaled by a large factor and this either increases power or limits the bandwidth and speed. Alternatively, offset calibration may be employed by adding extra capacitance with digital control at the comparator outputs [25] or with self-calibration [26].

In this design, a discrete-time charge-pump based background calibration technique is used to adjust the comparator’s offset every cycle. The comparator offset voltage calibration circuit is shown in Fig. 18 with the corresponding timing diagram. At the beginning of the reference sampling phase, $\Phi_4$ goes high for a brief time to short the input of the comparator for offset calibration. If the comparator input has a positive offset voltage then the comparator output will be high. Likewise, if the comparator input has a negative offset voltage, then the comparator output will be low. The result of this comparison is used to update the offset calibration every clock cycle. Fig. 18(c) shows the simulated waveforms of the comparator offset calibration, where $V_{\text{XR}}$ and $V_{\text{XR'}}$ converge to a $V_{\text{COMP OFFSET}}$ value of 50 mV. This 50 mV corrects for a forced differential offset voltage of the opposite magnitude at the comparator input in the simulation. A calibration voltage $V_{\text{XR'}}$ is applied to the inverting input of the auxiliary differential pair ($V_{\text{RM}}$ in Fig. 19). With the main input shorted, the voltage $V_{\text{XR'}}$ is incremented by the charge pump if the comparator output is “1” and decremented if the comparator output is “0”. After a few clock cycles, the voltage $V_{\text{XR'}}$ converges to a value that cancels the comparator offset. The current $I_{\text{CP}}$ in the charge pump is designed such that the voltage ripple on $V_{\text{RM}}$, after convergence, is much less than the sub-ADC’s LSB.

E. Zero-Crossing Detector

The ZCD senses zero crossing of $(V_{X^+}) - (V_{X^-})$ in both the coarse and fine phases. At the end of the fine phase, the ZCD toggles $E_2$ which turns off the sampling switch in the following stage, thereby completing the charge transfer as illustrated in Fig. 11. The ZCD consists of a main pre-amplifier ($M_{S1-2}$, $M_{F1-2}$, $M_{1-2}$, $M_{1-4}$), a coarse threshold detector ($M_{C1-2}$, $M_{C1-4}$), a fine threshold detector ($M_{F1-2}$, $M_{F1-4}$), and simple digital logic to create the appropriate timing signals as shown in Fig. 20. PMOS input pairs are chosen in the preamplifier to accommodate a low input common-mode level. To generate an undershoot voltage in the coarse phase for the uni-directional two-phase operation, an intentional offset is introduced between $M_{C1-2}$ and $M_{C1-4}$. The coarse phase offset is set to ensure the coarse phase sufficiently undershoots regardless of process, voltage, and temperature corners. The noise of the ZCD is mainly determined by the preamplifier because the noise associated with the coarse and fine detectors are reduced by the preamplifier open-loop gain.
Due to the dynamic operation of the core ZCBC, the power consumption is proportional to the sampling rate [12], with the exception of the bias circuitry which consumes a small amount of static power. In the preamplifier, $M_{S1}$ provides a small amount of bias current for a faster turn-on transient, while the larger $M_{S2}$ only turns on during the coarse and fine phases. As soon as $V_d$ goes low, $M_{S2}$ is turned off to save power. To reduce the power consumption at lower sampling frequencies, the ramp currents $I_1$ and $I_2$, as well as the ZCD bias current are designed to scale with the sampling clock frequency, and track the primary current generated from a master bias control circuit.

IV. MEASUREMENT RESULTS

The ADC was fabricated in a 55 nm CMOS process, with six metal layers, one poly layer, and MOM capacitors. Fig. 21 shows a die photograph of the ADC, occupying an area of 0.282 mm$^2$. The ADC operates from 1.1 V power supply. The measured spectrum of the ADC with input frequency of 10.1 MHz at 200 MS/s is shown in Fig. 22. The SNDR is 64.6 dB (10.44 ENOB), and the SFDR is 82.9 dBc. The SNDR and SFDR of the ADC at various input frequencies are plotted in Fig. 23. SNDR degrades gradually as the input frequency increases due to the clock jitter. Fig. 24 shows SNR (dBFS), SNR (dBc) versus the input amplitude with 99.9 MHz input frequency. DNL and INL are $+0.24$/$-0.28$ LSB and $+1.36$/$-1.89$ LSB, respectively; shown in Fig. 25. Table I shows the ADC performance summary. The total ADC power consumption, which includes the on-chip reference buffer power of 5.3 mW and digital power of 1 mW, is 30.7 mW, resulting in a figure of merit ($FOM = (P^2)/((2^{ENOB} \cdot F_S))$) of 111 fJ/conversion-step. The measured SNDR and power consumption versus sampling frequency are shown in Fig. 26. To achieve an optimal power consumption vs. sampling frequency, the primary current generated from a master bias control circuit...
is designed to scale with the sampling clock frequency. Since the ramp currents $I_1$ and $I_2$ track the master bias current, at lower sampling rates the ramp rate is reduced to take advantage of the increased time available for the charge transfer. As the sampling rate increases, the time variation associated with the second phase zero crossings becomes a larger fraction of the overall half clock period. Eventually, this leads to a higher percentage of zero-crossings failing to occur within the time provided by a half clock period, and the accuracy is significantly reduced as seen in Fig. 26. Conversely, at low sampling rates,
the SNDR is limited by the noise. Note the SNDR is almost flat up to 250 MS/s before degrading gradually. The SNDR is 62.9 dB at 250 MS/s. The power consumption is approximately proportional to the sampling frequency. The SNDR remains above 50 dB even at 300 MS/s.

Compared to the DNL results in [19] of +1.16/−0.72 LSB, the DNL in this work is improved significantly to +0.24/−0.28 LSB, by applying the charge pump based calibration technique to sub-ADC’s comparators. The SNDR is improved from 63.7 dB to 64.6 dB at low input frequencies and from 62.5 dB to 63.2 dB at the Nyquist input frequency of 200 MS/s. SFDR is improved from 76.6 dBc to 82.9 dBc. The FOM has a modest improvement from 114 fJ/step to 111 fJ/step with a slight increase in the overall ADC power consumption. At the higher sampling frequency, for example 250 MS/s, the ADC SNDR improves from 58.7 dB as compared to 62.9 dB in [19].

Table II compares the measurements of recently reported ADCs with resolution 12 bits and higher, while Fig. 27 shows graphical comparison of this work relative to similar previously published converters [27]. Although there are many ADCs with a FOM less than 100 fJ/conversion-step for lower speeds (<100 MS/s), few ADCs achieve this FOM at higher speeds (>100 MS/s). As Table II and Fig. 27 show, this ADC achieves the best figure of merit among ADCs with no off-chip components (e.g., off-chip reference buffers and calibration circuits), and sampling rates of 200 MS/s and higher.

Table II

<table>
<thead>
<tr>
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<td>IS1CC 2006[28]</td>
<td>14</td>
<td>100</td>
<td>130 nm</td>
<td>66.0</td>
<td>-</td>
<td>224.0</td>
<td>1373.8</td>
</tr>
<tr>
<td>IS1CC 2008[30]</td>
<td>14</td>
<td>100</td>
<td>180 nm</td>
<td>72.2</td>
<td>88.5</td>
<td>230.0</td>
<td>690.8</td>
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<tr>
<td>IS1CC 2009[31]</td>
<td>14</td>
<td>100</td>
<td>90 nm</td>
<td>68.8</td>
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<td>130.0</td>
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<tr>
<td>VLSI 2008[29]</td>
<td>14</td>
<td>100</td>
<td>90 nm</td>
<td>70.0</td>
<td>80.0</td>
<td>250.0</td>
<td>967.4</td>
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<tr>
<td>VLSI 2010[13]</td>
<td>12</td>
<td>100</td>
<td>90 nm</td>
<td>63.2</td>
<td>74</td>
<td>6.2</td>
<td>52.7</td>
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<tr>
<td>IS1CC 2009[3]</td>
<td>16</td>
<td>125</td>
<td>180 nm</td>
<td>78.6</td>
<td>92.0</td>
<td>385.0</td>
<td>532.3</td>
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<td>VLSI 2008[32]</td>
<td>13</td>
<td>250</td>
<td>180 nm</td>
<td>65.9</td>
<td>77</td>
<td>140.0</td>
<td>347.4</td>
</tr>
<tr>
<td>JSSC 2009[33]</td>
<td>12</td>
<td>200</td>
<td>90 nm</td>
<td>59.4</td>
<td>-</td>
<td>186.0</td>
<td>1220.0</td>
</tr>
<tr>
<td>VLSI 2013[35]</td>
<td>12</td>
<td>200</td>
<td>65nm</td>
<td>65</td>
<td>82</td>
<td>11.5</td>
<td>39.6</td>
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<tr>
<td>CICC 2012[19]</td>
<td>12</td>
<td>200</td>
<td>55 nm</td>
<td>63.7</td>
<td>76.1</td>
<td>28.5**</td>
<td>114.0**</td>
</tr>
<tr>
<td>This work</td>
<td>12</td>
<td>200</td>
<td>55 nm</td>
<td>64.6</td>
<td>82.9</td>
<td>30.7**</td>
<td>111.0**</td>
</tr>
</tbody>
</table>

*: Reference buffer and digital calibration engine powers are excluded.

**: Reference buffer and all digital powers are included.

V. CONCLUSION

A 12 bit 200 MS/s ZCBC pipelined ADC which exploits an early sub-ADC decision after the coarse phase, to maximize charge transfer time has been presented in this paper. The systematic offset voltage between coarse and fine phases is calibrated by a residue range calibration technique. A level shifted fine phase current source is also adopted for higher accuracy.
by reducing the signal dependency of the fine current source. Random offsets in the sub-ADC comparators are removed by background offset calibration through a charge-pump circuit. The ADC includes all necessary ancillary circuits including bias circuitry, a reference buffer, offset calibration circuits, and digital error correction logic. The linearity calibration is unnecessary due to sufficient accuracy in charge transfer and capacitor matching. This work represents the highest speed 12 bit ZCBC ADC to date. With the ramp rate and bias current designed to track the sampling rate, the ADC remains functional at frequencies well over the maximum design frequency and the performance degrades gracefully up to 350 MS/s. The circuit demonstrates that ZCBC’s provide broad sampling rate tunability with the power consumption approximately proportional to the sampling rate.

REFERENCES


[16] Soon-Kyun Shin (S’10–M’14) received the B.S. degree in electrical engineering and M.S. degree in electronic and electrical engineering from the Konkuk University and the Sungkyunkwan University, Seoul, Korea, in 1997 and 2006, respectively, and the Ph.D. degree in electrical engineering from the University of Washington, Seattle, WA, USA, in 2014.

[17] From 1997 to 2009, he was a Design Engineer with Samsung Electronics, Yongin, Korea, designing mixed-signal circuits for ASIC and SoCs. From 2006 to 2007, he was a Visiting Scientist with the Massachusetts Institute of Technology, Cambridge, MA, USA, where he worked on low-power zero-crossing-based ADC. In 2010, he joined Cambridge Analog Technologies (CAT), Billerica, MA, USA, where he worked on high-performance ADCs. In 2011, CAT was acquired by Maxim Integrated, where he has been a Senior Member of Technical Staff working on low-power high-performance ADCs. He holds nine U.S., two Chinese, one German, two Taiwanese, and four Korean patents.

[18] Dr. Shin is a recipient of the Samsung Electronics’ scholar program for the M.S. degree and received the Best Paper Award from Samsung Electronics in 2005.
Jacques C. Rudell (S’94–M’00–SM’09) received the B.S. degree from the University of Michigan, Ann Arbor, MI, USA, and the M.S. and Ph.D. degrees from the University of California, Berkeley, CA, USA, all in electrical engineering.

After completing his degrees, he worked for several years as an RF IC Designer with Berkana Wireless (now Qualcomm) and Intel Corporation. In January 2009, he joined the faculty at the University of Washington, Seattle, WA, USA, as an Assistant Professor of electrical engineering. His research interests include topics in RF and millimeter-wave integrated circuits design for communication systems, in addition to biomedical electronics for imaging and neural interface applications.

Dr. Rudell was the recipient of the Demetri Angelakos Memorial Achievement Award while at the University of California, which is a citation given to one student per year by the EECS Department. He has twice been corecipient of the Best Paper Award at the International Solid-State Circuits Conference, the first of which was the 1998 Jack Kilby Award, followed by the 2001 Lewis Winner Award. He received the 2008 ISSCC Best Evening Session Award and was corecipient of the 2011 RFIC Symposium Best Student Paper Award. He served on the ISSCC technical program committee (2003–2010), and on the MTT-IMS Radio Frequency Integrated Circuits (RFIC) Symposium steering committee (2002–2013), where he was the 2013 General Chair. He currently serves as an associate editor for the IEEE Journal of Solid-State Circuits (2009–present).

Denis C. Daly (S’02–M’09) received the B.A.Sc. degree in engineering science from the University of Toronto, Toronto, ON, Canada, in 2003, and the S.M. and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2005 and 2009, respectively.

Since August 2011, he has been a Senior Member of the Technical Staff with Maxim Integrated, Chelmsford, MA, USA, where he has been designing low-power, high-performance analog circuits including ADCs and PLLs. From January 2010 until August 2011, he was with Cambridge Analog Technologies, Billerica, MA, USA, which was acquired by Maxim Integrated. From May 2005 to August 2005 he worked in the Wireless Analog Technology Center, Texas Instruments, Dallas, TX, USA, designing transceiver modules. From May 2003 to August 2003, he worked on high-speed signaling systems at Intel Laboratories, Hillsboro, OR, USA.

Dr. Daly was a corecipient of the 2009 ISSCC Jack Kilby Award for Outstanding Student Paper and the 2006 DAC/ISSCC Student Design Contest (Operational System Category) and was awarded a Student Paper Prize at the 2006 RFIC Symposium. He received Natural Sciences and Engineering Research Council of Canada (NSERC) Postgraduate Scholarships in 2003 and 2005.

Carlos E. Munoz (M’95) received the B.S. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 1994. From 1994 to 2001, he was with Crystal Semiconductor/Cirrus Logic, Austin, TX, USA, and Nashua, NH, USA, working on various analog-to-digital converters for industrial measurements. From 2001 to 2005, he worked on DLLs, ADCs, and DACs for wireless applications at Engim Inc., a startup in Acton, MA, USA. From 2005 to 2008, he helped develop software-defined radios at BitWave Semiconductor, Lowell, MA, USA. From 2008 to 2011, he helped cofound Cambridge Analog Technologies Inc., Billerica, MA, USA, where he developed zero-crossing based analog-to-digital converters. In 2011, Cambridge Analog Technologies was acquired by Maxim Integrated Products, and he joined Maxim Integrated, North Chelmsford, MA, USA, as a Senior Principal Member of the Technical Staff to lead several developments in low-power, high-performance analog-to-digital converters for industrial, medical, and wireless applications. He is a coauthor on several VLSI and CICC papers and main inventor and coinventor on several patents.

Mr. Munoz is coauthor of a paper presented at the recent 2014 ISSCC on low-power, high-performance zero-crossing based ADCs.

Kush Gulati (M’13) received the B.S. degree in electronics and communication engineering from Delhi Institute of Technology (now NSIT), New Delhi, India, the M.S. degree in electrical and computer engineering from Vanderbilt University, Nashville, TN, USA, and the Ph.D. degree in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA. His doctoral research at MIT was directed towards the design of a low-power reconfigurable analog-to-digital converter. From 1993 to 1995, he worked on circuit techniques for minimizing susceptibility of DRAMs to alpha particles and cosmic ions.

He has a combined experience of more than 21 years in the areas of high-performance analog circuit design including analog-to-digital converters. In 2007 he cofounded Cambridge Analog Technologies, Inc. (CAT), Billerica, MA, USA, where he led the company as President and CEO. CAT was focused on a revolutionary ultra-low power technology including high-speed data converters; In August 2011, CAT was acquired by Maxim Integrated, Chelmsford, MA, USA, where he is now Executive Director and General Manager of the Advanced IP Solutions Group. Prior to cofounding CAT, in 2001, he helped cofound Engim Inc., a wireless communications startup based in Acton, MA, USA, where he led their mixed-signal/analog group developing high-speed and high-resolution data converters. Between 2005 and 2007, he was with Bitwave Semiconductor, a startup developing wireless handhelds based on software-defined radio techniques, based in Lowell, MA, USA, where he was the Director of analog and mixed-signal development. He has authored or coauthored numerous publications and patents in the area of circuit design.

Dr. Gulati has served on the Technical Program Committee of the VLSI Circuits Symposium and the SDR Forum. While at MIT, he received the Maxim Integrated Products Fellowship and the Analog Devices Outstanding Student Designer Award.

Dong-Young Chang (S’00–M’04) received the B.S. and M.S. degrees in electronic engineering from So-gang University, Seoul, Korea, and the Ph.D. degree in electrical and computer engineering from Oregon State University, Corvallis, OR, USA, in 1995, 1997 and 2002, respectively.

He joined Samsung Electronics, Kicheung, Korea, in 1997, where he was engaged in the design of analog front-end systems for CCD/CMOS image sensors and LCD displays. During the summer of 2002, he was with Lucent Technologies, Bell Laboratories, Allentown, PA, USA, where he investigated various low-voltage data converters. From 2003 to 2005, he was with Texas Instruments, Tucson, AZ, USA, working on low-power high-speed ADC products. In 2005, he was with Engim Inc., Acton, MA, USA, as a Senior Design Engineer. From 2005 to 2010, he was with BitWave Semiconductor, Lowell, MA, USA, as a Director of RF and AMS design team working on Programmable Wireless Transceivers. In 2010, he joined Cambridge Analog Technologies, Billerica, as a Senior Scientist and Director working on high-performance and low-power data converter products. Since August 2011, he has been a Principal Member of the Technical Staff with Maxim Integrated, San Jose, CA, USA, designing low-power, high-performance ADCs. He holds three U.S. patents.

He has received Outstanding Student Paper Award by IEEE Solid-State Circuits Seoul Chapter in 1998 and Outstanding Student Designer Award by Analog Devices in 2000.
Hae-Seung Lee (F’96) received the B.S. and M.S. degrees in electronic engineering from Seoul National University, Seoul, Korea, in 1978 and 1980, respectively, and the Ph.D. degree in electrical engineering from the University of California, Berkeley, CA, USA, in 1984, where he developed self-calibration techniques for A/D converters. Since 1984, he has been on the faculty in the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, USA, where he is now a Professor and the Director of Center for Integrated Circuits and Systems. He has acted as Consultant to Maxim Integrated, Analog Devices, Inc., Wilmington, MA, USA, and MIT Lincoln Laboratories. He has served the Technology Advisory Committee for Samsung Electronics, Cypress Semiconductor, and Sensata Technologies. He also co-founded SMal. Camera Technologies, Inc., and Cambridge Analog Technologies, Inc. His research interests are in the areas of analog integrated circuits with the emphasis on analog-to-digital converters in scaled CMOS technologies.

Prof. Lee was a recipient of the 1988 Presidential Young Investigators’ Award and a corecipient of the ISSCC Jack Kilby Outstanding Student Paper Award in 2002 and 2006. He has served a number of technical program committees for various IEEE conferences, including the International Electron Devices Meeting, the IEEE International Solid-State Circuits Conference, the IEEE Custom Integrated Circuits Conference, and the IEEE Symposium on VLSI circuits. He is an elected AdCom member and Treasurer of the IEEE Solid-State Circuits Society.

Matthew Z. Straayer (M’11) received the B.S. and M.S. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2000 and 2001, respectively, and the Ph.D. degree in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2008. From 2001 to 2003, he was with Integrated Sensing Systems, Ypsilanti, MI, USA, designing signal processing and converter circuits for wireless medical and industrial MEMS sensors. From 2003 to 2008, he was on staff with MIT’s Lincoln Laboratory, Lexington, MA, USA, working on next-generation RF technologies including low-power transceivers and low-noise frequency synthesizers. In 2008 he helped to cofound Cambridge Analog Technologies, Inc. (CAT), Billerica, MA, USA, where he led the technical development of zero-crossing circuits for high performance analog-to-digital converters. In 2011 CAT was acquired by Maxim Integrated, Chelmsford, MA, USA, where he manages the design activities for the Advanced IP Solutions team. He has authored or coauthored numerous publications and patents.

Dr. Straayer currently serves on the ISSCC data converter technical program committee. He has also served on the Steering Committee of the IEEE MTT-S International Microwave Symposium (IMS). At MIT, he received support from the Lincoln Scholars Program and was selected for the Analog Devices, Inc. Outstanding Student Designer Award.