

# A Transformer-Feedback Based Wideband IF Amplifier and Mixer for a Heterodyne 60 GHz receiver in 40 nm CMOS

Venumadhav Bhagavatula<sup>1</sup>, Michael Boers<sup>2</sup> and Jacques C.Rudell<sup>1</sup>

<sup>1</sup>Dept. of Electrical Engineering, Univ. of Washington, Seattle, WA, 98195 USA

<sup>2</sup>Broadcom Corporation, Irvine, CA, 92617, USA

**Abstract** — This paper presents a wideband Intermediate Frequency (IF) amplifier and downconverter implemented for a 60-GHz receiver in a standard CMOS 40nm process. A Source-Gate Transformer-Feedback based cascode IF amplifier with a flat passband response over a frequency range of 11 GHz to 13 GHz is presented. An on-chip Lange Coupler is used to generate quadrature (I/Q) Local Oscillator (LO) signals. The I/Q downconverter employs a three-winding transformer to couple the transconductance ( $G_m$ ) stage with the I and Q switching stages. Measured results show a peak receiver downconversion power-gain of 27.6dB with a maximum gain variation of 3.6dB, 4.7dB NF, -22dBm IIP3 while consuming 28.8mW from a 0.9V supply.

**Index Terms** — Transformer-Feedback, Lange Coupler, Intermediate Frequency, Mixer.

## I. INTRODUCTION

For the last decade, millimeter-wave (mm-wave) receivers have been an active subject of research, motivated primarily by the availability of the unlicensed 57GHz to 64GHz frequency band allocated for high-rate video and data-transfer applications. Mm-wave receivers typically fall into two categories: heterodyne [4] and direct conversion architectures (DCA) [1-3]. The generic heterodyne architecture, shown in Fig.1, comprises of a RF, IF, and baseband (BB) sections. The DCA reduces the power consumption in the signal path by eliminating the IF-section but requires an oscillator at the carrier frequency. From a power-consumption perspective, 60GHz oscillators and the associated drivers for LO distribution have proven problematic [2]. A heterodyne system, on the other hand, allows for a lower frequency LO distribution at the expense of an additional IF-section. The two-stage downconversion receiver allows flexibility regarding the choice of the LO and IF frequency. The system in [4] involves a 12GHz PLL and a  $4\times$  frequency multiplier to generate a 48GHz LO for the front-end RF downconverter. A 12GHz IF frequency ( $f_{IF}$ ) was selected for the receiver described in this paper. Although a heterodyne mm-wave receiver provides an advantage from the perspective of oscillator power consumption, new challenges are introduced when implementing the IF portion of the signal path. This paper discusses design

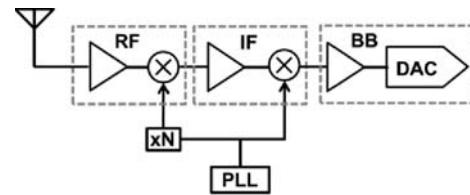


Fig.1. Two-stage heterodyne architecture

techniques to address the challenges of implementing a wideband IF-section in a 60GHz system. This paper assumes a frequency plan similar to that in [4].

Although [1-4] have demonstrated the feasibility of building 60GHz transceivers, there are opportunities for improving the performance of each section in the signal-path. In this paper, we present a transformer-feedback based wideband (11GHz to 13GHz) amplifier and a double-balanced I/Q downconversion mixer. In addition, we discuss a method for I/Q LO generation. In Section II, we highlight features of 60GHz systems which motivate high fractional bandwidth circuits. In Section III, we describe the source-gate transformer-feedback (SGTxFB) topology. In Section IV, we present the details regarding the circuit implementation, and in Section V, we provide the measurement results.

## II. SYSTEM CONSIDERATIONS

The IEEE 802.15.3c standard for 60GHz communication utilizes four channels, each ( $f_{IF-BW}$ ) 1.75GHz wide. For many of the systems designed to operate in this frequency band [1-4], the preferred solution for the RF front-end is a single tuned amplifier, which receives all 4 channels simultaneously, while channel tuning is implemented with a variable frequency LO. The effect of the RF-section ( $f_{RF-BW}/f_{RF}=7/60=11\%$ ) cascaded with the IF-section ( $f_{IF-BW}/f_{IF}=1.75/12=14\%$ ) must be considered to determine the composite receiver frequency response. The fractional bandwidth at the carrier frequency of a 60GHz receiver is significantly larger than that for other commercial wireless standards in the 0.8GHz to 5GHz bands. For example, GSM and WLAN

require a fractional BW of (25MHz/900MHz = 2.78%), and (80MHz/2.4GHz = 3 %), respectively.

Another significant challenge in high data-rate receivers is the need for equalization to mitigate the effects of multipath interference, distortion due to a non-uniform passband gain, and nonlinear phase [5]. Although the flavor of OFDMA modulation, supported in the IEEE 802.15.3c standard can mitigate the aforementioned problems, the high Peak-to-Average ratios of this modulation method necessitates a high back off, resulting in a low power amplifier (PA) efficiency. By contrast, for battery-powered portable devices, a single-carrier constant-envelope modulation method is supported by the same standard, which allows more power-efficient PA designs. Single-carrier modulation, however, lacks the robustness of OFDMA to multipath interference when high symbol rates are used. In addition, the receiver signal path becomes significantly more sensitive to gain variations. Although equalization must be implemented in most modern communication systems, it comes at a significant power and area penalty [5]. A flat receiver passband will significantly relax the required equalization and the associated hardware complexity. Thus, from a system perspective, the IF-section should provide a high fractional bandwidth.

### III. TRANSFORMER FEEDBACK

Different techniques to achieve high-gain wideband signal amplification include multi-stage stagger-tuned common-source or common-gate amplifiers, distributed amplifiers, LC band-pass filter topologies and transformer feedback based structures [3,6]. SGTxFB based amplifiers have been reported for 60GHz [3] and W-Band [6] front-end amplifiers. A single-ended SGTxFB amplifier is shown in Fig.2(a) along with its small-signal model. Using this model and assuming unity coupling, the admittance looking into the gate of the transistor can be described by,

$$Y_{in} = \frac{i_t}{v_t} = \frac{1}{s L n^2} + \frac{(n+1)^2 s C_{gs}}{n^2} + \frac{(n+1) g_m}{n^2} \quad (1)$$

From (1), one can see that the impedance looking into the gate of  $M_1$  appears as a parallel resonant network. The  $\text{Re}\{Y_{in}\}$  can be set to the desired value by suitable choice of the transformer turns-ratio ‘ $n$ ’. The quality factor ( $Q$ ) factor of the impedance match or the matching bandwidth can be controlled through the choice of  $L$ . For a high value of  $L$ , the  $Q$  of the  $\text{Re}\{Y_{in}\}$  is low, and a wideband match is achieved, but this comes at the expense of lower  $G_m$ , associated with an increase in inductor degeneration.

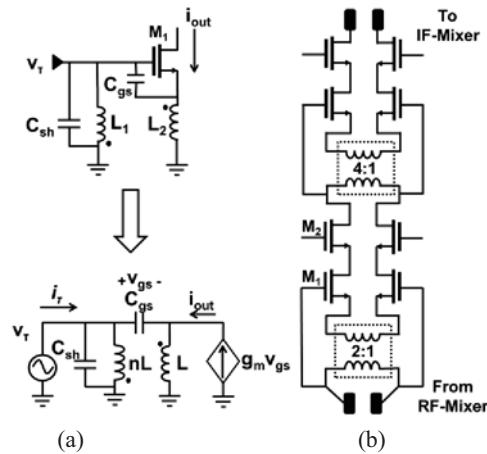


Fig.2. Source to Gate Transformer Feedback (SGTxFB)  
(a) Small-Signal Model (b) Two-Stage Structure

## IV. IMPLEMENTATION

### A. Amplifier Design

The schematic for the two-stage cascode IF-Amplifier (IFA) is shown in Fig.2(b). The SGTxFB topology discussed in Section III has been used to achieve a high fractional bandwidth and low passband gain variation at the interface between two IFAs and at the IFA/IF-Mixer interface. In simulation, a passband gain variation of less than 1dB over the 2GHz BW is observed. The IFA has a voltage gain of 19dB while consuming 17.2mW of power from a 0.9V supply. A  $100\Omega$  interface was selected for the first stage IF-Amp to facilitate stand-alone testing and characterization. A transformer with a turns ratio of 2 was realized using a 776pH ( $Q = 14$ ) and 2n ( $Q = 10$ ) spiral with a mutual coupling coefficient of  $\sim 0.7$ . The second IFA is interfaced to the first stage with a transformer which has a 1:4 turns ratio. From (1), a larger turns ratio implies a higher resistive load on the driver stage, allowing a larger voltage gain. In most mm-wave transformer-coupled designs, the primary and secondary inductors are connected to the drain and gate of two different active devices. Thus, the ports can appear on opposite ends to simplify the floor plan, as shown in Fig.3(b). By contrast, in SGTxFB, the transformer’s primary and secondary are connected to the same transistor, and therefore, the port interfaces must be on the same side. This arrangement places constraints on the top-level floor plan. One possible layout approach is shown in Fig.3(a), where the transformers have been placed to minimize the parasitic routing, which is achieved by maintaining close proximity between the active device and the transformer connection ports.

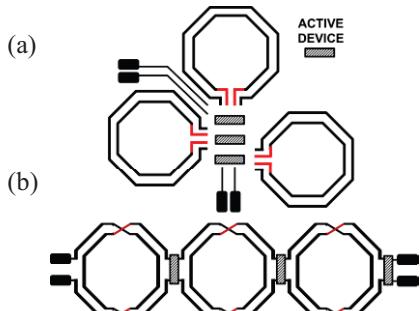


Fig.3. Multi-transformer layout floor-plan  
(a) SGTxFB (b) Transformer-Coupled

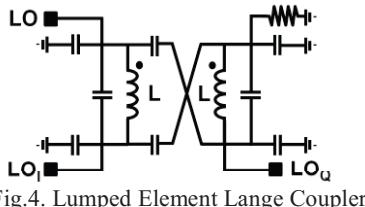


Fig.4. Lumped Element Lange Coupler

#### B. Quadrature LO Generation

The 12GHz Quadrature LO signals needed for I/Q downconversion were generated on-chip using a transformer-based lumped-element Lange coupler. Another LC-based wideband passive I/Q generation technique is to use a quadrature hybrid. The Lange coupler has been chosen in this design over the quadrature hybrid because of its compact area, which is enabled by a coupled inductor based design, as opposed to uncoupled-inductors used in the quadrature hybrid [7]. The schematic is shown in Fig.4. To reduce the amplitude mismatch between the I/Q signals, the magnetic coupling (K) between the transformer windings has to be 0.707 [7]. A multi-turn planar transformer layout ensures a high value of K. To interface with a  $50\Omega$  ( $Z_0$ ) port and operate at the LO frequency of 12GHz ( $f_{LO}$ ), the value of L, in Fig.4, should be

$$L = \frac{Z_0}{\{f_{LO}\sqrt{1 - K^2}\}} = 940pH \quad (2)$$

The outputs of the Lange-coupler feed a transformer-based Balun to generate the differential LO signals for the doubly balanced IF-mixer.

#### C. IF Downconversion Mixer Design

The schematic of the IF-Mixer is shown in Fig.5. The 11GHz to 13GHz IF signal is mixed with the 12GHz differential LO to generate the Baseband signals. The  $G_m$  stage of the mixer loads the final stage of the IF-Amplifier using SGTxFB. The  $G_m$  stage is transformer-coupled to the I and Q switching stages using a three-winding

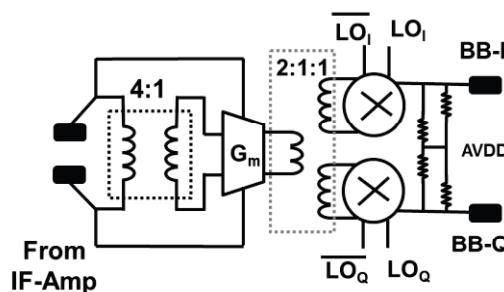


Fig.5. I/O Down Conversion Mixer

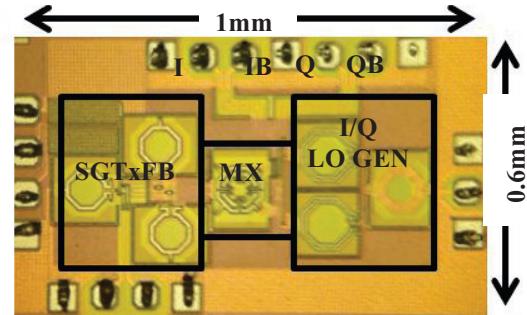


Fig.6. Chip Micrograph

transformer [8]. This topology allows a single  $G_m$  stage for both the I/Q double-balanced mixer switches, which results in power savings. The mixer consumes 10.8mW of power while operating from a 0.9V supply.

#### V. MEASUREMENT RESULTS

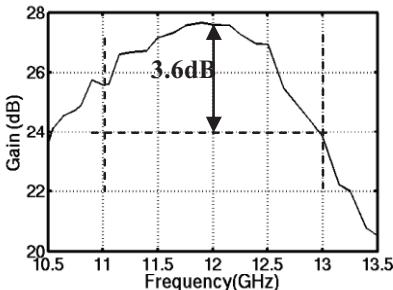


Fig.7. Conversion Gain

The IF-section has been fabricated in a 40nm CMOS process. The die photo is shown in Fig. 6. The size is 1mm x 0.6 mm including pads. The SGTxFB transformer and Lange-Coupler for I/Q LO generation have been highlighted. On-wafer probing was performed with a chip-on-board assembly. A balun-probe was used to provide a differential input signal to the circuit. A single ended 12GHz LO was provided for the on-chip I/Q generation circuitry.

The IF conversion gain and the input matching bandwidth are shown in Fig.7 and Fig.8 respectively. The peak conversion gain is 27.6dB with a gain variation of

3.6dB within 2GHz bandwidth. The input matching bandwidth S11<-9dB extends across from 11 GHz to 12.7 GHz. The double side band NF of the IF-section is measured to be 4.7dB.

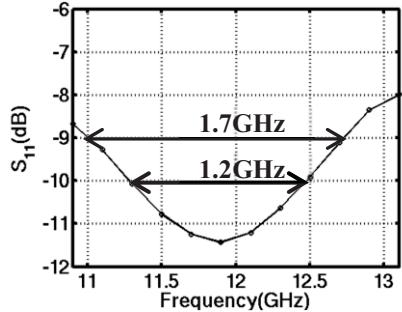


Fig.8. Input Matching Bandwidth

The linearity of the circuit was measured by a two-tone test. The result of the IIP3 test with two tones at 10MHz offset from a 12.1GHz center frequency is shown in Fig.9. The obtained IIP3 is -22dBm. This performance is obtained while consuming 28mW from a 0.9V supply. Table1 summarizes the performance of this chip.

Fractional Bandwidth (BW/f<sub>c</sub>) is a key metric to compare this design with prior-art. For this reason a

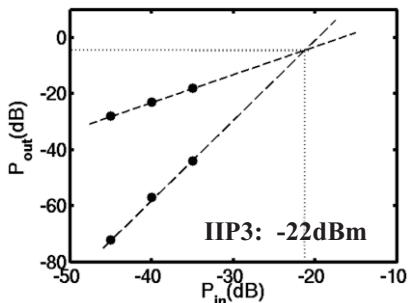


Fig.9.IIP3 measurement

comparison has been provided with wideband 24GHz CMOS receivers [9, 10]. While [9] reports a higher fractional bandwidth, this is achieved at the expense of a higher silicon area ( $> 1\text{mm}^2$ ) due to an LC-Bandpass filter-based implementation. [10] reports a higher passband gain variation for a lower fractional bandwidth compared to the design in this work.

## VI. CONCLUSION

This work presents a wideband IF-section consisting of a SGTxFB-based IF-Amplifier and a three-winding transformer-coupled I/Q downconverting mixer for a 60GHz receiver in a 40nm CMOS process. This design demonstrates the effectiveness of transformer-based

feedback to improve the passband gain variation in high fractional-bandwidth circuits. Layout techniques that minimize the frequency response sensitivity to layout parasitics were also presented. A combination of both novel design and layout methods applied to a mm-wave IF stage results in wideband response and relaxed demands on the synthesizer and oscillator power performance.

Table 1: Performance Summary and Comparison

Ref	Tech (V <sub>DC</sub> )	ΔGain (Gain)	BW f <sub>c</sub>	NF dB	Power (mW)
[9]	180nm	3.1dB (37dB)	<u>7GHz</u> 25.5GHz	5.5	51*
[10]	65nm 1.2V	6.5dB (31.5dB)	<u>2GHz</u> 24GHz	6.7	54.6 <sup>#</sup>
This work	40nm / 0.9V	3.6dB (27.6dB)	<u>2GHz</u> 12GHz	4.7	28.8 <sup>+</sup>

\* IFA and mixer ; \* LNA, mixer, BB; <sup>#</sup> LNA, mixer, BB

## ACKNOWLEDGEMENT

The authors are grateful for the assistance and support of S.Roy, M.Nariman, S.Sarkar, B.Perumana, P.Sen, E.Adabi, B.Afshar, and A. Behzad.

## REFERENCES

- [1] K.Okada, et.al, "A 60-GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver for IEEE802.15.3c", in *IEEE ISSCC Dig. Tech. Papers*, pp.160-161, Feb. 2011
- [2] C.Marcu, et.al. "A 90nm CMOS low-power 60GHz transceiver with integrated baseband circuitry", in *IEEE ISSCC Dig. Tech. Papers*, pp. 314-315, Feb. 2009.
- [3] N.Y.Wang et.al. "A 60dB Gain and 4dB Noise Figure CMOS V-Band Receiver Based on Two-Dimensional Passive Gm-Enhancement", in *IEEE RFIC Symp. Dig.*, pp.65-68, June 2011.
- [4] S.Emami, et.al, "A 60GHz CMOS phased array transceiver for multi-Gb/s wireless communication", in *IEEE ISSCC Dig. Tech. Papers*, pp. 164-165, Feb. 2011.
- [5] J.H.Park et.al, "A 2Gb/s 5.6mW Digital LOS/NLOS Equalizer for the 60GHz Band" in *IEEE JSSC*, Vol.46, Pp.2524-2534, Nov.2011
- [6] M.Khanpour et.al, "A Wideband W-Band Receiver Front-End in 65nm CMS", in *IEEE JSSC*, Vol.43, Pp.1717-1730, Aug. 2008.
- [7] D.Ozis et.al. "A CMOS 5GHz Image-Reject Receiver Front-End Architecture" in *IEEE RFIC Symp. Dig.*, June 2007
- [8] J.Paramesh et.al, "A four-antenna receiver in 90-nm CMOS for beamforming and spatial diversity", in *IEEE JSSC*, Vol.40, Pp.2515-2524, Dec. 2005
- [9] V.Jain et.al, "A CMOS 22-29GHz Receiver Front-End for UWB Automotive Pulse-Radar" in *CICC 2007*
- [10] A.Mazzanti et.al. "A 24GHz Subharmonic Direct Conversion Receiver in 65nm CMOS" in *IEEE TCAS*, Vol.58, Pg.88-97, Jan.2011.