A compact 24-54 GHz CMOS band-pass distributed amplifier for high fractional bandwidth signal amplification

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***Abstract* — This paper describes a compact 24-54 GHz two-stage band-pass distributed amplifier (BPDA) utilizing dual mirror-symmetric Norton transformations to reduce inductor component values allowing an area-efficient layout. The BPDA, implemented in a 40nm CMOS process, occupies an active area of 0.15mm^2, has a 77% fractional-bandwidth, an overall gain of 7dB, a minimum in-band IIP3 of 11dBm, in-band noise-figure less than 6.2dB while consuming 34mA from a 1V supply.**

***Index Terms* — wideband, distributed amplifier, Norton transform, coplanar waveguide.**

I. Introduction

Silicon technology scaling has motivated research and design of CMOS circuit components operating above several hundred GHz. In addition, new opportunities for single-chip mm-wave electronics are emerging in areas of ultra-wideband data-communication systems, high-resolutions radar, and medical-imaging. The goal of realizing CMOS transceivers for automotive-radar band (22-29GHz), phased-array systems for satellite-communication in the K_a-band (26.5GHz) and Q-band (30-50GHz) requires power and area efficient solutions with high fractional bandwidth signal amplification.

The low-pass distributed-amplifier (LPDA), shown in fig.1, is a generic circuit block commonly used to achieve signal gain across a large bandwidth. However, for ultra-wideband radar/radio applications band-pass amplification has several merits over low-pass amplification. First, from a system perspective, a band-pass response suppresses out-of-band interferers and blocker signals. Second, from a circuit perspective, the center-frequency of a band-pass distributed amplifier (BPDA) could potentially be higher than the cut-off frequency of an LPDA.

The major barrier to practical implementation of integrated ultra-wideband BPDAs is the large area associated with multiple on-chip spiral-inductors and/or transmission-lines. As a consequence, early attempts to realize a BPDA [1] [2] were in the discrete form. More recently, a SiGe-BiCMOS distributed amplifier reported in [3] employed a high-pass filter topology to reduce the number of inductors at the expense of an increased sensitivity to device parasitic capacitance. In contrast, this paper reports a fully-integrated, compact form-factor, high

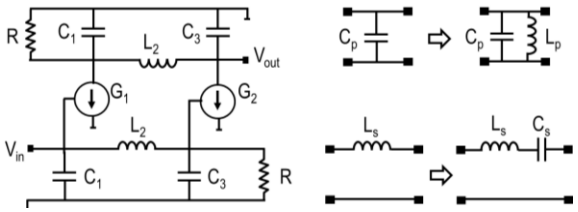

Fig.1 Low-pass distributed amplifier and low-pass to band-pass transformations

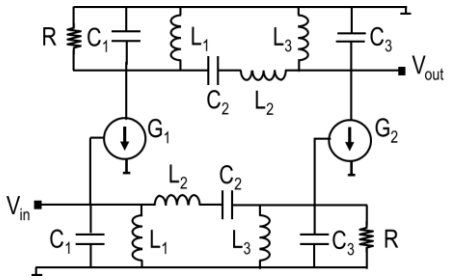

Fig.2 Canonical band-pass distributed amplifier

fractional-bandwidth CMOS BPDA based on a band-pass filter prototype. The design of a 'canonical' BPDA and the associated limitations are discussed in Section.II. A method to apply Norton-transforms which overcomes these limitations is described in Section.III. Following a detailed description of the amplifier in Section. IV, the measured results from a test-chip are presented in Section. V.

II. Canonical form

A BPDA can be derived from a LPDA by replacing the low-pass filters (LPF) on the gate, and drain lines with band-pass filters (BPF). The standard low-pass to band-pass transformation (fig.1) entails appending the shunt capacitors C_p with an inductor L_p, and the series inductors L_s with a series capacitor C_s. However, the resulting 'canonical' BPDA, shown in fig.2, has two significant limitations.

First, N inductors in an N-stage LPF are replaced by 2N+1 inductors in the BPF and thus, exacerbates the area-challenge plaguing all DAs. The second important limitation relates to inductance scaling as a function of bandwidth (BW) and center frequency (ω_c). To illustrate

this limitation, consider a doubly-terminated Butterworth BPF with a termination impedance Z_0,

$$L_2 = 2 * Z_0/BW \quad (1)$$

$$L_1 = BW * Z_0/{\omega_c}^2 \quad (2)$$

From (1), L_2 is independent of ω_c; therefore for a given BW, the inductor operates closer to its self-resonance frequency (SRF) as ω_c increases. Conversely, from (2), L_1 is inversely proportional to $1/{\omega_c}^2$, but directly proportional to the target BW. Thus, at millimeter-wave frequencies, the SRF of the inductors $L_{1/2}$ ultimately limits ω_c and the BW achievable for a BPDA implementation. The work reported in this paper applies a Norton transform to overcome the aforementioned limitations by substantially reducing the value of all the required inductances.

III. Norton Transformations

The basic idea of a Norton transform (NT), illustrated in fig.3, is to replace a series floating inductance L with an electrical equivalent circuit using the inductors labeled $L/(1-N)$, L/N , $L/\{N(N-1)\}$, and a single $1:N$ transformer. An NT-based broadband CMOS power-amplifier reported in [4], exploits the 1:N transformer for an impedance transformation in the output matching network. The proposed BPDA exploits mirror-symmetric Norton transforms to eliminate all transformers in the BPF. Starting with the BPF canonical form, component reduction may be found by setting N equal to 2. This results in a fictitious negative inductance, $L/(1-2)$, which can be exploited to further reduce the number of inductors in the BPDA. Inductor L_2 is first split into two equal valued series inductors and placed symmetrically about capacitance C_2. Next, the left most $L_2/2$ inductor is futher split into two inductances, L_1 and $L_x = L_2/2 - L_1$. Applying an NT on the series inductor, L_1 $(N = 2)$, results in a fictitious negative inductance, $-L_1$, in parallel with a shunt inductor, L_1 ; note $L_1 // -L_1$ is an open circuit, effectively eliminating both inductors. The NT also introduces a 1:2 transformer T_1 .The same process is repeated by replacing the second half-inductance $L_2/2$ with L_x and L_1 . The synthesis further continues by reflecting the two residual series inductances, L_x, and capacitance, C_2, across the windings of transformer T_2 . This scales the required value of inductor L_x by $(1/N)^2$. Finally, the residual transformers T_1 and T_2, produced by the mirror-symmetric NTs, now appear in cascade, and have equal turns ratios of $1:N$ and $N:1$ respectively, which effectively neutralizes (eliminates) one another. In summary, inductor L_2 in the canonical form of the band-pass filter is reduced to two series inductances of

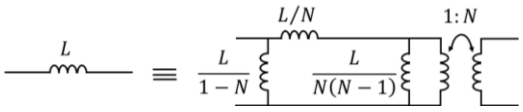

Fig.3 Norton transfomration for a series floating inductor

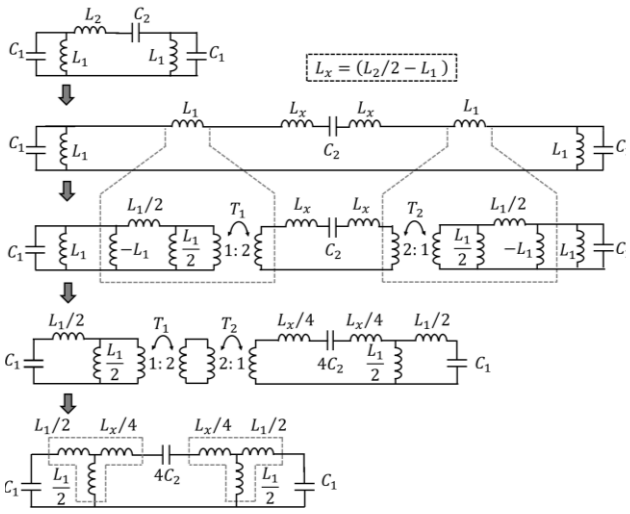

Fig.4 Derivation of the compact-area BPF from the canonical BPF through mirror-symmetric dual Norton-transforms.

$\{(L_2/2) - L_1\}/N^2$ after recursive transformations are applied; a minimum reduction of 75% $(N = 2)$ and inductor L_1 , is split into two equal halves along the series, and shunt signal paths.

IV. Circuit Implementation

The BPDA reported in this work implements two doubly-terminated band-pass filters with a Butterworth-filter response. Through the application of Norton transforms, the inductance values of L_1=180pH and L_2=800pH in the canonical structure are reduced to 90pH, 90pH, and 55pH, respectively, after applying the aforementioned NT techniques. The 800pH series inductor has been reduced to two inductances of ((800/2)-180)/4=55pH each. The band-pass section is now realized as two symmetric T-sections; highlighted in fig.4. Thus, although the Norton transform (NT) appears to increase the number of inductors in the circuit, the value of these inductances are at least an order of magnitude lower. In addition to the size advantage, it is noteworthy to mention the 55pH inductor will have a significantly higher SRF as compared to an 800pH inductor, further ensuring proper operation at mm-wave frequencies.

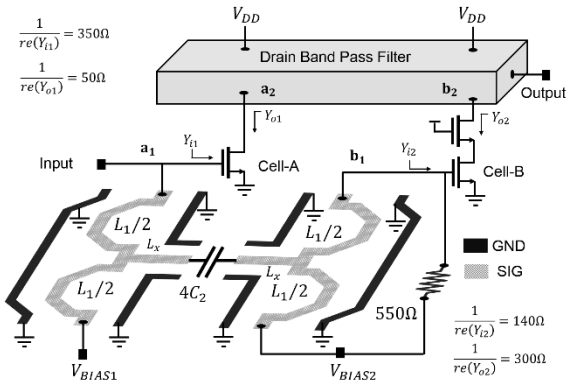

Fig.5 Circuit diagram of the BPDA

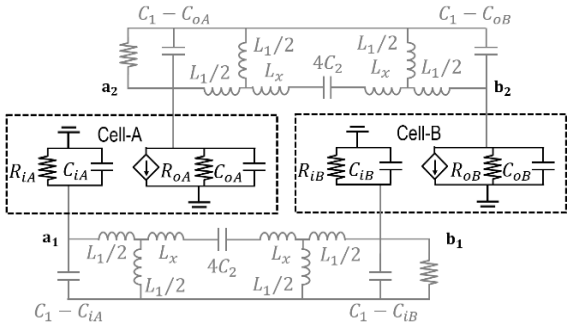

Fig.6 Input and output impedance of the gain-cells

Although reducing the BPDA inductance values to as low as 55pH provides a significant area advantage, it makes the transfer function more sensitive to routing-dependent parasitic inductance and capacitance. To alleviate this concern, the scaled inductor $L_x/4$ is realized as a coplanar waveguide (CPW) and used as routing between two symmetric T-sections in the simplified BPDA structure, fig.5. The series and shunt inductors $L_1/2$ are implemented as half-turn spiral inductors to eliminate additional routing to the supply and bias pads, fig. 5. To account for stray parasitic capacitance and mutual magnetic-coupling, the three inductors in each T-section were modeled and simulated as a single, three-port passive structure.

Similar to a LPDA, which has transmissions lines at the input (gate) and output (drain) to absorb the C_{GS} and the C_{GD} capacitance, the BPDA is realized using band-pass filters at the input and output. The two-stage BPDA consists of a common-source (gain-cell A) and cascode (gain-cell B) transconductance stage. The gain-cells are optimized to reduce the effect of its finite input/output impedance on the DA gain. Cell-A and B have different shunt input/output resistance (R_{in}/R_{out}) requirements. As shown in fig.6, the input impedance of cell-A (R_{iA}) loads node-a_1 in the gate BPF. Thus, to minimize the Q degradation, R_{iA} should be large, resulting in a small device

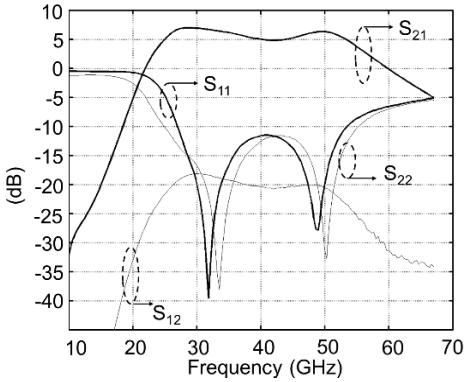

Fig.7 Measured S-parameter results

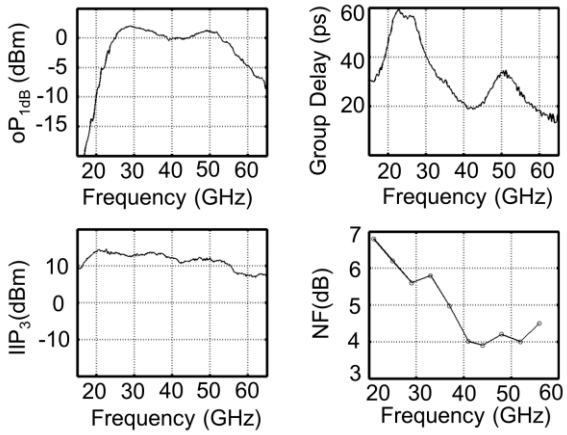

Fig. 8 Compression-point, group-delay, IIP3 characterization and noise-figure versus frequency.

width. In contrast, cell-B allows a larger width because the R_{iB} is absorbed into the termination impedance at node-b_1. Correspondingly, at node-b_2, R_{oB} degrades the Q of the drain-BPF, whereas at node-b_1, R_{oA} can be absorbed into the drain termination resistance. The 64um wide cell-A has R_{iA}=350Ω and low R_{oA}= 50Ω. The cascode gain-cell B has R_{iB}=140Ω and a high R_{oB}=300Ω. Both cells consume a current of 17mA from a 1V supply.

V. Measured Results

The chip was characterized using Cascade's 12000AP Summit on-wafer probe station. Measurements were performed using Agilent's N5247A PNA-X. For accurate S-parameter measurements, a two-port SOLT calibration was done on the Impedance Standard Substrate (ISS). For linearity metrics, such as IIP3 and P1dB, which require an accurate power measurement, power-calibration was performed up to the end of the interface cables.

The measured S-parameters of the BPDA are plotted in fig.7. The S_{11} and S_{22} are less than 10dB across a frequency

Table 1. Table of comparison

Parameters	[3]	[5]	[6]	This Work
Technique	High-pass DA	Coupled resonator	T-type matching	Band-pass DA
Bandwidth (GHz)	21-42.5	23-32	47-77	24-54
ω_c (GHz)	31.75	9	30	39
fBW	67.7	32%	48%	77%
Gain (dB)	8.3 (power-gain)	12 (voltage-gain)	22.5 (power gain)	7dB (power gain)
Power (mW)	28	13	52	34
IIP3 (dBm)	-x-	-6.3 to -4.5	-x-	10 to 13
NF (dB)	6.9-8	4.5-6.3	5-7.2	3.9-6.2
OP_{-1}(dBm)	0	-x-	4.5 (simulated)	-0.5 to 2
Area (mm^2) Pads not included	0.28	0.25	0.55	0.15
Technology	120nm SiGe-BiCMOS	180nm BiCMOS	250nm BiCMOS	40nm CMOS

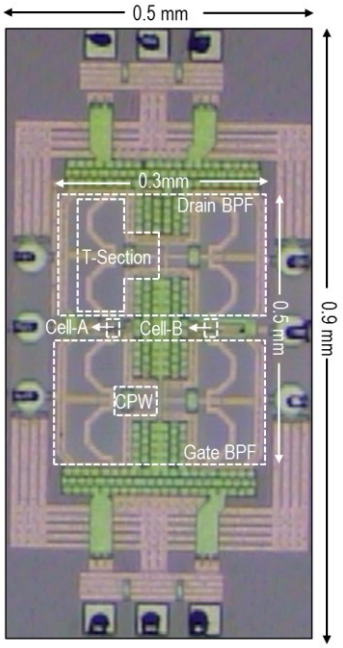

Fig.9 Chip micrograph

range of 26.8GHz-to-54GHz, and 24.8GHz-to-55GHz, respectively. The peak-gain of the amplifier is 7dB with a 3-dB pass-band from 24GHz to 54GHz; a BW of 30GHz, or a fBW of 77%. The amplifier pass-band covers both the K_a-band and Q-band. The total in-band gain-variation is 2dB. The measured noise-figure, linearity and group-delay variation are plotted in fig.8. The NF of the receiver is measured using the Y-factor method. The minimum NF is 3.9dB, and remains less than 6.2dB across the entire passband. To characterize the wideband linearity of the BPDA, the compression and intercept points were measured across frequency. The minimum and maximum in-band output 1dB compression points are -0.5dBm and 2dBm, respectively. The minimum in-band IIP3 for a 100MHz tone-spacing is 11dBm. The in-band group-delay varies between 20ps and 55ps.

A die photograph of the prototype mm-wave receiver chip, fabricated in a 40nm CMOS process, is shown in fig.9. The 6-layer metal stack consists of one ultra-thick metal (UTM) and one aluminum passivation layer (AP). The DC-supply is brought on chip using a 3-pin Z-probe on the north-end. The gate bias voltages are brought on-chip through a Z-probe from the south-side. The millimeter-wave input and output are brought on-chip using GSG probes on the west and east-side, respectively. The core of this compact DA occupies an area of 0.5mm x 0.3mm. The performance of the BPDA is summarized in Table 1. In contrast to prior-art, the Norton simplified BPDA presented in this work is in a standard-CMOS technology and achieves the highest fBW, while consuming the lowest silicon area.

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