A Class-G Dual-Supply Switched-Capacitor Power Amplifier in 65nm CMOS

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***Abstract*—A digitally-controlled switched-capacitor RF power amplifier (SCPA) that uses a dual-supply voltage, class-G architecture is implemented in 65nm CMOS. It implements signal envelope digital-to-analog conversion using switching functions controlled by digital logic to achieve superior efficiency and linearity at output power backoff. The SCPA delivers a peak (average) output power of 24.3 (16.8) dBm with a peak (average) PAE of 44% (33%) for an *IEEE 802.11g* signal (64 QAM OFDM) with a measured EVM of 2.9 % in the 2.4 GHz band. No digital predistortion was necessary because of the superior linearity.**

***Index Terms*—CMOS integrated circuits, EER, polar transmitters, power amplifiers, power combining circuits, switched-capacitor circuits**

I. Introduction

It is well known that the RF power amplifier (PA) consumes the most power of any block in the RF transceiver in modern wireless communication systems. Consequently, it has a significant impact on the battery lifetime of mobile wireless devices. Non-constant envelope (non-CE) modulation is prevalent in modern communication systems (e.g., *WiFi*, *WiMAX*, *LTE*, etc.) because the costly and scarce spectrum available for communication links necessitates high spectral efficiency [1][2].

Power efficiency in an RF PA is typically defined using the drain efficiency (η_{PA}) and power-added efficiency (PAE_{PA}) metrics:

$$\eta_{PA} = {P_{out}}/{P_{DC}} \tag{1}$$

$$PAE_{PA} = \frac{P_{out}}{P_{in}+P_{DC}} \tag{2}$$

where P_{out} is the output power, P_{DC} is the dissipation in the DC supply and P_{in} is the input power provided to drive the PA.

An RF PA exhibits a quadratic relationship between output voltage and output power:

$$P_{out} \propto {V_{out}^2}/{R} \tag{3}$$

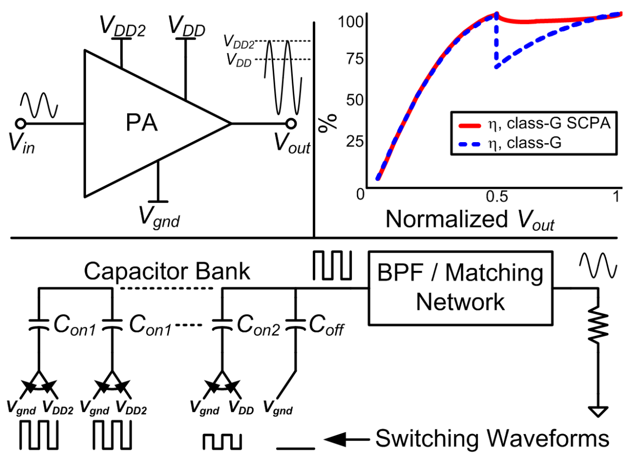

Fig. 1. Class-G SCPA with two power supply voltages. Clockwise from top left: Conceptual class-G PA, comparison of ideal efficiencies for the conventional and SCPA versions, and an implementation with ideal switches and capacitors.

where V_{out} is the instantaneous output voltage and R is the transformed termination resistance applied to the output of the PA.

Operation using modulation schemes with high spectral efficiency causes the RF PA to lose power efficiency because the signal information is coded in both instantaneous phase, $\phi(t)$, and amplitude, $A(t)$. Changes in $A(t)$ result in changes in V_{out} while P_{in} and P_{DC} remain relatively constant. Although the RF PA is designed to exhibit peak efficiency at its maximum output power level, P_{sat}, it loses efficiency as the envelope amplitude decreases the output voltage of the PA. The ratio of the peak to average envelope amplitudes defines the peak-to-average power ratio (PAPR), which varies depending on the type of modulation. Large PAPR values are problematic because the average mode of operation for the envelope signal is far from the peak amplitude where the PA operates with maximum efficiency.

Many modern communication systems employ orthogonal frequency-division multiplexing (OFDM) because of its superior spectral efficiency; however, a drawback of OFDM is its large PAPR (e.g., ~13 dB for *WiFi* and *WiMAX*) which results in low energy efficiency for these formats.

Many attempts to improve the energy efficiency operate the RF PA as close to saturation as possible using external linearization around a *switching-amplifier* topology. Notably the envelope elimination and restoration (EER) technique has shown great promise [3]. Two such SCPA implementations that combine a digitally-modulated PA with EER enable operation with high average efficiency, linearity and output power [4][5][6].

In this paper, a class-G SCPA architecture is introduced that improves the average efficiency for signals with large PAPR values. It operates from either of two power supply voltages depending on the amplitude of the signal, as shown in Fig. 1. The overall objective of operating close to saturation for more than just the near-peak signal levels is achieved by digitally selecting the optimal supply voltage based on a digital code word representation of $A(t)$. For small (large) $A(t)$ values, the SCPA switches selected capacitors between V_{DD} and V_{gnd} (V_{DD2} ($2\times V_{DD}$) and V_{gnd}). The design of a class-G SCPA with an optimal switching arrangement to maximize efficiency is described in Section II. Measurement results from a 65nm experimental prototype are presented in Section III, and conclusions are given in Section IV.

II. Design of the Class-G SCPA

The SCPA topology is ideal for CMOS implementations: (1) CMOS processes provide capacitors as native, area-efficient passive elements, and (2) precision capacitor *ratios* enable accurate and linear realizations [5]. Finally, owing to the continuing increases in switching speeds, scaled CMOS switched-capacitor circuits can be employed at the GHz frequencies commensurate with RF communication systems. A description of the theory of operation of the basic SCPA is given by Yoo, et al. [6]. Details of the class-G SCPA with the optimal decoding scheme are now described.

A. Class-G SCPA Design Details

A block diagram of the class-G SCPA is shown in Fig. 2; a single-ended version is shown although the fabricated circuit is fully differential. It utilizes a digital EER technique to achieve a highly linear output characteristic from a high-efficiency switching configuration. First, the non-CE modulated baseband signal is transformed from a Cartesian representation to an equivalent polar form. The resulting time-varying amplitude signal, $A(t)$, is input as a digital code word, $B_{IN}(A)$, to combinatorial decoding logic that enables switching of the bottom plates of selected capacitors between V_{DD} and V_{gnd} or V_{DD2} and V_{gnd}. After up-conversion to the RF carrier frequency, the time-varying phase signal, $\phi(t)$, serves as the clock input to the combinatorial logic that drives the capacitor array.

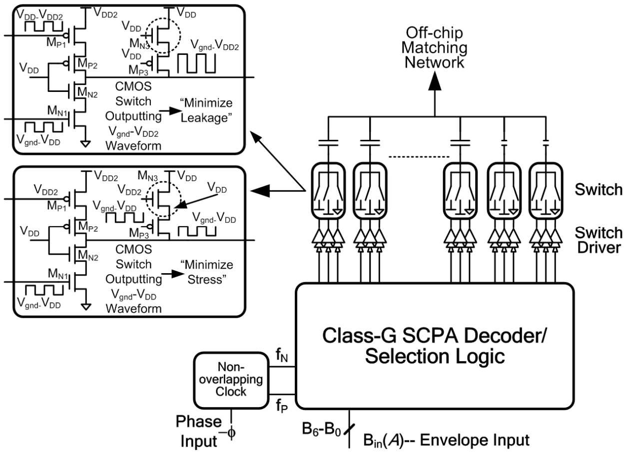

Fig. 2. Block diagram of the class-G SCPA showing minimum leakage and minimum voltage stress switch implementations.

The capacitor array comprises a total of 6 bits: The four MSBs are unary-weighted and controlled by a binary-to-thermometer decoder whereas the two LSBs are binary-weighted for fine resolution. An extra bit is achieved by operating with two different power supply voltages; hence, 7 total bits of resolution are realized.

It is desirable to operate the RF PA at a maximum supply voltage that exceeds V_{DD} in order to reduce the losses associated with the matching network. This advantage accrues because the resulting impedance transformation ratio (ITR) is smaller as are proportionate losses in the matching network [7]. Cascoded switch designs are used as depicted in Fig. 2 because scaled NMOS and PMOS devices cannot tolerate voltages greater than V_{DD}.

When the output of the switch (Fig. 2 top) toggles between V_{gnd} and V_{DD2}, the series combination of M_{N3}/M_{P3} remains OFF, which isolates V_{DD} from V_{DD2} and minimizes the leakage current. When the output of the other switch (Fig. 2 bottom) toggles between V_{gnd} and V_{DD}, M_{N3} is ON and M_{P3} is switched, which limits the maximum voltage stress to V_{DD} between any two terminals. Additionally, the switching transistors are laid out in a cascode configuration wherein the gates of $M_{N1,2}$ ($M_{P1,2}$) operate between V_{gnd} and V_{DD} (V_{DD} and V_{DD2}) [8].

The un-switched capacitor top plates are connected together to a band-pass matching network which provides low impedance to the array at the desired operating frequency, enables high power output, and filters harmonics associated with the switching operation.

Although the SCPA has been shown previously to operate efficiently with on-chip matching networks, this class-G implementation employs an external matching network to save die area and improve harmonic filtering.

	C1	C2	C3	C4	C5	C6	C7	C8A	C8B
0000	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}
0001	V_{DD}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}
0010	V_{DD}	V_{DD}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}
0011	V_{DD}	V_{DD}	V_{DD}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}
0100	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}
0101	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}
0110	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{gnd}	V_{gnd}	V_{gnd}
0111	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{gnd}	V_{gnd}
1000	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}
1001	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{gnd}	V_{gnd}	V_{gnd}	V_{DD2}	V_{gnd}
1010	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}
1011	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{gnd}	V_{gnd}	V_{DD2}	V_{gnd}
1100	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{gnd}	V_{gnd}	V_{gnd}
1101	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{gnd}	V_{DD2}	V_{gnd}
1110	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{gnd}	V_{gnd}
1111	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{gnd}

	C1	C2	C3	C4	C5	C6	C7	C8
0000	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}
0001	V_{DD}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}
0010	V_{DD}	V_{DD}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}
0011	V_{DD}	V_{DD}	V_{DD}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}
0100	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{gnd}	V_{gnd}	V_{gnd}	V_{gnd}
0101	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{gnd}	V_{gnd}	V_{gnd}
0110	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{gnd}	V_{gnd}
0111	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{gnd}
1000	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
1001	V_{DD2}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
1010	V_{DD2}	V_{DD2}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
1011	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
1100	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
1101	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD}	V_{DD}	V_{DD}
1110	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD}	V_{DD}
1111	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD}

Fig. 3. Example 4-b switching sequences for conventional (left) and improved class-G SCPA stages (right). Note: V_{gnd} indicates no switching, V_{DD} switching between V_{gnd} and V_{DD} and V_{DD2} switching between V_{gnd} and V_{DD2}.

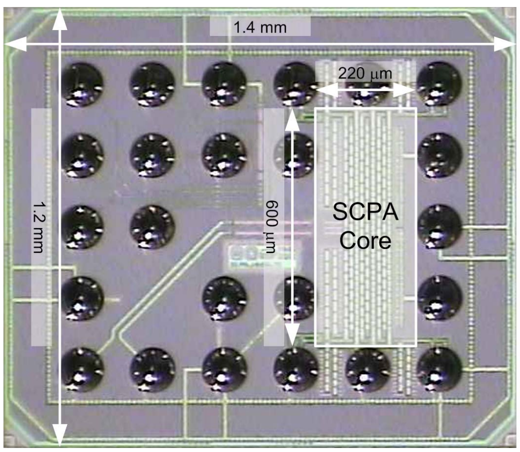

Fig. 4. Chip microphotograph in 65nm CMOS.

B. Optimal Selection Logic

The conventional envelope code switching sequence for a 3-bit unary capacitor array is tabulated in Fig. 3 (left). Note from Fig. 1 that the efficiency decreases substantially as the normalized output voltage changes from 1.0 to 0.5 V. The codes are divided in a non-optimal pattern as switching between V_{gnd} and V_{DD} (V_{gnd} and V_{DD2}) is enabled only with MSB = 0 (MSB = 1). This drawback is overcome in the class-G SCPA using the modified envelope code switching sequence shown in Fig. 3 (right) that uses V_{DD} and V_{DD2} simultaneously.

Although Fig. 3 details a 4-bit implementation, the number of bits can be varied in accordance with the specifications for linearity, efficiency, etc. A 6-bit capacitor array is used in the 65nm design; an extra bit of resolution is achieved using two power supply voltages.

III. Measurement Results

An experimental prototype of the class-G SCPA is fabricated in a 65 nm RF CMOS process. The die is flip-chip bonded to a PCB and uses an external impedance matching network. A microphotograph of the SCPA chip is shown in Fig. 4. It operates at a center frequency of 2.15 GHz and generates peak output power and efficiency levels of 24.3 dBm and 43.5%, respectively, as shown in

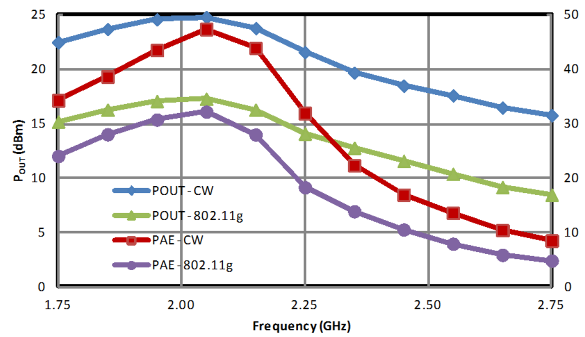

Fig. 5. Measured frequency and efficiency responses.

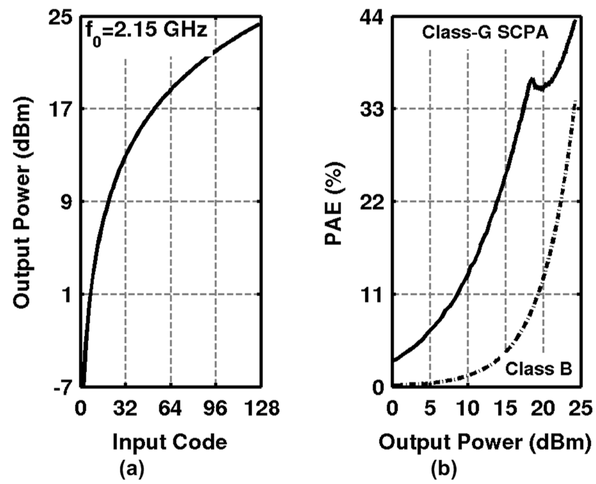

Fig. 6. (a) Measured output power vs. input code and (b) PAE vs. output power.

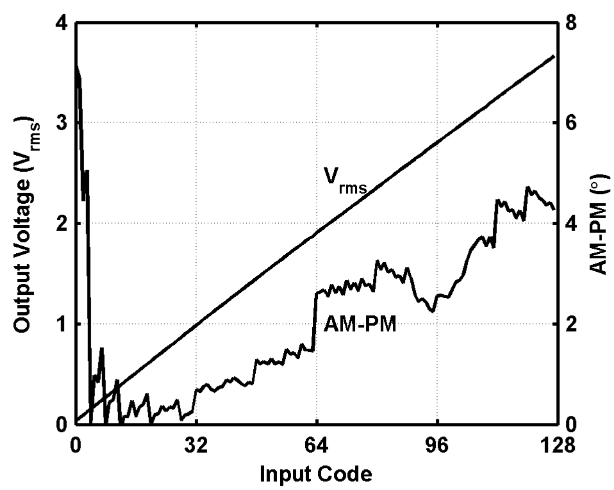

Fig. 7. Measured output voltage and AM-PM distortion characteristics for the class-G SCPA.

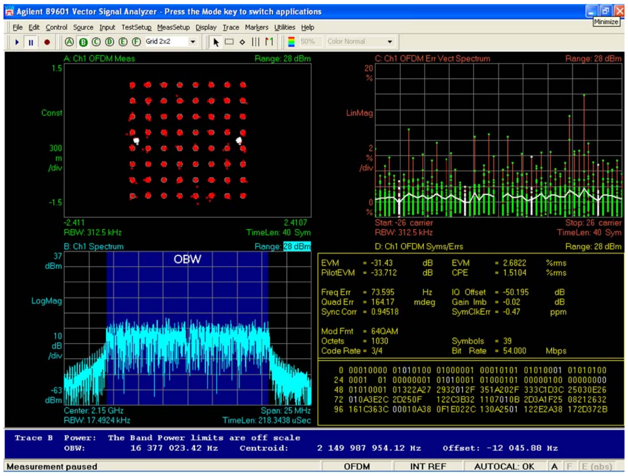

Fig. 8. Measured EVM performance of the class-G SCPA.

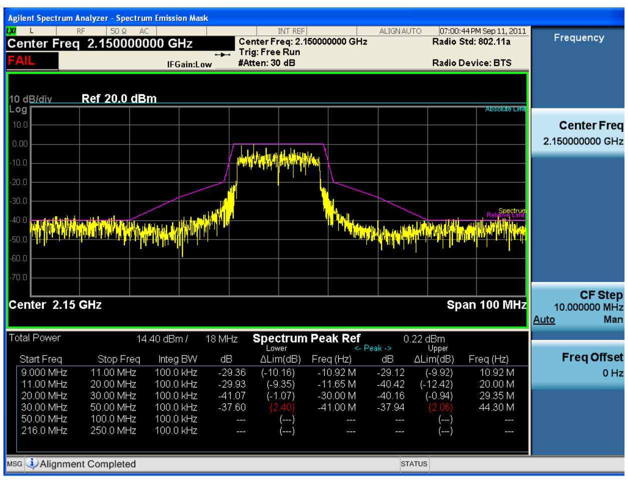

Fig. 9. (a) Measured in-band and out-of-band spectral responses relative to the *WiFi* spectral mask.

Fig. 5. The -3 dB bandwidth is ~500 MHz as determined by the loaded quality factor of the band-pass matching network.

The output power of the class-G SCPA versus input code and PAE versus output power are plotted in Fig. 6. The PA achieves a peak output power of 24.3 dBm with a corresponding efficiency of 44%. The efficiency is degraded by only 7% at a power backoff level of -6 dB because of the second power supply voltage. Owing to the precision of capacitor ratios in CMOS, the linearity performance is also excellent as shown in Fig. 7.

The dynamic performance is measured by inputting an *IEEE 802.11g* signal (e.g., 64 QAM OFDM with a 20 MHz channel bandwidth) to the PA and measuring the resulting error vector magnitude and output power spectral density as shown in Figs. 8 and 9, respectively. The PA achieves a measured EVM of 2.9% and excellent spectral performance using no additional filtering or predistortion. The measured average output power and efficiency while amplifying the *IEEE 802.11g* signal are 16.8 dBm and 33%, respectively.

IV. Conclusions

A class-G SCPA prototype, fabricated in a 65 nm RF CMOS process is demonstrated. It incorporates the functionality of an envelope DAC into a power amplifier, which enables efficient and linear amplification of non-CE modulated signals. The superior linearity of the class-G SCPA allows it to linearly amplify large PAPR signals with no predistortion.

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