Filter-Bank Design by Transconductor for Sub-Band ADC

by

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Certificate

This is to certify that this thesis on **Filter-Bank Design by Transconductor for Sub-Band ADC** submitted by **Arka Majumdar**,**(03EC1024)** to the department of Electronics and Electrical Communication Engineering, IIT, Kharagpur, in partial fulfilment for the award of the degree of Bachelor of Technology (Hons) is an authentic record of the work carried out by him under my guidance and supervision. This thesis has fulfilled all the requirements as per the rules of this institute and in my opinion has reached the standard needed for submission. The same has not been submitted for any other degree or diploma elsewhere.

Prof. A.S.Dhar, Supervisor

This Thesis is dedicated to my Parents and Godhuli

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The growing VLSI technology and ease in signal processing in digital domain calls for high-speed good ADCs. In this thesis a new type of ADC, viz., sub-band ADC is described. The system level simulation and mathematical analysis are done to show that in certain applications, Sub-band ADC performs better than conventional time-interleaved ADC. The practical difficulties of implementation this ADC in silicon are described. The most critical part of sub-band ADC, viz., the filter-bank is designed and simulated in CADENCE in commercially available 0.18μ *technology. Two types of architectures are described and their design criteria are elaborated. For designing filters* g_mC *topology is used and hence a transconductor is designed. An analog active delay is designed in MOS. For recombining the signal from different bands a new heuristic is proposed and considerable performance (around* $6dB$*) enhancement is obtained.*

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Chapter 1

Introduction

1.1 Motivation

In today's Electronics Industry, Analog to digital converters are gaining a lot of attention due to the ease of signal processing in digital domain [1]. Digital Signal Processing Algorithms are becoming more powerful, while advances in integrated-circuit (IC) technology are providing compact, efficient implementation of these algorithms in silicon. But naturally occurring signals are analog and for all the digital processors we require an interface to convert the analog signal to a digital one. In fact, the whole philosophy of realization of a large system may be significantly eased by the performance enhancement of many analog circuits (like filters, Analog-Digital-Converters etc.) at some interfacing point between real world and digital computation. Advent of software defined radio has made the necessity of ADC, working at very high speed and for a large bandwidth, more prominent. Bit or resolution and dynamic range are two key specifications of an ADC and people are trying to get a good trade-off between these two [2] while designing ADCs. Now-a-days over-sampling ADCs are also getting attention with nyquist-rate ADCs for its better resolution and better noise shaping. But the performance of all the ADCs is limited by the requirement of good sample-hold circuit. In many applications, the incoming signal is of very high band-width. To digitize this signal, the sampling frequency required is very high and often unreachable in practical realization on silicon. These practical problems motivated me to design a new kind of ADC, which requires less sampling frequency. As the basic concept is taken from sub-band coding technique, it is called sub-band ADC.

My thesis is about some basic investigations which I carried out into the possibility of breaking the analog signal in several frequency sub-bands and performing analog to digital conversion in each frequency band separately and finally combine the signals from each band. To put this work into context, it may be wise to discuss about the basic problem when the incoming signal is of high bandwidth and the idea by which this can be combatted.

1.2 Problems With Conventional ADCs

According to nyquist criteria, a signal should be sampled at more than twice the bandwidth of the signal for faithful reconstruction of the original signal from sampled signal. Hence for a wide band-width signal the sampling frequency required is very high. For sampling, we need good track-and-hold circuits. But whenever the circuits are mapped to silicon, due to many non-idealities the track-and-hold cannot work properly at high frequency.

Again all the track-and-hold circuits need a clock of the sampling frequency. Due to phase noise all practical clocks are jittery. The phase noise increases with the frequency of the clock and hence at high frequency the jittery clock causes distortion in the sampled digital signal. In the following subsection an analysis is given to show how the jitter in clock causes distortion in the signal.

However, to reduce the requirement of track-and-hold circuit operating at very high sampling frequency people have already proposed time-interleaved ADC. This type of ADC basically has M ADCs, each sampling the signal at F_s/M frequency in a serial fashion and thus ultimately results in sampling the signal at a frequency F_s. A fundamental problem with an actual implementation of such time-interleaved architecture is that each ADC sees the full bandwidth of the input signal and hence clock jitter is very detrimental to the performance of this type of ADC. Hence good time-interleaved ADC needs a good sample-hold circuit along with a clock with a very little phase noise. Both of these are difficult to achieve. Apart from this the synchronization of the clocks is also difficult in practice and clock-skew causes problem in time-interleaved ADCs.

1.2.1 Jitter Analysis

Jitter is a severe problem in any sample-hold circuit. The clock-jitter is translated into the output spectra and distorts the signal. A theoretical jitter analysis is

performed to predict the distortion in output spectra from the clock-jitter. Two types of analysis are performed (time and frequency domain analysis) to reach the same result. Let the input signal be $A\sin(2\pi f_{in}t)$ and the sampling clock (which is jittery) be $B\sin(2\pi f_s t)$.

Time Domain Analysis: Due to jitter at n^{th} sampling instant the actual instant becomes $nT + \tau_n$. So the error $\epsilon(t)$ becomes

$$\epsilon(t) = A\sin(2\pi f_{in}(nT + \tau_n)) - A\sin(2\pi f_{in}nT) \tag{1.1}$$

By taylor's series expansion

$$\epsilon(t) = A2\pi f_{in}\tau_n \cos(2\pi f_{in}nT) \tag{1.2}$$

Hence noise-power N_τ in the sampled signal is given by

$$N_\tau = E((\epsilon(t))^2) = 2\pi^2 f_{in}^2 A^2 \sigma_t^2 \tag{1.3}$$

where

$$E((\tau_n)^2) = \sigma_t^2 \tag{1.4}$$

Now in the similar manner, for oscillator due to the jitter

$$\epsilon_{osc}(t) = B2\pi f_s \tau_n \cos(2\pi f_s nT) \tag{1.5}$$

$$N_{osc\tau} = E((\epsilon_{osc}(t))^2) = 2\pi^2 f_s^2 B^2 \sigma_t^2 \tag{1.6}$$

Hence the ratio R of the noise-power in oscillator and sampled signal is

$$R = (\frac{f_{in}}{f_s})^2 (\frac{A}{B})^2 \tag{1.7}$$

The same relation can be obtained by modeling the jitter as a random walk model [3].

Frequency-Domain Analysis: In frequency domain also the same analysis can be done [4]. Oscillator output $S(t)$ is

$$S(t) = B\sin(2\pi f_s(nT + \tau_n)) = B\sin(2\pi f_s nT) + 2\pi f_s \tau_n B\cos(2\pi f_s sinT) \tag{1.8}$$

So if the autocorrelation of the jitter is $r(\lambda)$ then the autocorrelation $R(\lambda)$ of the

oscillator noisy signal is given by

$$R(\lambda) = \frac{B^2}{2} E(\cos(2\pi f_s \tau_n))(1 + 4\pi^2 f_s^2) r(\lambda)) \tag{1.9}$$

So PSD $S(f)$ is given by

$$S(f) = \frac{B^2}{4}(1 + (2\pi f_s)^2 s(f)) * (\delta(f + f_s) + \delta(f - f_s)) \tag{1.10}$$

For the sampled output from the relation given in 1.5 autocorrelation as well as PSD obtained is

$$R(\lambda) = \frac{A^2}{2} E(\cos(2\pi f_{in} \tau_n))(4\pi^2 f_{in}^2) r(\lambda)) \tag{1.11}$$

$$S_{sample}(f) = \frac{A^2}{4}(1+(2\pi f_{in})^2 s(f)) * \frac{1}{T} \sum_{k=-\infty}^{k=+\infty} (\delta(f - f_{in} + \frac{k}{T}) + \delta(f + f_{in} + \frac{k}{T})) \tag{1.12}$$

So in baseband the ratio becomes the same as obtained from the time-domain as $f_s^2 >> 1$.

1.3 Concept of Sub-band Coding

In video and image applications people use sub-band coding. The idea is to break the image or the video in several frequency bands. Now in most of these signals the information content is non-uniformly distributed in frequency bands. Most of the information are in lower frequencies and higher frequency bands contain less information. So the lower frequency signals are assigned more number of bits compared to the higher frequency signals and thus total number of bits are reduced retaining the amount of information. This sub-band technique is very much used in speech analysis [5]. This idea is exploited in sub-band ADC. A mathematical analysis on the virtue of sub-band ADC is given in chapter 2.

1.4 Applications

There are many applications where the sub-band ADC will be helpful. Now-a-days UWB radio is gaining lots of attention. This type of radio operates by spreading the energy of the radio signal very thinly from near d.c. to a few gigahertz [6]. For this type of radio this ADC can be useful. In some satellite applications we get signal

with very wide band-width [7]. In that case the signal information is not uniformly distributed. Some band contain more information compared to other bands. Here this type of ADC is useful. In fact, if in some applications we see the signal is of very high band-width and the information is not uniformly spread over the whole frequency band, then this type of ADC gives very good performance.

1.5 The Work Described in the Thesis

The thesis mainly deals with the possible CMOS implementation of this new type of ADC. Due to many practical difficulties no ADC performs well when the input signal bandwidth is more. The architecture proposed here works better in this type of scenario. The virtue of this proposed sub-band ADC is mathematically established. By MATLAB simulations, the superiority of sub-band ADC over conventional time-interleaved ADC is established. Though mathematically true, practical implementation of this type of ADC poses many problems. Those problems are addressed and possible solutions are found out in this thesis. I mainly concentrated on the filter-bank design of this ADC as this is the most important part in this ADC. Two types of band-splitting architectures are proposed. In CADENCE, in commercially available 0.18μ technology the filter-banks are simulated. Here the incoming signal is split mainly in two bands. ADCs for each band is also designed. For this good track-and-hold circuits and comparators are studied as well as designed in silicon.

The thesis is organized as follows. Chapter 2 deals with the system level simulation (mainly in MATLAB) of sub-band ADC and the performance enhancement is reported and mathematically analyzed. This chapter also gives many useful design criteria of the ADC. Chapter 3 describes basic transconductor block and transconductor-C filter. Different implementations of transconductors are discussed and the performance of the transconductor used in my case is reported. The next 2 chapters deal with the filter-bank. Two different architectures for filter-banks are discussed and their implementation in silicon are described. The advantages and disadvantages of each architecture are also discussed. In chapter 6 the design of ADC is described. It includes design of good sample-hold as well as good comparator circuits. Chapter 7 mainly discusses the reconstruction in digital domain by means of FIR filtering and equalization concept. The result obtained from the system-level simulation in MATLAB is also reported. Chapter 8 discusses some other works not directly related to the main work of the thesis. Chapter 9 draws the conclusion and

discusses about the future work.

Chapter 2

System Level Description of Sub-band ADC

2.1 Introduction

In this chapter the system level simulations (the procedure and the result) on sub-band ADC are described. I have simulated the whole system in MATLAB and the performance enhancement is reported. I have also established mathematically the reason for enhancement in performance.

2.2 Virtue of Sub-band ADC

Sub-band ADC can perform better than conventional time-interleaved ADC. In this section, mathematically the virtue of sub-band ADC is established. The requirement of less sampling frequency for some bands are also established.

2.2.1 Dynamic Range Reduction

The dynamic range of the signal is reduced due to filtering. Variance of the signal is a good estimate of the dynamic range of the signal. The variance $R(0)$ (R is the autocorrelation function of the signal) of a signal (whose spectral content lies in the range of $\pm f$)can be expressed in terms of its Power Spectral Density (PSD) $S(\omega)$ as

$$R(0) = \int_{-f}^{+f} S(\omega) d\omega \tag{2.1}$$

After low pass filtering (with transfer function $H(\omega)$) let the spectral content lies in the range of $\pm w$. Then the new variance $R'(0)$ of the signal becomes

$$R'(0) = \int_{-w}^{+w} H(\omega)S(\omega)d\omega \tag{2.2}$$

Now if $|H(\omega)| < 1$, (which is true for a low-pass filter with pass-band gain 1) then the variance after filtering reduces and this helps in reduction in the dynamic range. For band-pass filtering also this argument holds true. This reduction in dynamic range helps in reduction in quantization noise. This is elaborated here. Let us assume that the incoming signal amplitude is Gaussian distributed. So using non-uniform quantization (smaller steps at $\pm 3\sigma$ limit) for the incoming signal total quantization noise q_{in} is

$$q_{in} = P_1 \frac{\Delta_1^2}{12} + (1 - P_1)\frac{\Delta_2^2}{12} \tag{2.3}$$

Where P_1 denotes the probability that the signal will be in $\pm 3\sigma$ limit. For the filtered signal also this is valid. But due to the reduction of variance the value of Δ_1 (which is proportional to the σ as $\delta_1 = \frac{6\sigma}{2^N}$) reduces and thus the quantization noise is less. Again if the incoming signal amplitude is uniformly distributed and the signal amplitudes are uncorrelated, then after filtering the amplitude is normally distributed. Mathematically it can be argued that the filtering operation is nothing but multiplying the random signal by some deterministic weights. If a random signal $x(t)$ is passed through a filter then the output $y(t)$ can be written as

$$y(t) = \int_0^t \xi(t)x(t)dt \tag{2.4}$$

where the $\xi(t)$s are deterministic coefficients dependent on the filter. If the incoming signal is uncorrelated (which is the worst scenario as no data compression is possible) then the integration provides a summation of infinite number of independent random variables and hence the filtered output follows a gaussian distribution by central limit theorem [8]. Figure (2.1) shows the probability distribution of a signal and its filtered output. Figure (2.2) shows the change in variance of the filtered signal with the filter order. As we increase the order, the dynamic range of the filtered signal is reduced more and more. For uniform distribution, uniform quantization is used. But for Gaussian distribution, non-uniform quantization can be used and that helps in reducing the quantization noise.

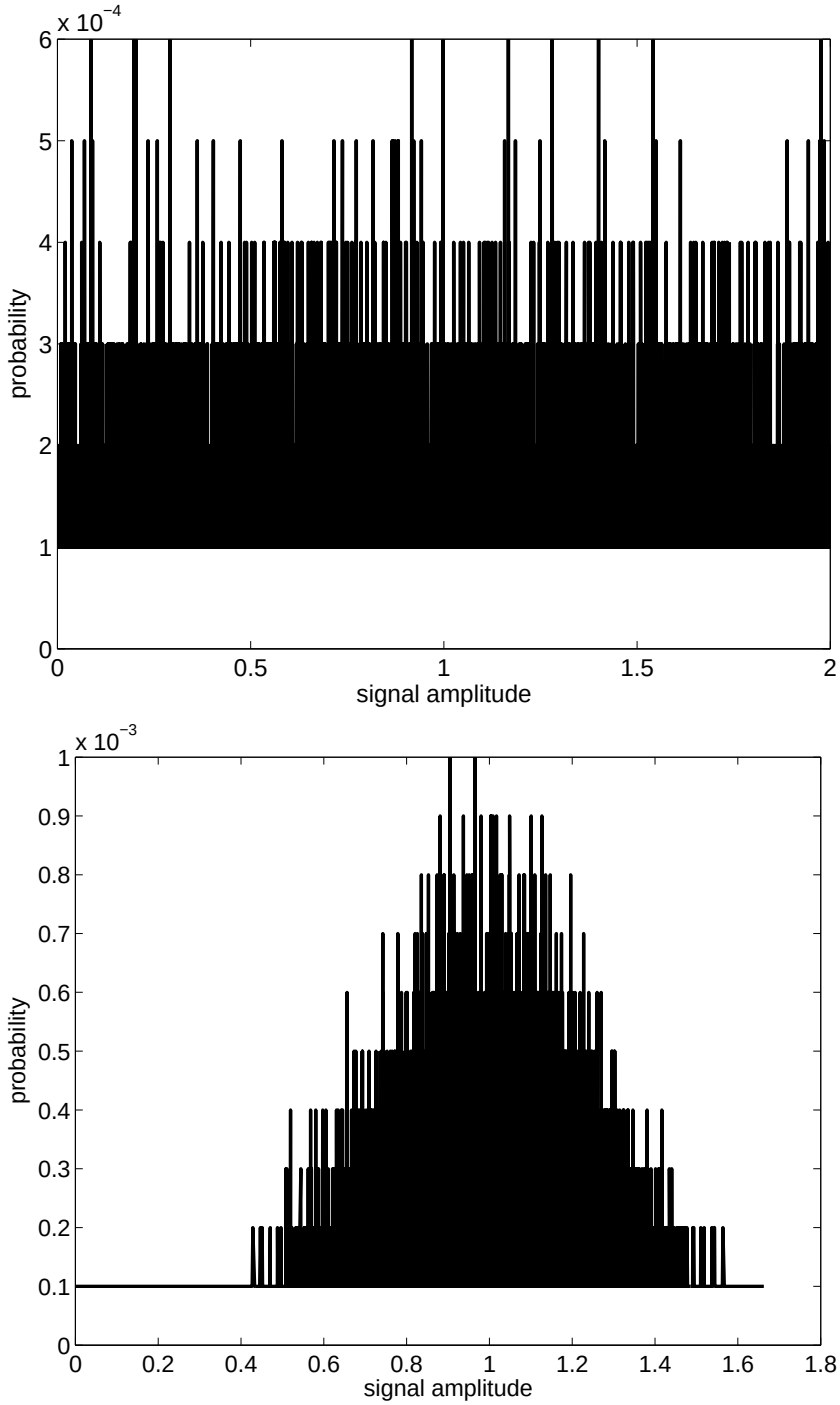

Figure 2.1: Probability distribution of a signal and its filtered output

2.2.2 Lower Sampling Frequency

As the signal is divided in bands, hence the sampling frequency required for the lower bands is less. Again, the band-pass sampling theory [9]states that for proper reconstruction of a signal of bandwidth BW and at a center frequency of f_c, it should be sampled at $2 \times BW$ frequency only. The sampling frequency does not depend on f_c. In some literature, it is proposed to down-convert the upper sub-bands of the sub-band ADC to lower bands and thus to reduce the sampling frequency for the higher bands[10],[11].

But for a signal with equal signal components in all the frequency the down-conversion process is difficult to implement in silicon. The non-idealities of filters and the down-converters make the SNR go low. So here I am doing the digitization keeping the higher sub-band at the same frequency. Though for lower frequency-bands the sampling frequency is reduced,this method calls for higher sampling frequency for the higher sub-bands but helps to reduce the effect of clock-jitter as the sample-hold faces a portion of the signal at the upper bands, unlike time-interleaved ADC, where the sample-hold faces the whole signal all the time. For lower sub-bands, the

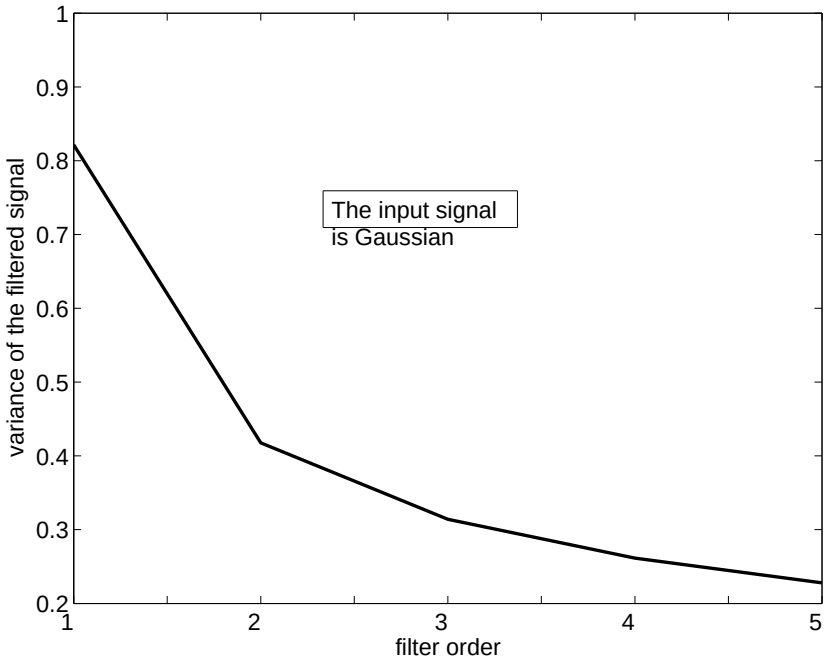

Figure 2.2: Relation between the variance of the filtered signal and the filter order

jitter is less as the jitter noise increases with the frequency of the clock.

2.2.3 Lower Jitter Effect

The jitter due to the clock is less detrimental in case of sub-band ADC, as ADCs will not face the whole signal hence the effect of jitter is much less.

2.2.4 Noise Immunity in Dead Bands

If we have a signal with lots of dead-bands in the signal spectrum, then the noise in the dead-band can be removed by filtering. Sub-band ADC helps in those cases by removing the noise in the dead-bands. This is not a fundamental virtue of splitting bands and the same performance can be achieved by filtering and cleaning the noise before using conventional ADC. But sub-band ADC does not require any additional filtering to achieve this.

2.2.5 Ease in Reconstruction

As the output is digital it is easier to reconstruct the signal from digitized signal from different paths.

2.3 System Level Simulation

The whole system is simulated in MATLAB and Simulink. Several cases are simulated and the corresponding simulation results are shown. From these system level simulations significant design insights are found out. The reason for the performance enhancement, or in some cases performance degradation is intuitively established. Before going to the simulation results, I will describe the simulation procedure.

2.3.1 Simulation Procedure

To characterize the system several inputs are used. Three-tone signal is used to investigate the effect of sub-band ADC in presence of dead-bands in the incoming signal. Chirp signal is used to see the performance when there is no dead-band in the incoming signal spectrum. The filters used are of very high order to reduce the overlap between filter contents. A second order filter transfer function is found out and is incorporated in simulink. Several such blocks are cascaded to obtain

the desired higher order transfer function. The in-built sample-hold function and quantizer of simulink are used. Quantization step is kept same for all the simulations to ensure same quantization noise for all cases. Figure 2.3 shows one such simulation setup. The system is also simulated in presence of white gaussian noise. To establish

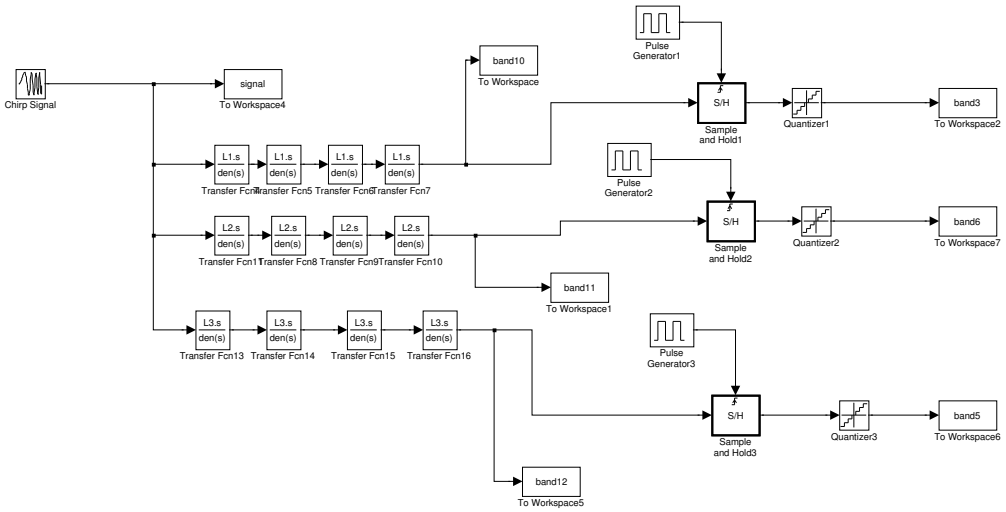

Figure 2.3: Simulink Model for sub-band ADC

its virtue over time-interleaved ADC, simulation with jittery clock is performed. For this jittery clock has been generated. To generate the jittery clock I first pass a gaussian white noise through a very narrow band filter. Then I hard-limit the signal to get jittery clock. As the filter is very narrow-band hence it passes other frequencies in small amount. The spectrum of jittery clock is shown in figure 2.4.

2.3.2 Case I:Simulation With Three-tone Signal and Noise

Here a three tone signal (frequency $50MHz$, $150MHz$ and $250MHz$) with noise is taken as input. Here we are comparing two situations. In both the situations,

we have jitter free clock. In the first case, the whole signal is sampled following nyquist rate. In the second case, the signal is broken in three bands and each band is sampled at corresponding nyquist frequency. Table 2.1 (Case-I) shows the performance enhancement in the sub-band ADC. Figure 2.5 and figure 2.6 show the spectrum of the output of sub-band ADC and the conventional ADC (without splitting the signal in bands). Here we can see that the output SNR of the sub-band ADC is more than the input SNR. Actually the sub-band ADC is cleaning the out-band noise and thus this performance enhancement is achieved. In this context, I want to make an important observation. If there can be any ADC which can sample the whole signal following nyquist criteria, then no other ADC can give better performance compared to that. The need for other ADCs roots in the fact that such high sampling frequency is not achievable.

2.3.3 Case II:Simulation With Chirp Signal

The next simulation is performed with no dead-band in the signal spectrum. For this, a chirp signal (bandlimited from d.c. to $500MHz$) is used. Here also the clocks are assumed to be jitter free. The filters are designed such that, just adding the signal in analog domain gives back the signal. Here second order filters are

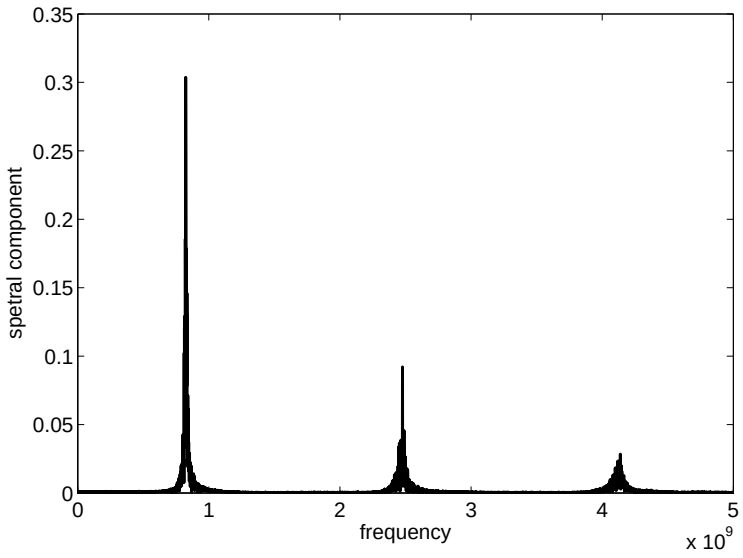

Figure 2.4: Spectrum of the Jittery Clock

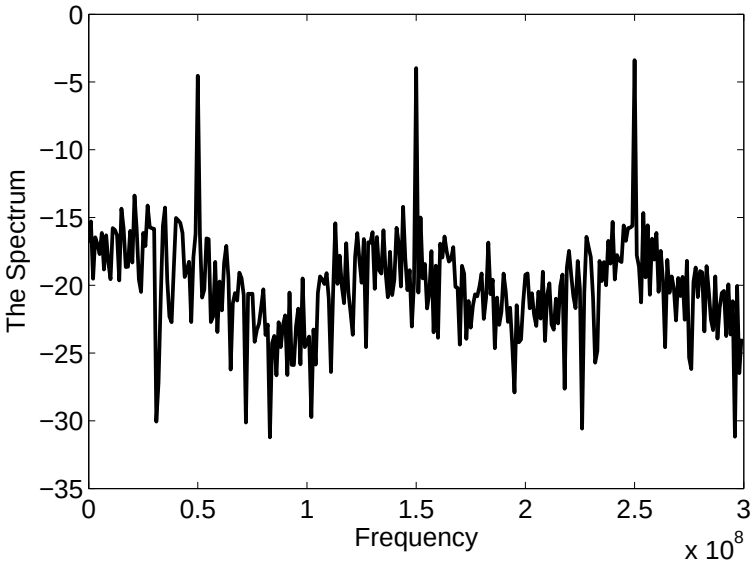

Figure 2.5: Spectrum of the output of the sub-band ADC

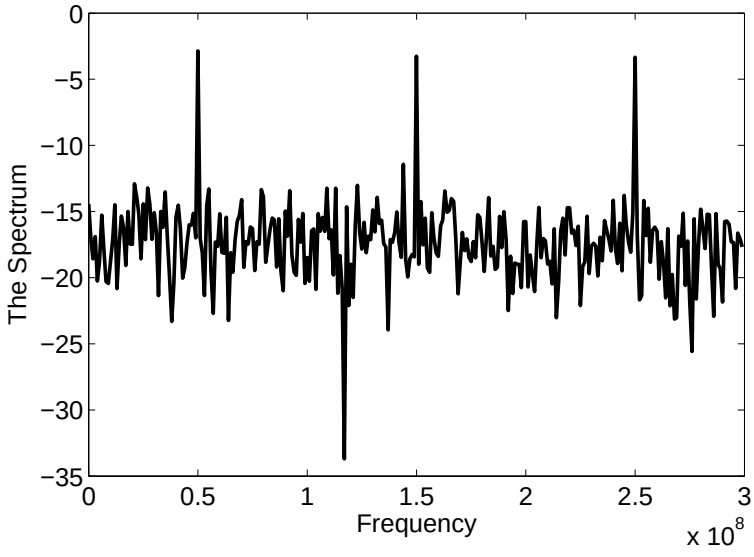

Figure 2.6: Spectrum of the output of the conventional ADC

used. This criteria of reconstruction in analog domain is very important. In fact designing higher order filters ensuring this reconstruction criteria is difficult and hence in chapter 7 some heuristic is proposed to reconstruct the signal totally.

However, here for the conventional ADC the sampling speed is taken as $2GHz$. The signal is broken into bands and the spectrum of all the bands are shown in figure 2.7. The bands are also sampled at $2GHz$. The resultant SNR is shown

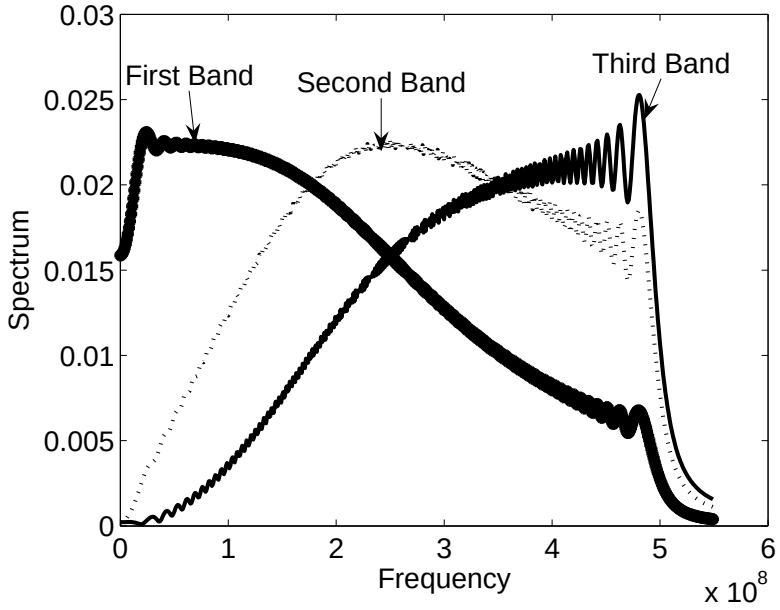

Figure 2.7: Spectrum of the three bands

in the table 2.1 (Case-II(a)). The final spectrum of the output of sub-band ADC is shown in figure 2.8. Now the first band is sampled at a frequency $1GHz$. Then the SNR is degraded and the result is tabulated in the table 2.1 (Case-II(b)). The corresponding spectrum is shown in figure 2.9.

This simulation gives a lot of insights. First of all, here we can see that if reconstruction is guaranteed in analog domain, then we will get reconstruction in digital domain also. But if the used filters are of less order, then we do not get any advantage as far as the reduced sampling frequency is concerned. In fact, reduced sampling frequency will cause degradation in SNR. So to make a good sub-band ADC, the filters should be of higher order and reconstruction in analog domain should be guaranteed.

Hence another simulation is performed, where the filter-bank used is not

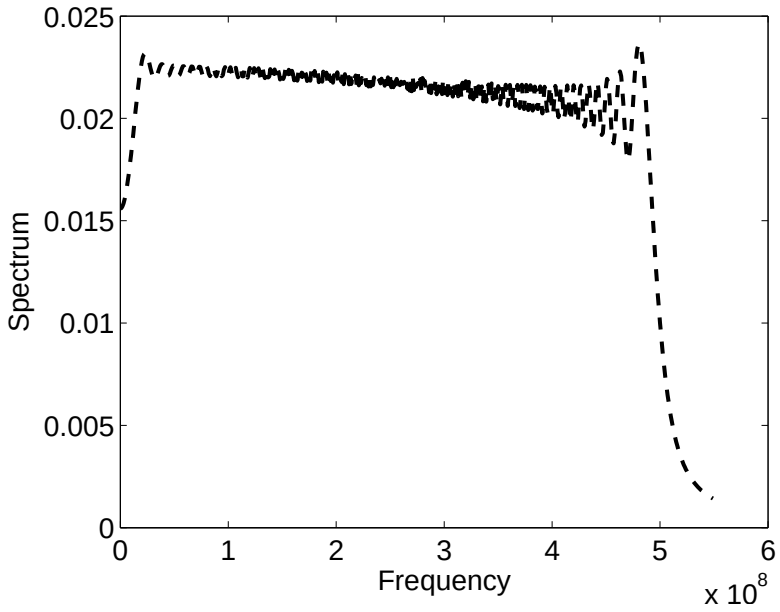

Figure 2.8: Spectrum of the final result when all the bands are sampled at $2GHz$

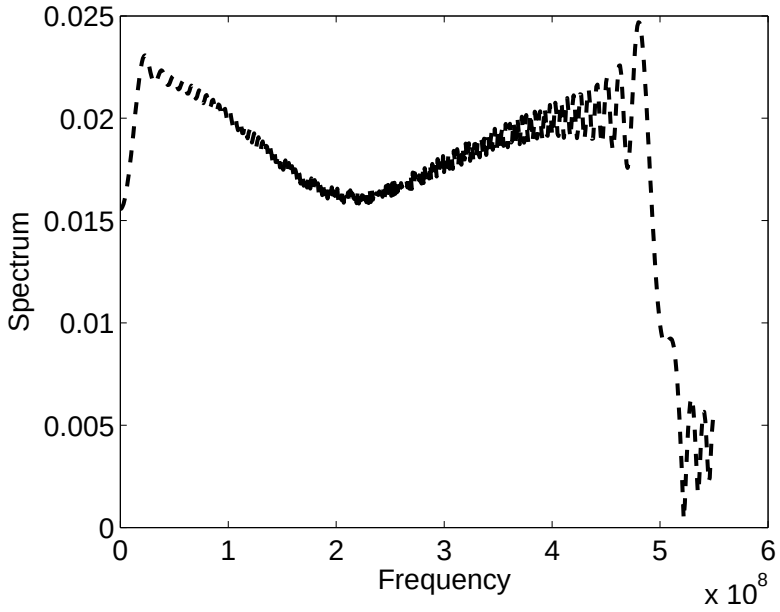

Figure 2.9: Spectrum of the final result when the first band is sampled at $1GHz$

conventional parallel filter-bank type. Rather here the signal is broken into bands by means of low-pass filters and delay banks. The architecture is shown in figure 2.10.

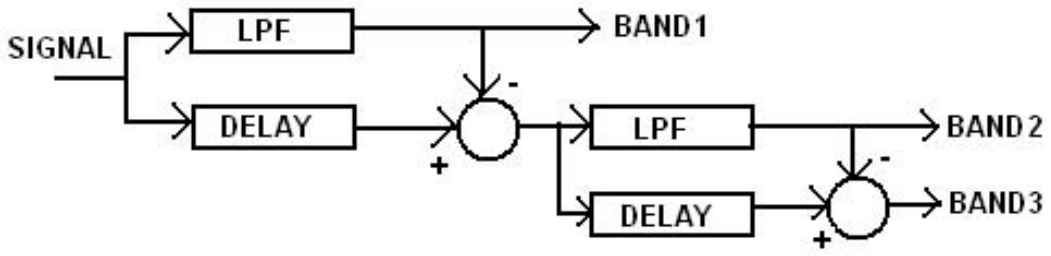

Figure 2.10: Second Filter-bank Architecture (involving only low-pass filters and delays)

The spectrum of the bands are shown in figure 2.11. Here we get same SNR

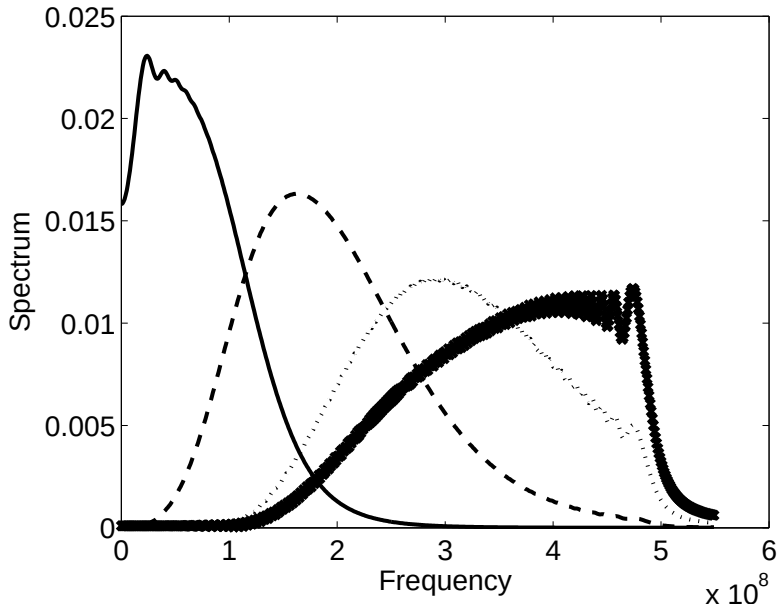

Figure 2.11: Spectrum of bands (obtained by the second type of Filter-Bank)

as conventional ADC, with less sampling frequency for the lower bands.

Table 2.1: SNR of the input signal and the output of conventional ADC and sub-band ADC for the three cases

Cases	Actual Signal	Conventional ADC	Sub-band ADC
Case-I	$7.8391dB$	$6.5545dB$	$8.8526dB$
Case-II(a)	$14.8263dB$	$13.0733dB$	$13.0733dB$
Case-II(b)	$14.8263dB$	$13.0733dB$	$12.6405dB$
Case-III(a)	$7.8391dB$	$4.7308dB$	$7.8391dB$
Case-III(b)	$50.2508dB$	$12.0720dB$	$19.3005dB$

2.3.4 Case III:Comparison With Time-interleaved ADC

So far in the simulations jitter is not considered. Those simulations are done to gain some insights about the design of sub-band ADC. In this simulation the jitter effect is considered. The simulation is performed on the three-tone signal (frequency $50MHz$, $150MHz$ and $250MHz$) with noise and without noise. Clocks used are jittery and the jitter increases with the frequency. The signal is passed through a time-interleaved ADC and a sub-band ADC.

In both cases (with noise and without noise) the signal is broken in three bands for sub-band ADC and there are three channels for time-interleaved ADC. For time-interleaved ADC sampling frequency in each channel is kept $500MHz$. For sub-band ADC, the sampling frequency at first two-bands are kept at $500MHz$ and for the third band it is kept $1GHz$. Table 2.1 (Case-III(a)) shows the performance when there is noise. Figure 2.12 and 2.13 shows the spectrum of the final output. Table 2.1 (Case-III(b)) shows the performance when there is no noise. Figure 2.14 and 2.15 shows the spectrum of the final output.

2.4 Difficulty in Practical Implementation

Though the ADC performs well in system level, it is difficult to implement it in silicon. When I tried to implement the whole system by means of analog circuit in silicon, I came across the following difficulties. In no literature people have reported the implementation the sub-band ADC in CMOS technology. So I think it is wise to mention the practical difficulties of implementation, so that the non-triviality of

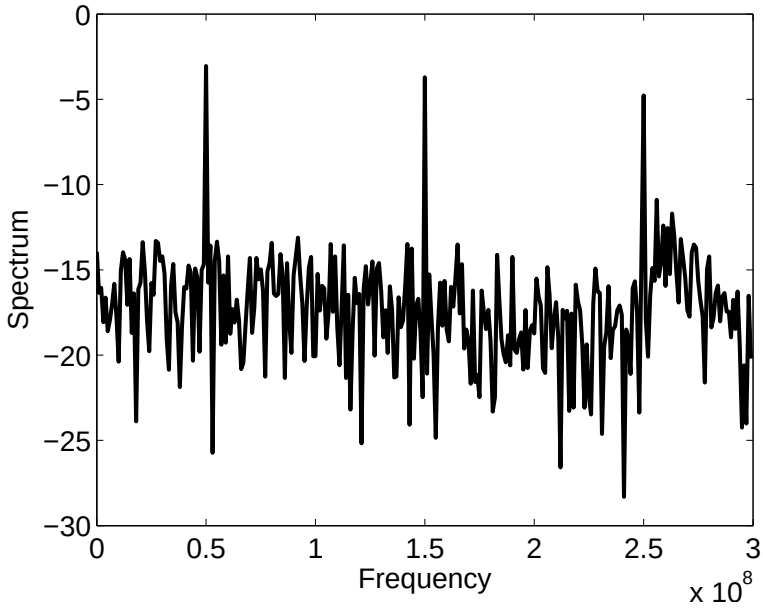

Figure 2.12: Spectrum of the output of time-interleaved ADC when the signal is noisy

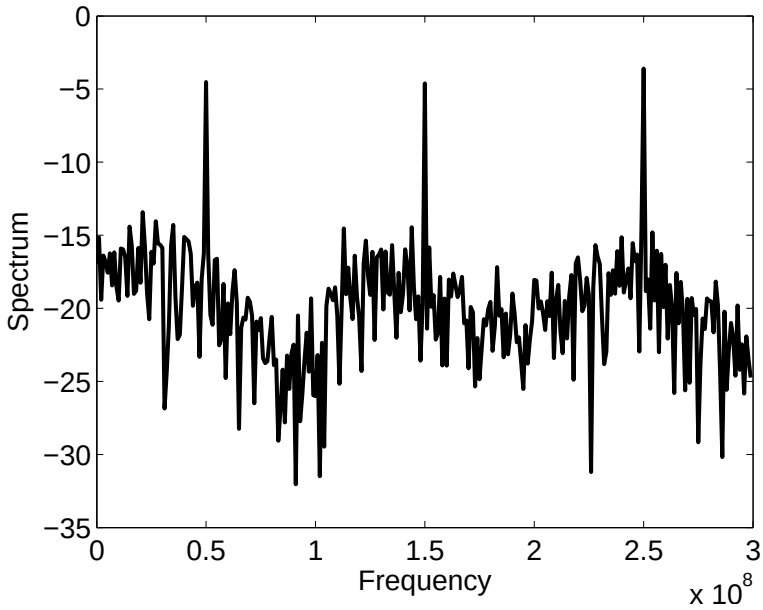

Figure 2.13: Spectrum of the output of sub-band ADC when the signal is noisy

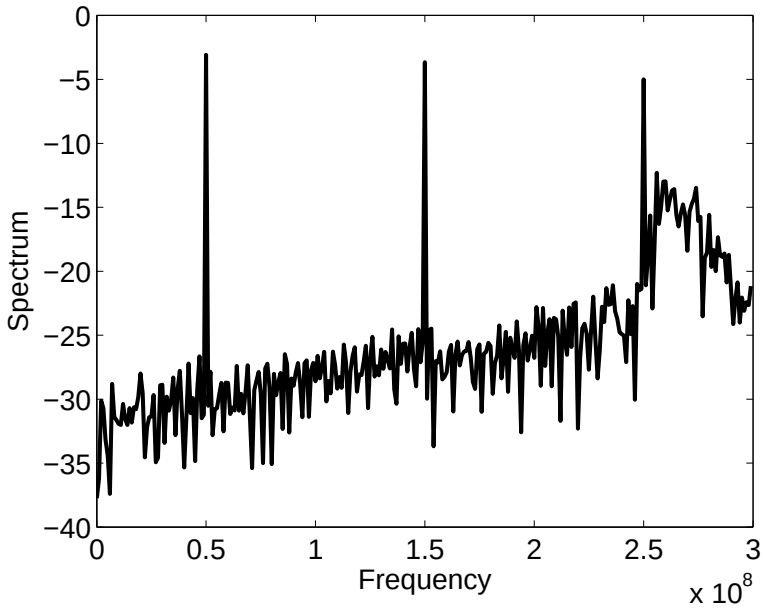

Figure 2.14: Spectrum of the output of time-interleaved ADC when the signal is noise free

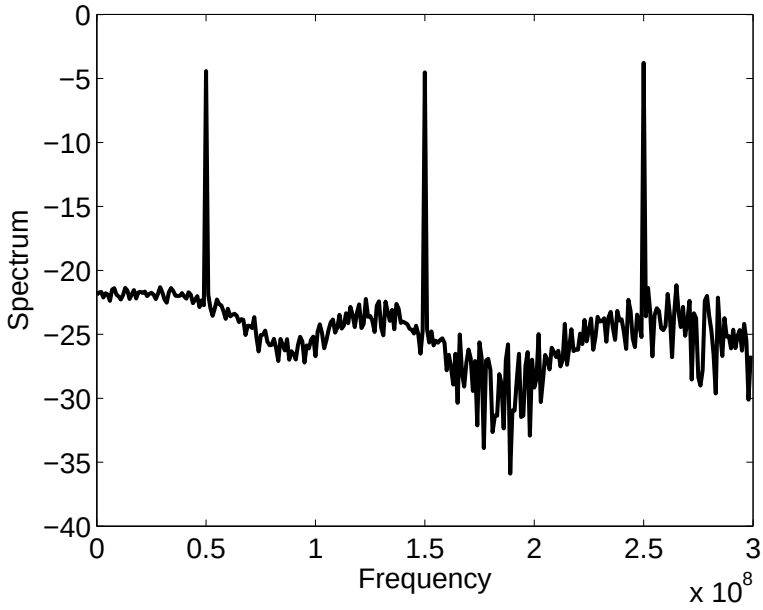

Figure 2.15: Spectrum of the output of sub-band ADC when the signal is noise free

many blocks can be established, though they may seem to be trivial in system level simulation.

1. Designing a good filter bank is the main challenge in practical implementation of sub-band ADC. The filters designed are not brick-walled and hence there will be always some overlap between different bands. This causes error in the data conversion. If dead-bands are present in the signal, then the filtering is easier. But if the spectral components are distributed in the whole frequency range, then it is difficult to do proper filtering.

2. Maintaining the linear phase characteristic of the filter is difficult. In a modified architecture(described in chapter 5), I have to design an analog delay block. There the linear phase of the filter is must and it is difficult to achieve.

3. Though down-sampling seems lucrative in system level, but this is difficult to do in silicon. After breaking the signal into bands, for the higher bands the center frequency and the bandwidth is comparable (due to finite Q of the filters) and hence down-conversion poses some problems. This down-conversion also calls for up-conversion and a little mismatch in frequency produces a large distortion.

4. Designing good sample-hold circuit as well as good comparator for ADC is also a big challenge.

In this thesis, I am mainly concerned about the implementation of the filter-bank in silicon. Two types of architectures are proposed and for implementation of the filters $g_m - C$ topology is selected. The design of delay block and subtractors are also described. Design of sample-hold circuit and comparators are discussed. As filter-banks are mainly based on transconductance-c topology, hence the transconductance is described at length in the next chapter.

Chapter 3

Transconductance

3.1 Introduction

In this chapter, the different types of implementations of transconductors are described. Brief literature survey on various transconductor structures has been reported. Different performance criteria to design appropriate transconductors have also been addressed here. Detailed analysis and design of the differential transconductor, used throughout the thesis, have also been carried out in this chapter.

3.2 Review

This section presents comprehensive review of different transconductors and operational transconductance amplifiers (OTA) which have been proposed for different applications of filters and amplifier structures. While BiCmos OTAs are receiving some attention in the literature [12], CMOS transconductors have been highlighted since CMOS technology is predominating the field of integrated circuit design for its significant use towards low power dissipation and major application in digital circuits. Some of the literatures contribute towards sub-threshold transconductor with their inherent advantage of low transconductance gain, very low power dissipation and possibility of tuning and adjustability through current bias changing at the cost of worsening noise performance [13].

Various transconductors and OTA structures, proposed in different literatures, are designed to fit with some specific application, so it is absolutely unreliable to fix one single performance criteria to design a transconductor for a specific appli-

cation. The following subsection describes the criteria, which are normally fixed to determine meaningful classification between different transconductance topologies.

3.2.1 Performance Criteria of Transconductors

The brief descriptions of each criteria for measuring the performance are given below:

1. ***Bandwidth:***One of the most important aspects of active lowpass filter design is the bandwidth of the OTA, defined as the frequency range between DC and the 3-dB point of the OTA frequency response. Empirically, the OTA must provide bandwidth at least 10 times higher than the operating frequency.

2. ***Power Dissipation:***One of the motivations for integrating analog filters is their prospective use in portable system applications where low power dissipation is a major design consideration. In addition, the increased feature density of modern CMOS technologies leads to higher power dissipation per area, which can cause reliability problems. Power dissipation of less than $100mW$ is desirable for CMOS transconductors. Power dissipation can be measured as the product of the supply voltage and the total current flowing through the supply terminal.

3. ***Total Harmonic Distortion:***In general, the output signal y(t) of a time-invariant electrical network can be expressed in terms of its input x(t) by a Taylor series expansion:

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + ... \tag{3.1}$$

   where the coefficient a_1 represents the desired linear gain of the network and coefficients $a_2, a_3, ...$ represent its distortions. In practice, the output signal $y(t)$ of a transistor-level OTA will be distorted and its maximum signal level will be dictated by the non-linear effect of practical amplifier saturation characteristics. If for example, a sinusoidal signal is applied to the input of an OTA, then harmonic distortion is defined as the root-men-square (rms) value of the ratio of all the harmonics a_n to the fundamental a_1. In differential implementation the even harmonics are eliminated. Hence the odd harmonics decide the non-linearity. As the value of the harmonics reduces with the order of the harmonics hence in most applications, we are concerned with the third

order distortion only. Mathematically, the third order distortion (THD) is measured as:

$$THD(dB) = 20log_{10}(\frac{a_3}{a_1}) \tag{3.2}$$

In some applications people are interested in total harmonic distortion and this THD can be expressed as

$$THD(dB) = 20log_{10}(\sqrt{\sum_{i=2}^{n}(\frac{a_i}{a_1})^2}) \tag{3.3}$$

where n depends on the application.

4. ***Tuning Range:***In almost every OTA reported in the literature, the transconductance gain g_m is proportional to an external DC bias voltage or current. The ability to tune the g_m is one of the main advantages of $g_m - C$ filter design, since it enables external control of filter parameters including center frequency (ω_0), cutoff frequency (ω_c) and quality factor (Q). A wide tuning range is advantageous in active integrated filter design, especially for tuning ω_c or ω_0 of the $g_m - C$ filter. The tuning range will be expressed in terms of the minimum and maximum g_m value, which can be achieved within the possible bias voltage or current range.

3.2.2 Transconductance-C Filter

Till today various analog filters in the megahertz range have been reported using both switched capacitor and continuous time techniques. In my application, I have opted for the continuous time implementation and chosen transconductance-C topology. In this subsection, I mainly discuss about the reason behind choosing transconductance-C topology by stating various advantages and disadvantages of different topologies.

Switched capacitor filters have some advantages of implementation, such as easy tunability of frequency by varying the clock frequency and easy programmability. But they have got some drawbacks as well, which make them less suitable for high frequency application. Performance of switched capacitor filters is dependent on the clock, and at high frequency due to clock jitters, switched capacitor filters are not suitable for high frequency applications. Switched capacitor filters also need pre and post filters (anti-aliasing and smoothing) which due to small clock to baseband

frequency ratio must have sharp and precise cut-off characteristics, which is not easily realizable in integrated circuits. Furthermore, switched capacitor filters also need a precise multi-phase clock signal four times or higher than the filter bandwidth.

Thus continuous time filters are always preferred for implementing high frequency filters [14], [15]. MOSFET-C and transconductance-C are the two main techniques of realizing continuous time filters. Continuous time integrator is the basic building block for both the topologies. Apart from the advantage of the high frequency operation of the filters, the implementation of high order filters is very easy in transconductance-C filters. Here there is no global feedback and all the cascaded structures have local feedback and hence stability of the higher order filters is easily achieved.

But this type of filters has some disadvantages too. Due to the lack of virtual ground and low impedance nodes, continuous time integrators are sensitive to parasitic capacitors. Capacitances at the output nodes also include the parasitic capacitances at those nodes and hence distract it from the actual application. Again these filters, due to high non-linearity, cannot filter the signal faithfully if the input signal amplitude is very large. The other drawbacks are the deviations of the g_m/C ratios due to process parameter tolerances, temperature variations, mismatches, aging etc.

3.3 Performance of the Transconductor Used

The transconductor used in my application is shown in figure 3.1. The transconductance is source-degenerated to increase the linearity [16]. Some preliminary observations (on linearity and tunability of the value of the transconductance w.r.t. the biasing current) are reported here on the transconductance. Figures 3.2 and 3.3 show the 1^{st} and 3^{rd} harmonics of the output current with the input voltage. Figure 3.4 shows the cut-off frequency of transconductance-C filter w.r.t. the biasing current. Actually by changing the current gm value is changed and that is reflected in the increased cut-off frequency of $gm - C$ filter.

The transistors used for source degeneration are $7-8$ times less size of that of the input transistor as this gives the optimum performance [1]. These two transistors are kept in linear region.

The transconductance of the transconductor is derived below: Let us assume

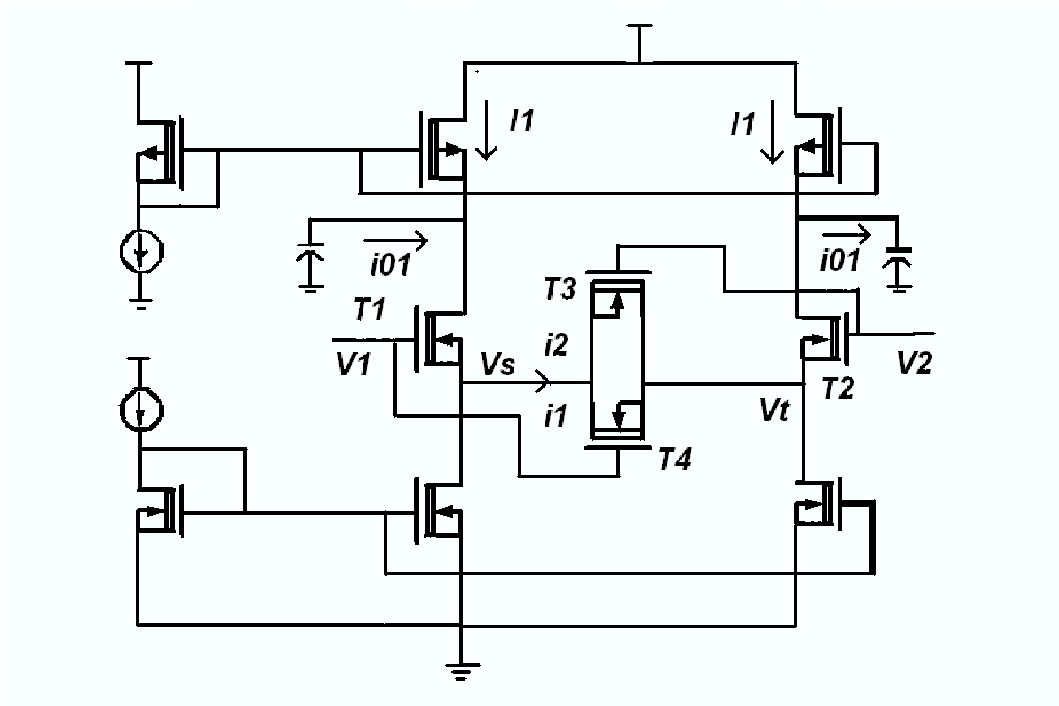

Figure 3.1: The circuit used for implementing the transconductor (differential topology)

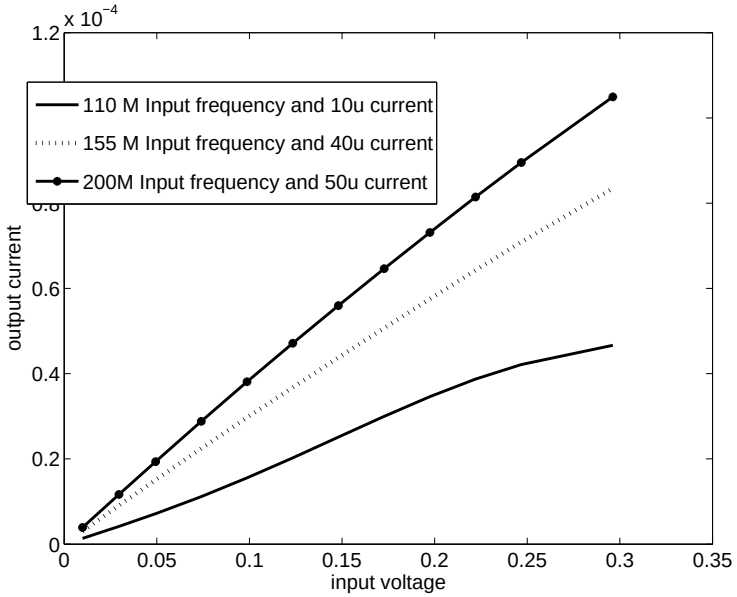

Figure 3.2: The linearity of the transconductor: first harmonic measured at different input frequencies and different control current

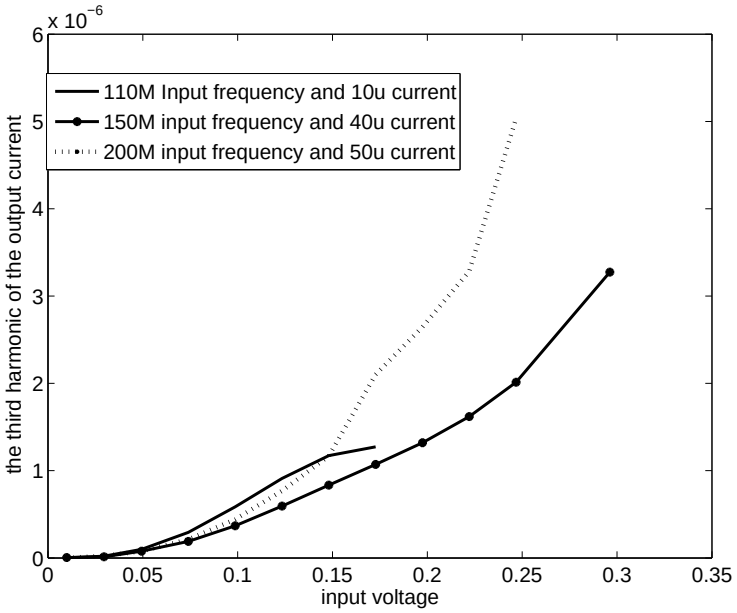

Figure 3.3: The non-linearity of the transconductor: third harmonic measured at different input frequencies and different control current

that V_1 and V_2 are differential input. Hence

$$V_1 = V_0 + \Delta V; V_2 = V_0 - \Delta V; \tag{3.4}$$

The current in two branches can be written as

$$I_1 + i_{01} = \frac{\beta_1}{2}(V_1 - V_s - V_{th1})^2 \tag{3.5}$$

$$I_1 - i_{01} = \frac{\beta_2}{2}(V_2 - V_t - V_{th2})^2 \tag{3.6}$$

where $\beta = \mu C_{ox}(\frac{W}{L})$. The length of T_1 and T_2 are taken 1μ. Hence the effect of λ can be neglected. Again as T_3 and T_4 are in linear region, hence we can write

$$i_1 = \frac{\beta_3}{2}(2(V_1 - V_t - V_{th3})(V_s - V_t) - (V_s - V_t)^2) \tag{3.7}$$

$$i_2 = \frac{\beta_4}{2}(2(V_2 - V_t - V_{th4})(V_s - V_t) - (V_s - V_t)^2) \tag{3.8}$$

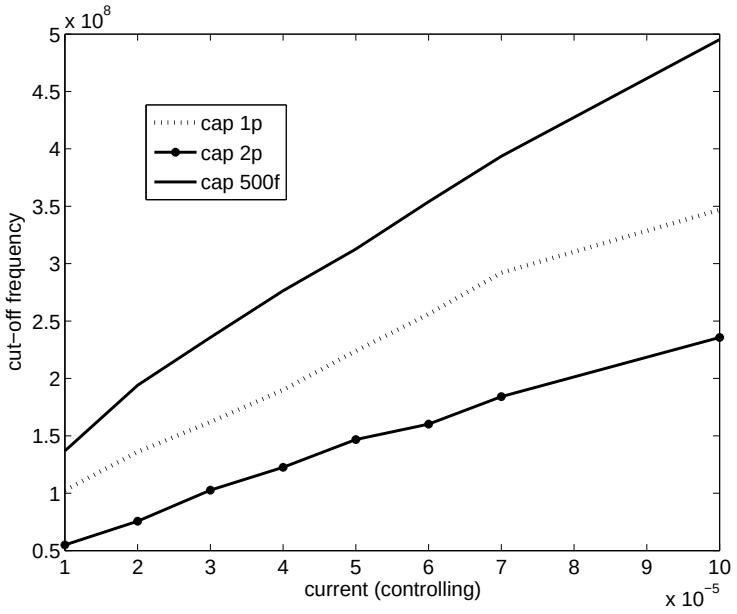

Figure 3.4: The tunability of the transconductance with controlling current (measured by the cut-off frequency of the first order g_mC low-pass filter

But

$$i_1 + i_2 = i_{01} \tag{3.9}$$

Adding equations 3.7 and 3.8 and assuming T_3 and T_4 are same we get

$$i_{01} = \beta_3((V_1+V_2-2V_t-2V_{th3})(V_s-V_t)-(V_s-V_t)^2) = \beta_3(V_s-V_t)(2V_0-(V_s+V_t)-2V_{th}) \tag{3.10}$$

Subtracting 3.6 from 3.5 and assuming T_1 and T_2 are same we get

$$i_{01} = \frac{\beta_1}{4}(2V_0 - (V_s + V_t) - 2V_{th})(2\Delta V - (V_s - V_t)) \tag{3.11}$$

Dividing equations 3.10 and 3.11 we get

$$(V_s - V_t) = \frac{2\Delta V \beta_1}{\beta_1 + 4\beta_3} \tag{3.12}$$

Now from equations 3.5 and 3.6 we get

$$2\Delta V - (V_s - V_t) = \sqrt{\frac{2(I_1 + i_{01})}{\beta_1}} - \sqrt{\frac{2(I_1 - i_{01})}{\beta_1}} \tag{3.13}$$

By binomial expansion and a little algebra we get

$$g_m = \frac{i_{01}}{V_1 - V_2} = \frac{4\sqrt{2}\beta_1\beta_3\sqrt{I_1}}{(\beta_1 + 4\beta_3)\sqrt{\beta_1}} \tag{3.14}$$

Hence by increasing β and bias current I_1 the transconductance can be increased. This helps in designing filters with high cut-off frequency.

Chapter 4

Filter-bank:First Architecture

4.1 Introduction

To divide the signal into several frequency-bands, a filter-bank is required. As explained earlier, the filter-bank is the most important and critical part of sub-band ADC. The filter-banks should divide the signal in bands with very less overlap and all the bands together should contain the whole signal. Otherwise, after conversion, recombination of different bands will create problem. In this chapter the architecture of the filter-bank is described. The advantage and disadvantages of this architecture is also explained. The implementation of the filters is described and the performance of the filters are reported.

4.2 Description of Architecture

The first architecture of the filter-bank consists of several parallel band-pass filters. Figure 4.1 shows the architecture of the filter-bank. In my project, I have divided the whole signal in two bands. In this architecture, ideally we need n filters for dividing the signal in n bands. Among those filters the first one is low-pass filter and all others are band-pass filters. But due to the non-ideality of filters and overlap between bands to split the signal in two bands, we require some more filters. So in my analysis I have three filters and I get three bands, which are overlapping. The filters should satisfy certain criteria:

1. The filters should have zero pass-band ripple.

2. The filters should have sharp roll-off so that the overlap between bands are less.

3. The filters should be linear w.r.t. the input signal amplitude and should be able to handle signals with high amplitude.

4. They should have linear phase in the pass-band.

5. The filters should have flat band response for a large band-width.

4.3 Implementation and Performance of Filters

The filters are implemented in $g_m - C$ topology [17],[18]. The basic filter topology made by $g_m - C$ is shown in the figure 4.2. The transfer function of this filter is

$$V_{out}(s) = \frac{s^2 C_1 C_2 V_c(s) + s C_1 g_{m2} V_b(s) + g_{m1} g_{m2} V_a(s)}{s^2 C_1 C_2 + s C_1 g_{m2} + g_{m1} g_{m2}} \tag{4.1}$$

Making $V_a = V_{in}$ and $V_b = V_c = 0$ the filter acts as a low-pass filter; $V_b = V_{in}$ and $V_a = V_c = 0$ makes the filter act as a band-pass filter and $V_c = V_{in}$ and $V_a = V_b = 0$ makes the filter act as a high-pass filter. Following equations show the performance measure of the filters.

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}}; Q = \sqrt{\frac{C2}{C1}} \tag{4.2}$$

As the transconductor designed here is differential hence the single ended filter topology, as shown in figure 4.2, is converted into a double-ended filter (as shown in figure 4.3). The second order low-pass, band-pass and high-pass filter responses are

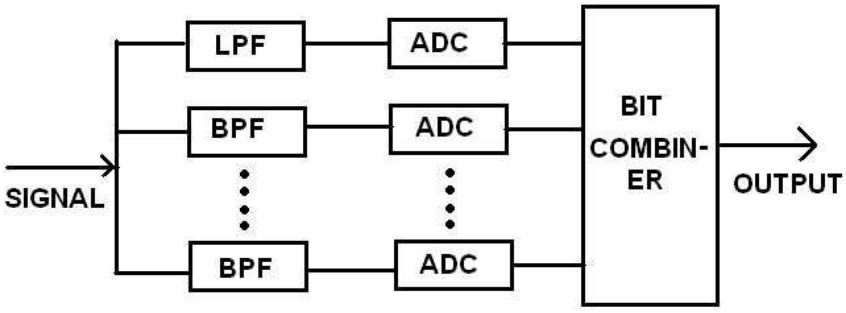

Figure 4.1: Block-Diagram of Filter-bank Architecture

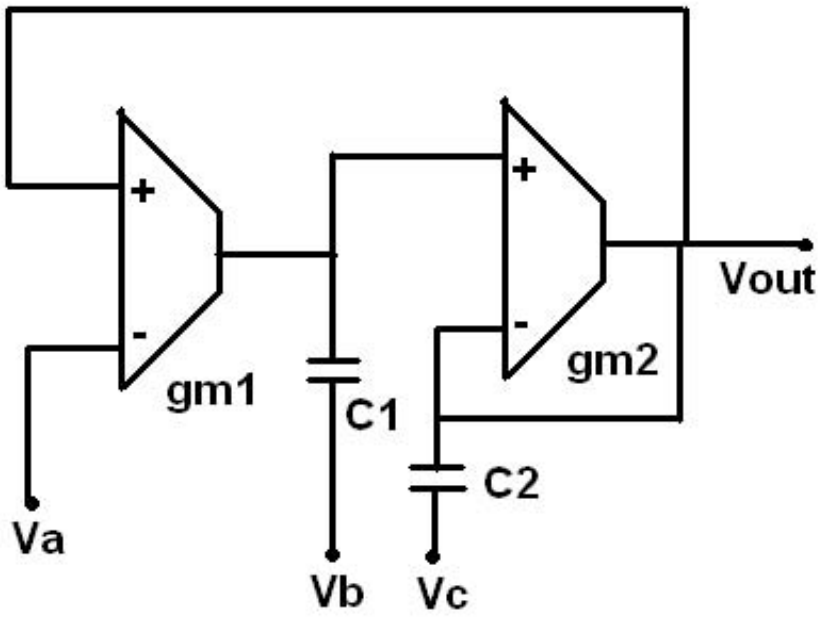

Figure 4.2: Block-Diagram for gm-c filter (single-ended)

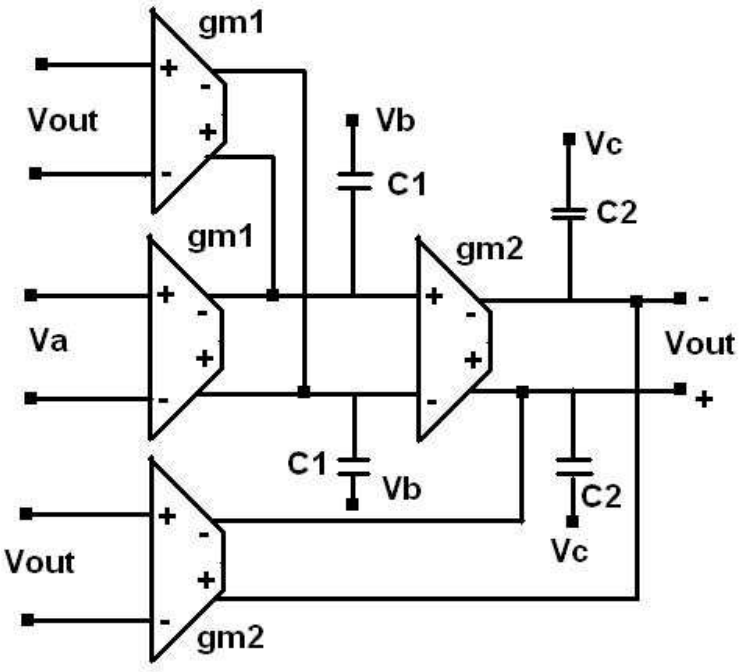

Figure 4.3: Block-Diagram for gm-c filter (double-ended)

shown in figure 4.4, 4.5 and 4.6. In my application, I tried to break the signal in two

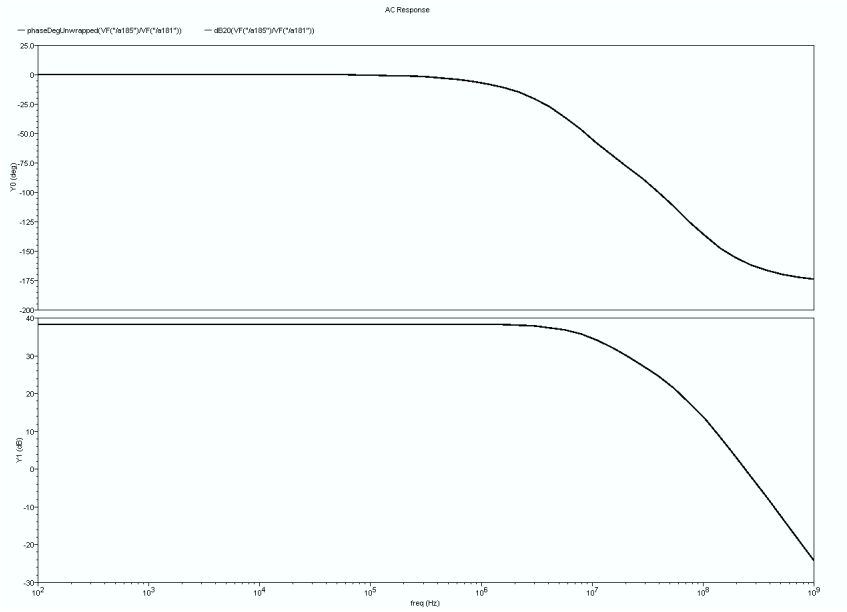

Figure 4.4: Second-order Filter Low-pass Response (Upper one is Phase and Lower one is Magnitude Response)

bands and hence I needed two filters. But as explained earlier, due to non-ideality of the filter-bank, I need to keep another filter. All three filters are designed in CMOS and simulated in CADENCE in commercially available $0.18\mu m$ technology. The order of the low pass filter designed is 8 and that of the band-pass filters are 10. The low pass filter has a cut-off frequency of $100MHz$. The center frequency and bandwidth of the first band-pass filter are $130MHz$ and $50MHz$ and those of the second band-pass filter are $200MHz$ and $80MHz$. The filter ac responses are shown in the figures 4.7, 4.8 and 4.9. To characterize the system, chirp signal is used as input. This signal is used as it has all the frequency components in a specified band. Figure 4.10 shows the spectrum of the chirp signal used for characterization. This signal is passed through all the filters and the output of each filter (both the waveform and the spectrum) are shown in figures 4.11, 4.12, 4.13, 4.14, 4.15, 4.16.

The linearity (w.r.t. the input signal amplitude) of the filters are measured. Figures 4.17, 4.18, 4.19 show the output amplitude versus the input amplitude for

these three filters. It can be noted that the low pass filter has more linearity, compared to the band-pass filters. The phase-response of the filters are also not linear. In fact, as we increase the order of the filter, the linearity decreases and phase also becomes non-linear. To get same roll-off the order of the low-pass filter is less compared to that of the band-pass filter. That is why significant linearity can be achieved in low-pass filters. But this architecture can break the signal in bands. The filters are of higher order and hence the foll-off is good. This architecture has many disadvantages (which will be explained in next chapter) and hence a new architecture is studied.

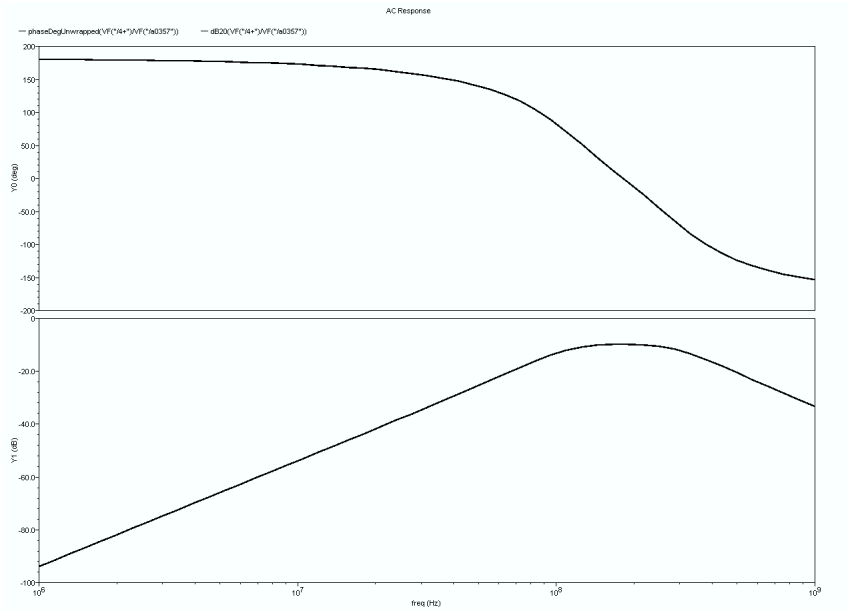

Figure 4.5: Second-order Filter Band-pass Response (Upper one is Phase and Lower one is Magnitude Response)

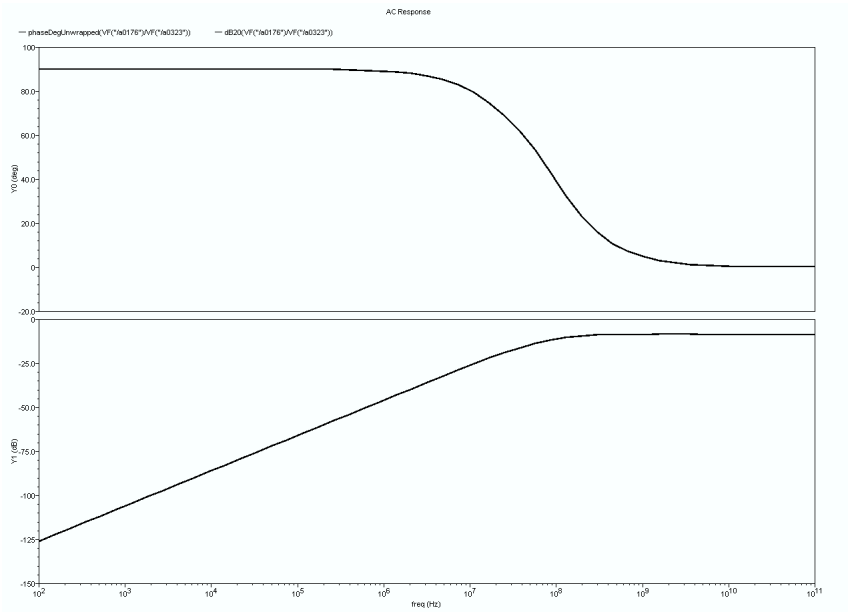

Figure 4.6: Second-order Filter High-pass Response (Upper one is Phase and Lower one is Magnitude Response)

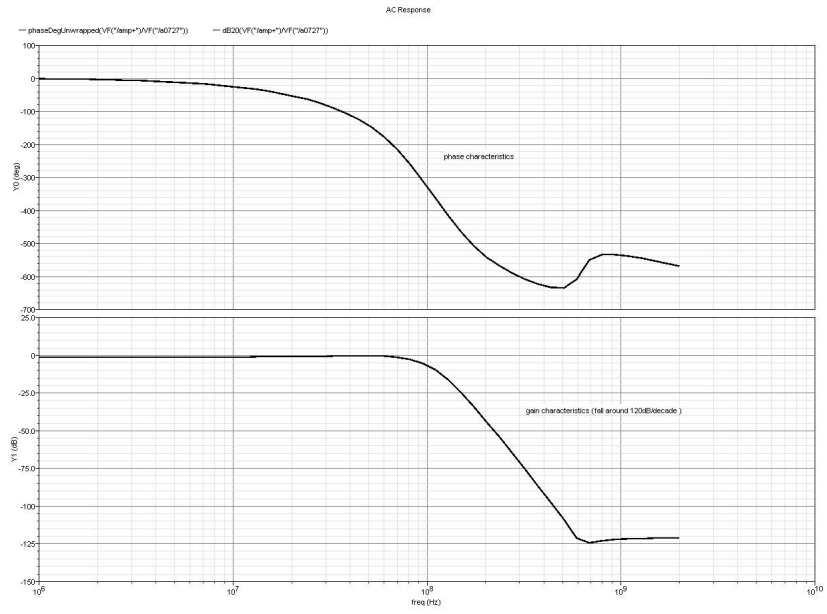

Figure 4.7: Frequency Response (Phase and Magnitude) of the low-pass filter

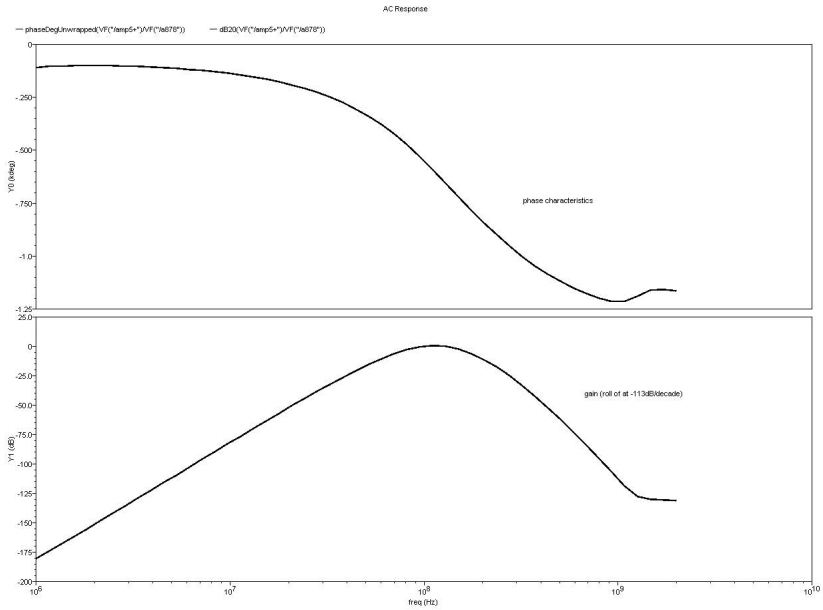

Figure 4.8: Frequency Response (Phase and Magnitude) of the first band-pass filter

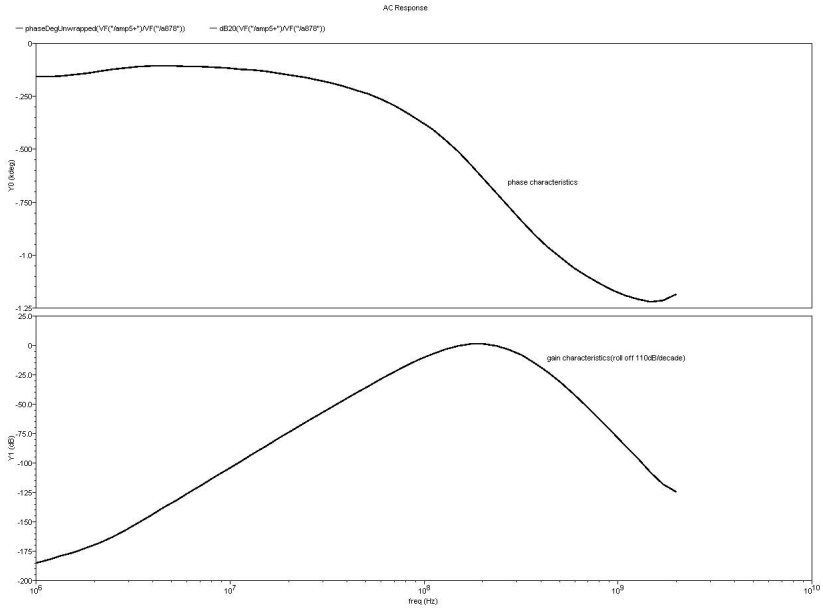

Figure 4.9: Frequency Response (Phase and Magnitude) of the second band-pass filter

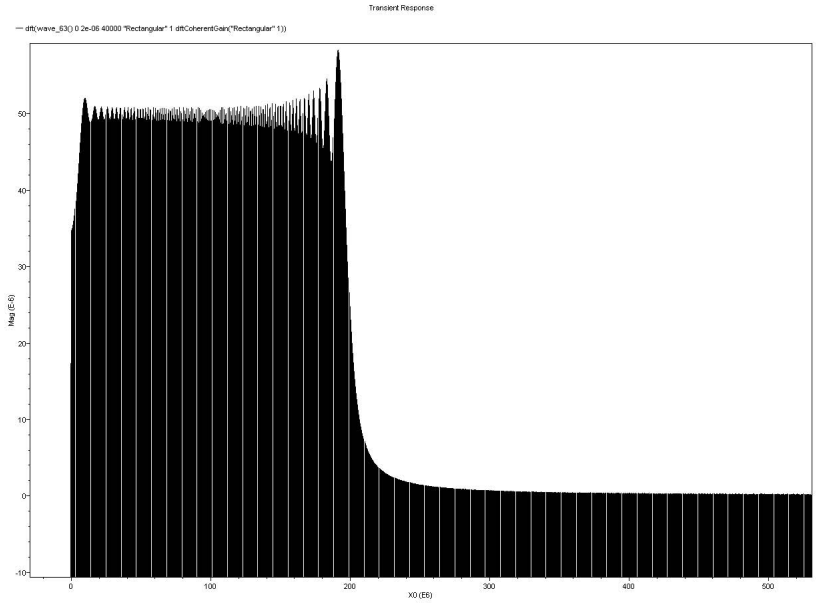

Figure 4.10: Spectrum of the input chirp signal to the filter-bank

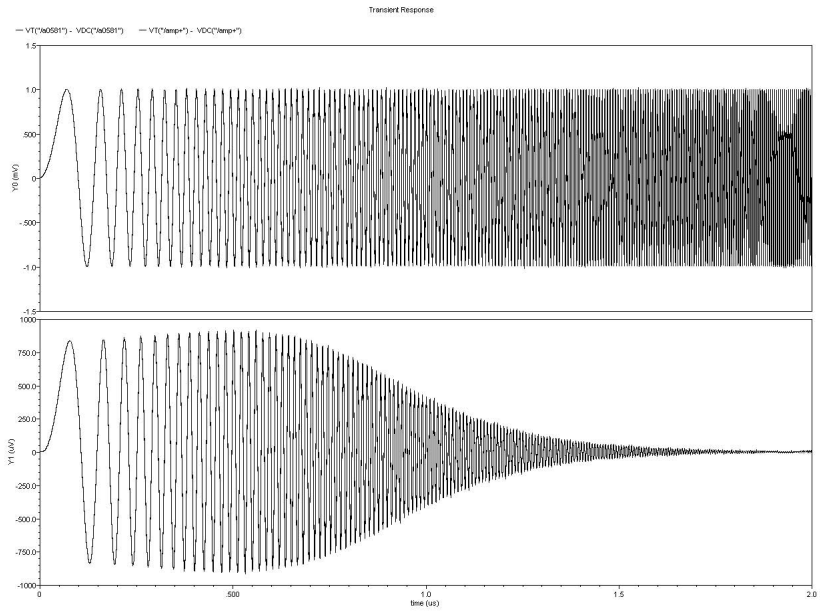

Figure 4.11: The waveform of the original signal and the signal obtained after passing the chirp signal through the low-pass filter

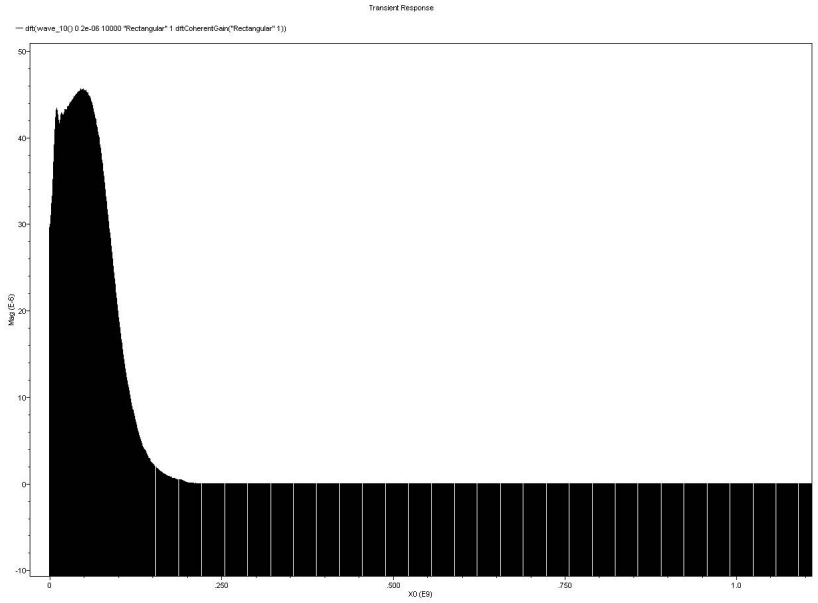

Figure 4.12: The spectrum of the output of the low-pass filter (the first band)

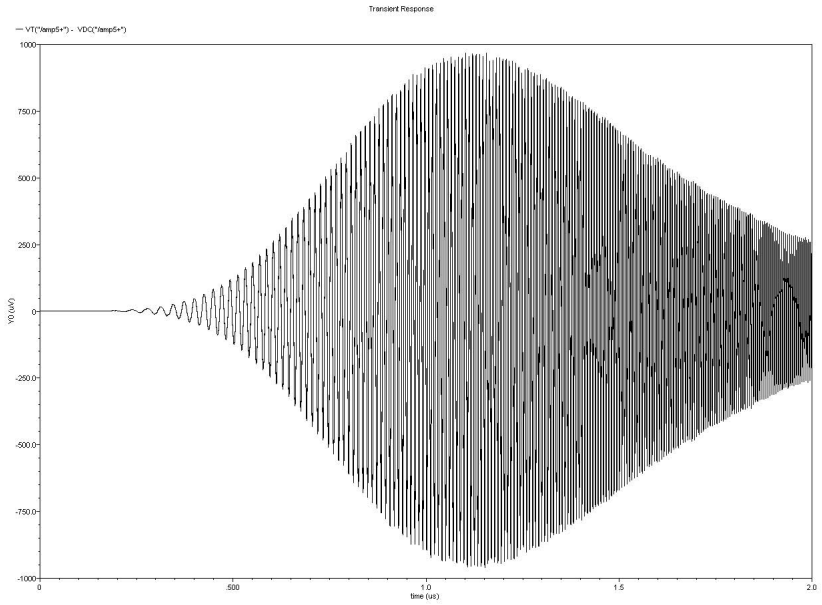

Figure 4.13: The waveform of the signal obtained after passing the chirp signal through the second band-pass filter (the second band)

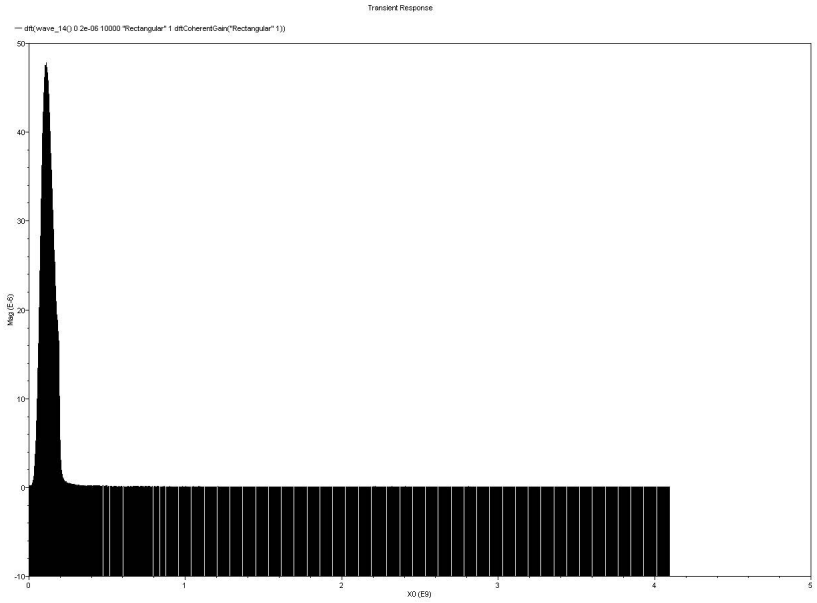

Figure 4.14: The spectrum of the output of the second bandpass filter (the second band)

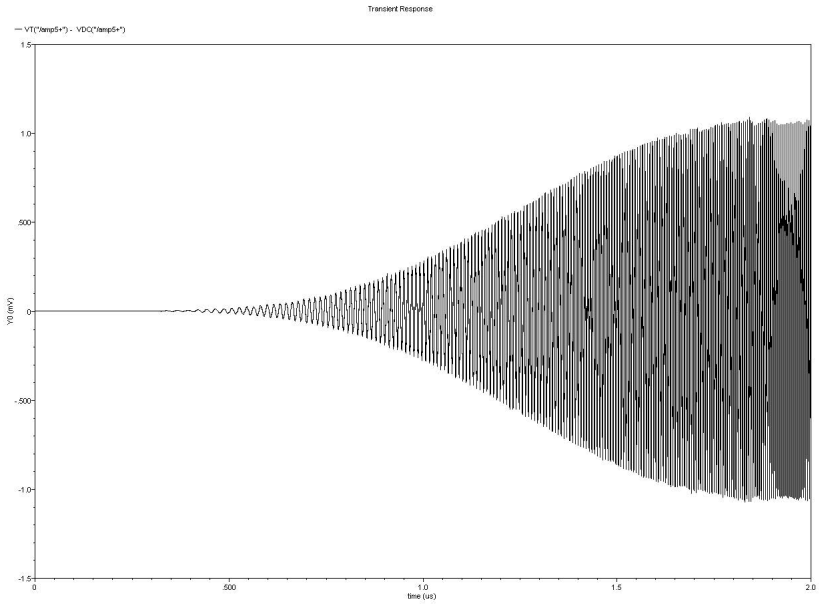

Figure 4.15: The waveform of the signal obtained after passing the chirp signal through the second band-pass filter(the third band)

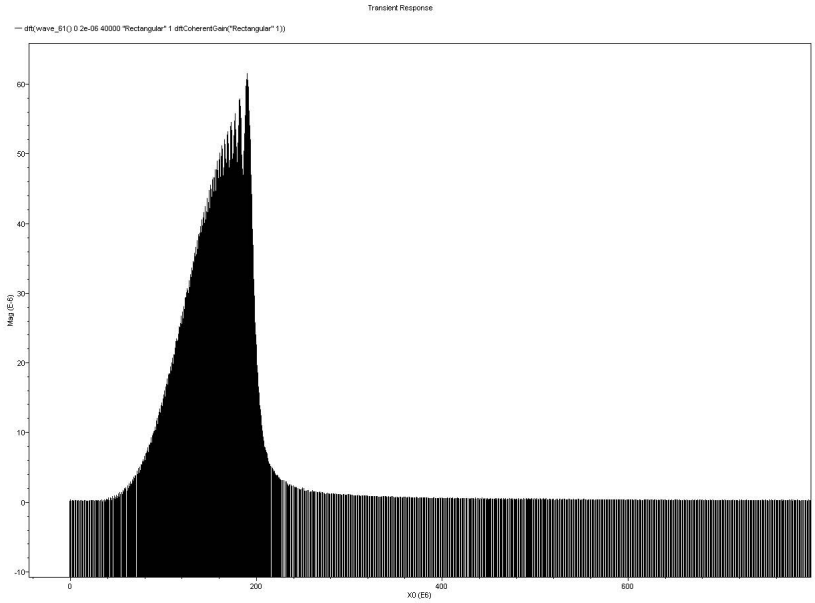

Figure 4.16: The spectrum of the signal obtained after passing the chirp signal through the second band-pass filter(the third band)

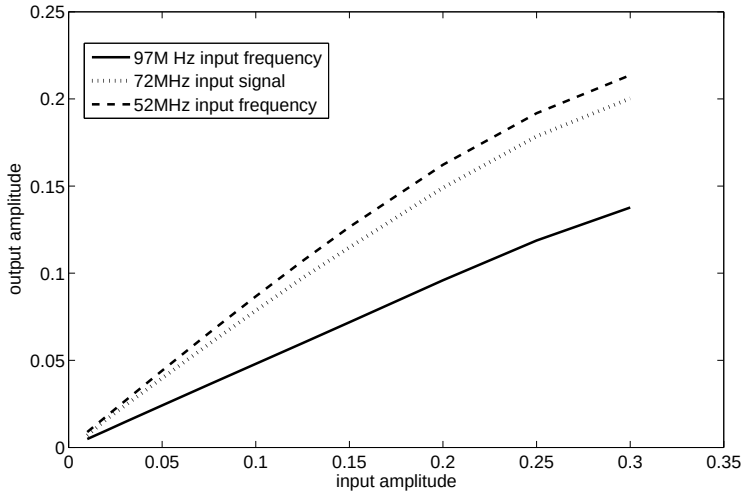

Figure 4.17: The linearity of the low pass filter

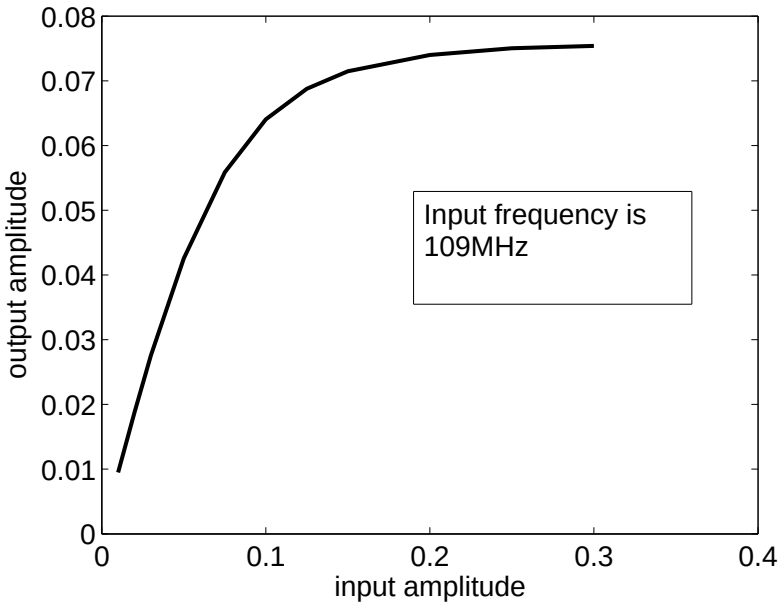

Figure 4.18: The linearity of the first band pass filter

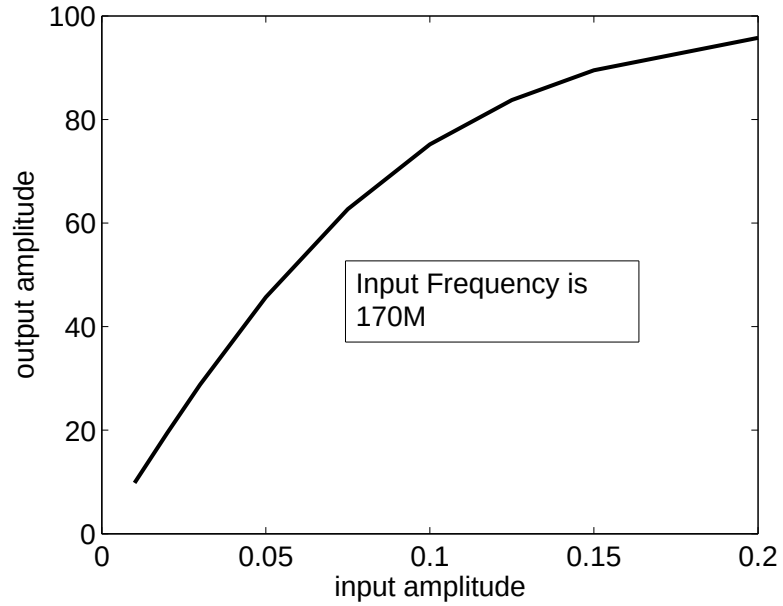

Figure 4.19: The linearity of the second band pass filter

Chapter 5

Filter-bank:Second Architecture

5.1 Introduction

Due to many disadvantages (both in system level as well as from the perspective of implementation in silicon) this new architecture is proposed. This architecture has many advantages over the previous architecture. But implementation of this architecture is also much involved as it requires design of an analog delay block. In this chapter, the architecture is described and the implementation is elaborated.

5.2 Architecture and Its Advantages

Here without using any band-pass filter the signal is broken into bands by means of low-pass filters (of different cut-off frequencies) and delay blocks. The schematic of the architecture is shown in the figure 2.10 and this is already discussed in chapter 2. Here different bands are subtracted from original signal to get the residual signal and filtering is done on the residual signal. The virtue of this architecture over the previous one is as follows:

1. The reconstruction in analog domain is guaranteed if the delays provided by the delay block and the filter are same. In the previous architecture the bands are overlapping and hence in analog domain the reconstruction is not guaranteed.

2. The number of Low pass filters and delay blocks required is $n-1$ each if we want to break the signal in n bands. No additional filters are required for the

overlap band. But in Band-pass filter-bank (the previous architecture) extra filters are needed.

3. Circuit complexity of delay blocks are much less than the band pass filters. Hence this architecture is less complex.

4. As only low pass filters are used, the order of the filters is much less as the roll- off of the low pass filters is more than that of the band-pass filters (order being same as that of the low-pass filters).

5. In band-pass filter it is difficult to get a flat pass-band for a wide range of frequency. It is easy to get this in case of low-pass filters.

6. Low-pass filters are better than the band-pass filters in term of linearity w.r.t. input signal amplitude as well as phase linearity.

Although this architecture has many virtues, it is difficult to design an active delay block which can give precise delay.

5.3 Design of Delay Block & Subtractor

Designing a proper delay bock in analog is very difficult as ideal delay is an infinite order system. Laplace domain representation of delay by T time-unit is e^{-sT}. This infinite series can be approximated upto first order as

$$e^{-sT} = \frac{1 - sT/2}{1 + sT/2} \tag{5.1}$$

In analog domain to get such a transfer function the circuit (as shown in figure 5.1 is used. The idea is inspired by [19] but that was implemented in BJT. Here I have used MOS to design the delay. This is a source degenerated common source amplifier with a miller capacitance C_e. The following set of equations are written to get the approximate transfer function. All the capacitances except C_e are parasitic device capacitances.

$$\frac{V_x + V_p - V_{in}}{R_i} + V_x C_{GS} s + (V_x + V_p - V_{out}) C_e s = 0 \tag{5.2}$$

$$(V_{out} - V_x - V_p) C_e s + gm V_x + V_{out}(\frac{1}{R_d} + C_{DB} s) = 0 \tag{5.3}$$

$$R_s(V_x C_{GS} s + gmV_x) = V_p \tag{5.4}$$

These equations are solved to get the final result.

$$\frac{V_{out}}{V_{in}} = \frac{R_d(-gm + (C_e + gmC_eR_s)s + C_eC_{GS}R_s s^2)}{R_dR_iR_sC_{GS}C_eC_{DB}s^3 + (R_iR_dA + R_sB)s^2 + Cs + (1 + gmR_s)} \tag{5.5}$$

where

$$A = C_{GS}C_{DB} + C_{DB}C_e + C_eC_{GS} \tag{5.6}$$

$$B = R_iC_eC_{GS} + R_d(C_eC_{GS} + C_{GS}C_{DB}) + R_iR_dgmC_{DB}C_e \tag{5.7}$$

$$C = R_i(C_{GS}+C_e+gmC_eR_d)+R_d(C_e+C_{DB})+R_s(R_iC_egm+C_{GS}+C_egmR_d+gmC_{DB}R_d) \tag{5.8}$$

Now in our case $R_i = 0$ and hence the third order equation is reduced to second-order equation with the second-order term having the coefficient as $R - sR_iC_eC_{GS} + R_d(C_eC_{GS}+C_{GS}C_{DB})+R_iR_dgmC_{DB}C_e$. This term is small for small values of R_s,R_d and C_e. Again the second-order term in numerator is also small. So the equation

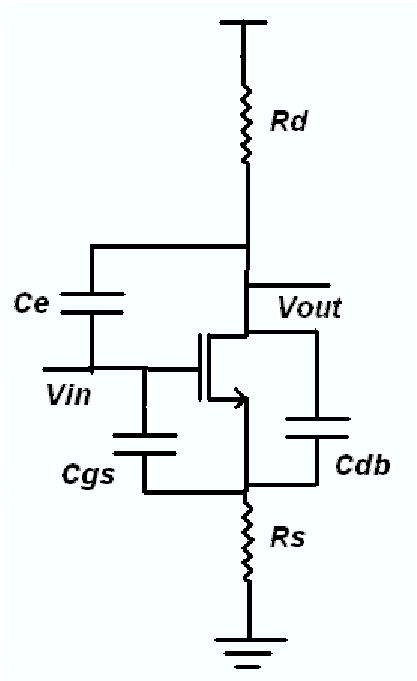

Figure 5.1: The circuit used for implementing delay in analog domain

can be written as

$$\frac{V_{out}}{V_{in}} = \frac{R_d(-gm + (C_e + gmC_eR_s)s)}{Ds + (1 + gmR_s)} \tag{5.9}$$

where

$$D = R_d(C_e + C_{DB}) + R_s(C_{GS} + C_egmR_d + gmC_{DB}R_d) \tag{5.10}$$

as $R_i = 0$. Now to have a good approximation of the equation 5.9 required condition is

$$1 + gmR_s = gmR_d \tag{5.11}$$

and the delay provided by the delay block is $2R_dC_e$. The linear phase of the delay block is mainly dependent on the equation 5.11 and the approximation (i.e., the third and the second order terms are much less compared to the first order terms). This gives the design criteria for the delay block.

- R_d and R_s should not be kept very high. They should maintain the condition given by equation 5.11. In my design, I have taken R_d and R_s to be 251Ω and 8Ω.
- The capacitance C_e also should be kept low. In my design it is kept $4.8pF$.
- The condition in equation 5.11 enforces gain to be 1. Hence no additional requirement is necessary to make the delay unity-gain. So the transistor sizing is not very crucial. Large size of transistor is avoided to reduce the device capacitances.

After the signal is delayed the already filtered signal is to be subtracted from the delayed signal. For subtractor the following circuit 5.2 is designed. This subtractor, which is nothing but a difference amplifier cannot handle large amplitude signal. The following analysis shows the reason and as a support of the analysis, some plots are also given. If the input signals are like

$$V_{in1} = V_0 + \Delta V; V_{in2} = V_0 - \Delta V \tag{5.12}$$

then,

$$I_1 = \frac{\beta_1}{2}(V_0 + \Delta V - V_p - V_{th1})^2 \tag{5.13}$$

$$I_2 = \frac{\beta_2}{2}(V_0 - \Delta V - V_p - V_{th1})^2 \tag{5.14}$$

So the a.c. output voltage V_{out} can be written as

$$V_{out} = \beta R(\Delta V)^2 \tag{5.15}$$

where $\beta_1 = \beta_2 = \beta$. But if we do linear analysis, then a.c. output should come zero as $V_{out} = gm_1\Delta V - gm_2\Delta V = 0$ if $gm_1 = gm_2$. Figure 5.3 shows the nonlinearity of the subtractor when proper differential signal is given to the subtractor.

This analog delay produced is very much process dependent. To make the delay tunable, the resistances R_d and R_s are replaced by a PMOS and an NMOS, with biasing. Then R_d is provided by $1/g_{ds}$ of the PMOS and R_s is provided by $1/g_{ds}$ of the NMOS. They can be changed by changing the voltage at the gate. If the transistors are kept in linear region, then

$$\frac{1}{g_{ds}} = \frac{1}{\beta(|V_{GS}| - |V_{th}|)} \tag{5.16}$$

where V_{GS} is the gate-to-source voltage of the MOS.

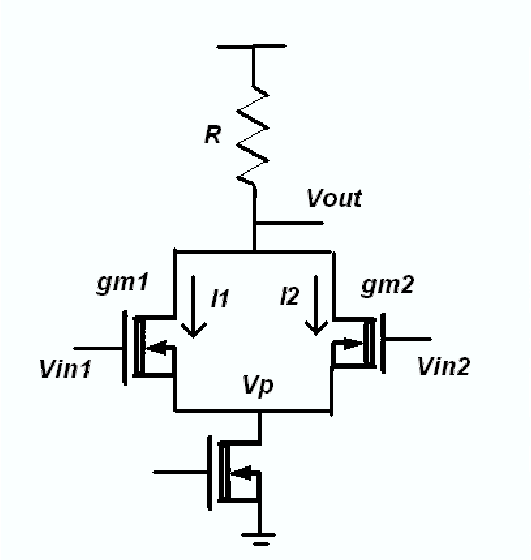

Figure 5.2: The circuit used for implementing subtractor in analog domain

Often the delay provided by one of this delay stage is not sufficient. For this the delay stages are to be cascaded. Cascading stages is difficult as due to high miller capacitance the previous stage is loaded by the next stage. To cascade two stages a source follower is used as a buffer (figure 5.4). But due to miller capacitance the buffer faces a capacitance C_m. If the resistance of the NMOS (in the source follower) is R then the transfer function of the source follower can be written as

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_m R}{1 + g_m R + R C_m s} \tag{5.17}$$

So the cut-off frequency of the source-follower is $\frac{1+g_m R}{RC_m}$. I have to increase the bandwidth to get good delay block. Band-width can be increased by increasing g_m or be decreasing C_m. To increase g_m, more current is passed through the NMOS in the source follower. Figure 5.5 shows the the actual signal, signal delayed by one stage and the signal delayed by two stages. Reducing C_m is same as reducing C_e. But that will reduce delay. In fact, if we want to give high delay in each stage, then we have to use high C_e. That will cause problem in cascading by increasing C_m.

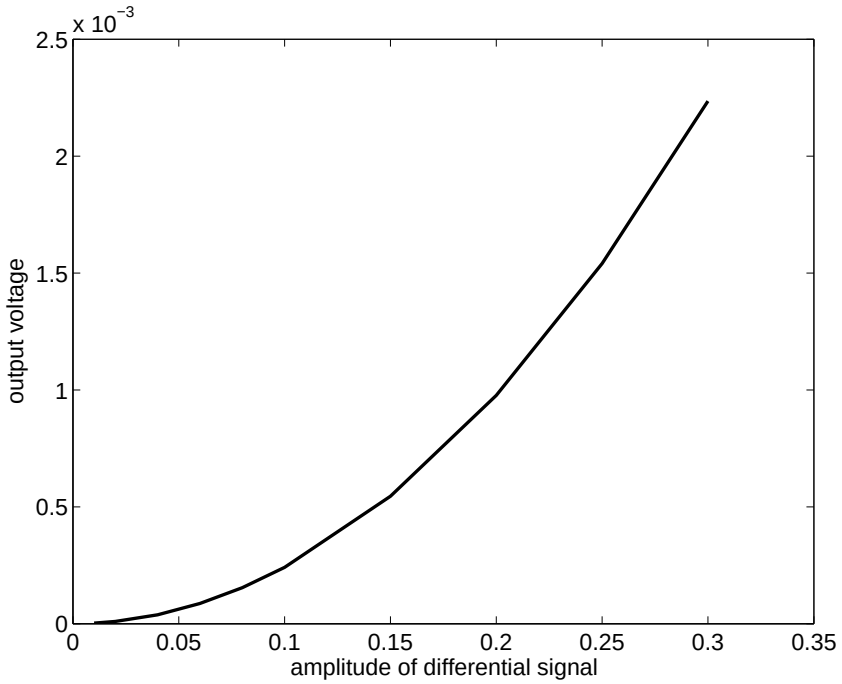

Figure 5.3: The output of the subtractor when input is totally differential

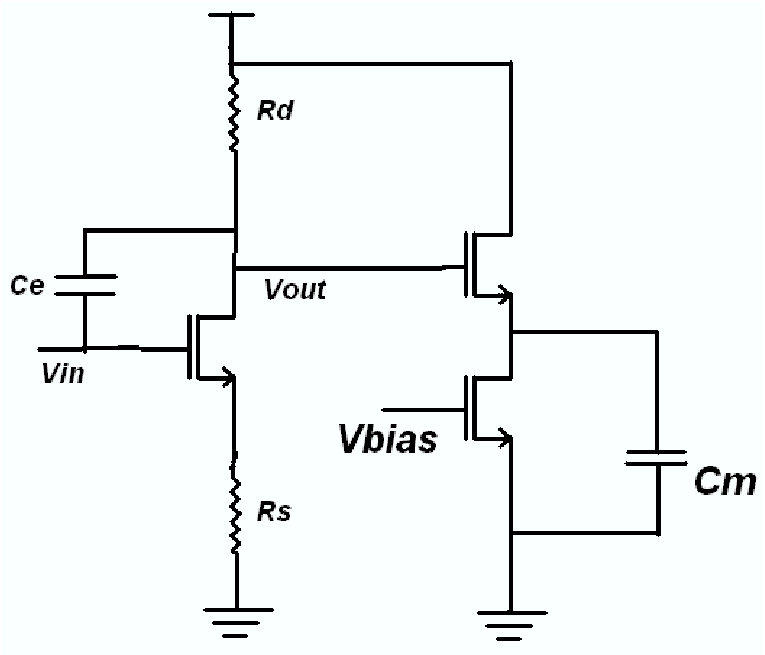

Figure 5.4: Cascaded delays (C_m is the load due to the next stage)

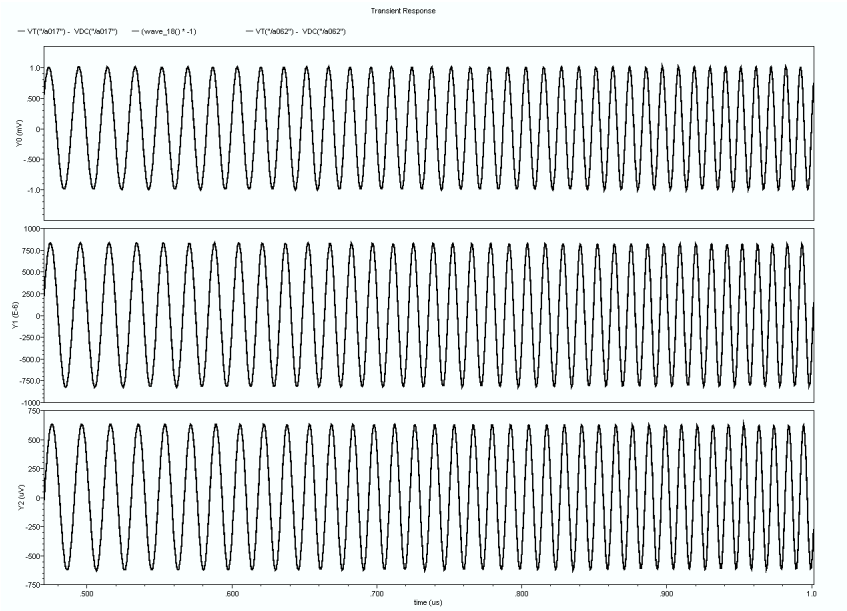

Figure 5.5: The actual signal, delayed signal by one stage delay, delayed single by two stages

Hence in each stage, the capacitance is to be reduced and by increasing number of stages we can produce the required delay.

5.4 Result

For characterization of the system chirp signal is used. The chirp signal is passed through a low-pass filter (with cut-off frequency of $100MHz$). This signal is also passed through a delay block to delay the original signal. The filtered signal and the delayed signal are subtracted to get the second band. The two bands are added in analog domain to show that in analog domain just by adding two bands we can get back the initial signal. The little distortion in the reconstructed signal is due to the non-ideality of the circuits. Figure 5.6 shows the two bands obtained by this type of filter-bank. The actual signal and the reconstructed signal are shown in the figure 5.7. The spectrum of two bands are shown in the figures 5.8 and 5.9. The

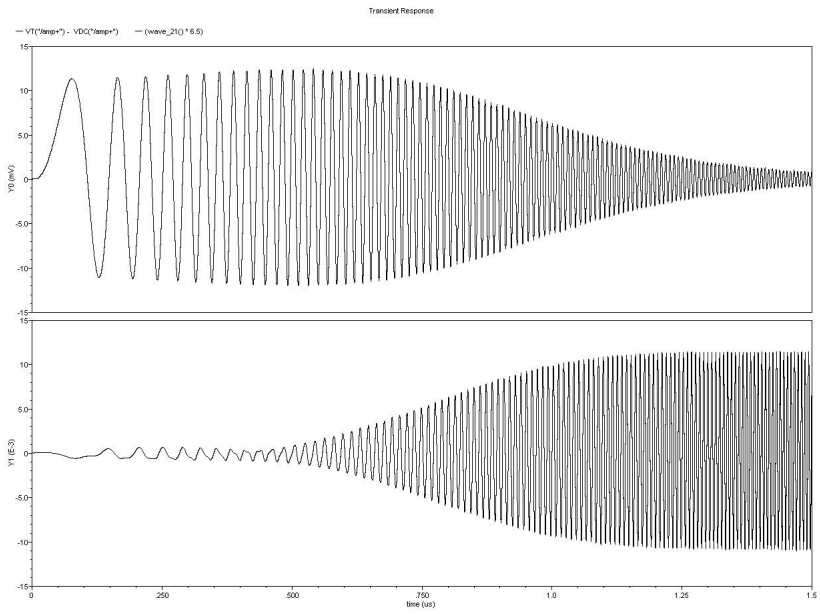

Figure 5.6: The two bands obtained using the filter-bank (consisting of low-pass filters and delays)

spectrum of the reconstructed signal is shown in figure 5.10.

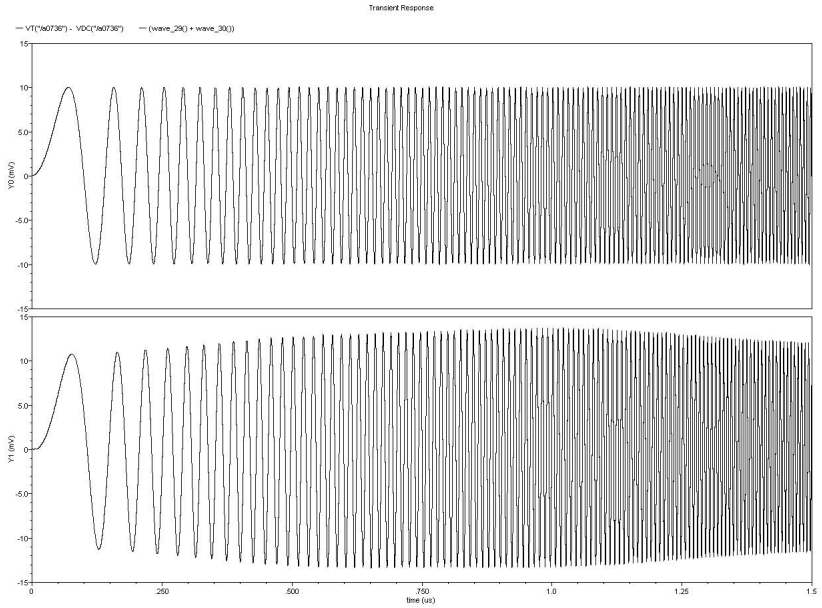

Figure 5.7: The signal and the reconstructed signal (in analog domain) using the filter-bank (consisting of low-pass filters and delays)

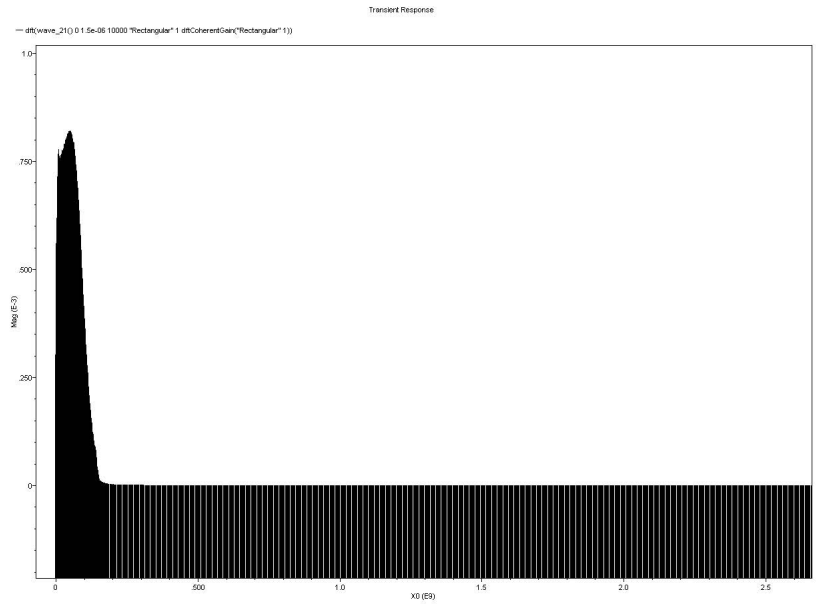

Figure 5.8: Spectrum of the first band (obtained by low-pass filtering)

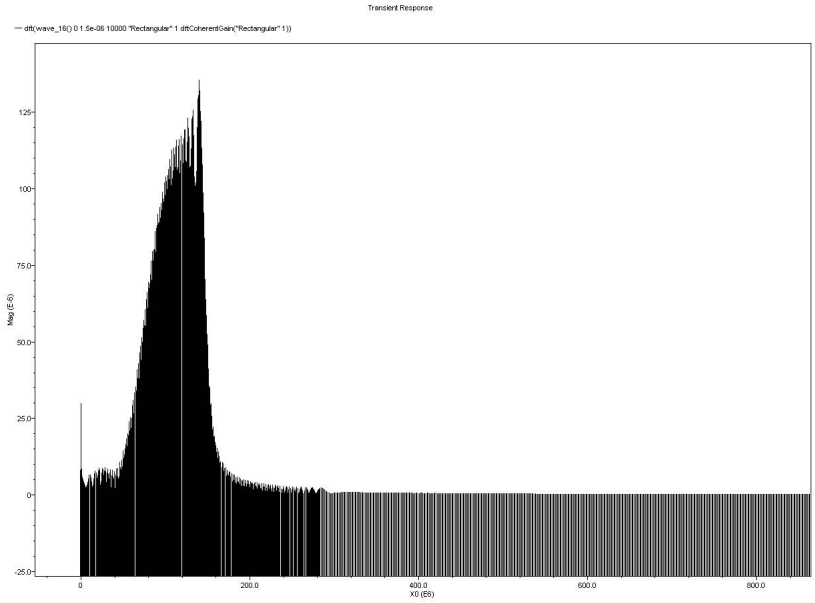

Figure 5.9: Spectrum of the second band (obtained by subtracting the low-pass signal from the original signal)

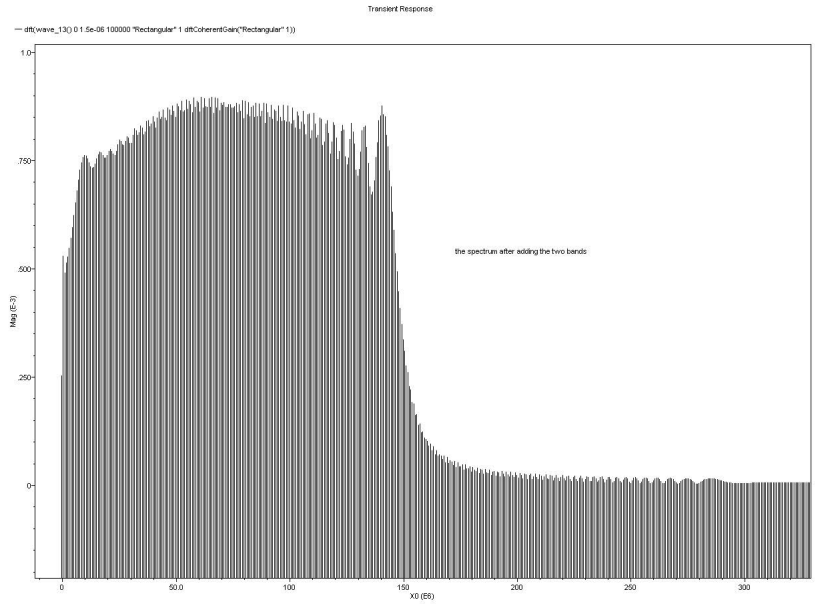

Figure 5.10: Spectrum of the reconstructed signal (just adding the two signals in analog domain)

Chapter 6

ADC Block

6.1 Introduction

After breaking the signal in several bands, in each band I have to digitize the signal. For this ADCs are to be designed. For designing a good ADC one has to design good sample-hold circuit and good comparators. In this chapter, mainly the design of comparator and sample-hold circuit is described. Using those a $3-bit$ flash ADC is designed.

6.2 Sample-Hold

As discussed already, the design of a good sample-hold circuit is the main bottleneck of designing a good ADC. The circuit designed in CADENCE for sample-hold is shown in figure 6.1.

For sample-hold we need a good switch and a capacitor. For switch, transmission gates (consisting of $M1$ and $M2$) are used as it provides almost same resistance for all the input voltage $(0 - V_{dd})$. The main challenge while designing sample-hold circuit is to operate at very high speed (which calls for a larger W/L or a smaller sampling capacitor) with satisfactory precision. There are mainly three mechanisms in MOS transistor operation, which introduces error at the instant when the switch turns off, viz., Channel Charge Injection, Clock Feedthrough and KT/C noise. Detailed analysis of these errors and the way to correct them can be found in [1]. In this circuit the capacitor used is $400fF$. $M3$ and $M4$ are used to reduce the channel charge injection. This charge cancelation technique works for a specific dc voltage

(which depends on the sizing of the transistors) of the signal. In my case it turns out to be $783mV$. This sample-hold circuit is not linear w.r.t. the input amplitude.

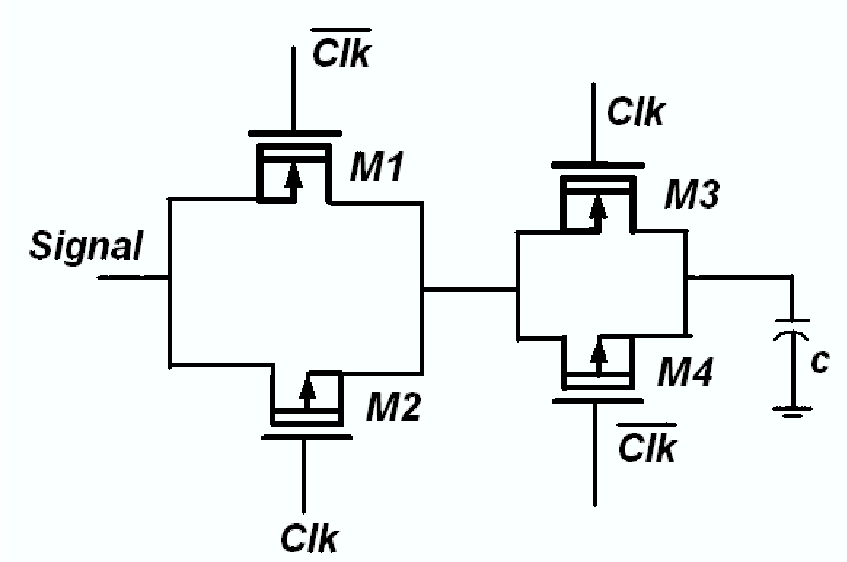

Figure 6.1: The Circuit Diagram for Sample and Hold

That causes some problem in ADC operation. A new method is suggested by Dr. Shanti Pavan [20] to solve that problem.

6.3 Comparator

For good ADC we need a good comparator. While designing comparator, clocked comparator strategy is not used as it causes more jitter noise. Two types of comparators are designed. The circuit diagram for both are shown in the figures 6.3 and 6.4. The first comparator (open-loop) does not have any positive feedback and hence its working speed is not much. The range of reference voltage for which the circuit is working is form $1.05V$ to $1.7V$. Figure 6.5 shows the output of the comparator when the reference voltage is $1.05V$ and figure 6.6 output of the comparator when the reference voltage is $1.7V$. The second one (regenerative and has positive feedback) is faster. The range of reference voltages for which the circuit operates is from $1.05V$ to $1.45V$. Figure 6.7 shows the output of the comparator when the ref-

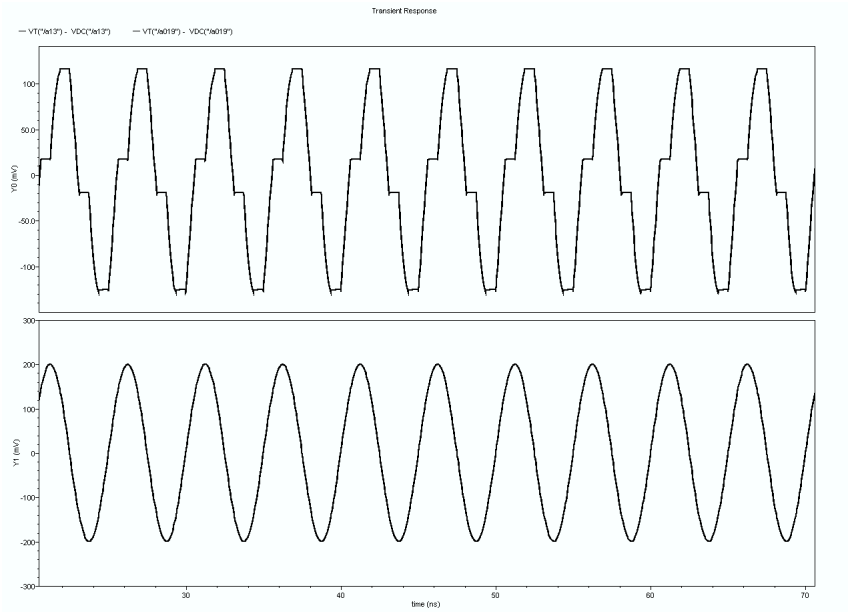

Figure 6.2: The output of the Sample and Hold Circuit when the clock frequency is $800MHz$ and the input signal is at 200MHz

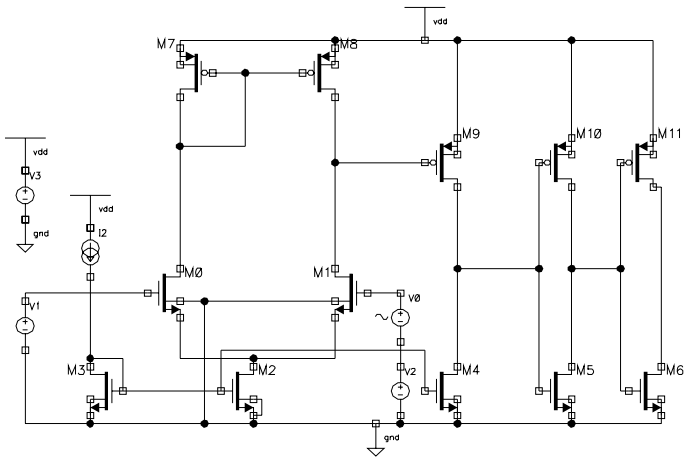

Figure 6.3: The Circuit Diagram for Comparator(open-loop)

erence voltage is $1.05V$ and figure 6.8 output of the comparator when the reference voltage is $1.45V$.

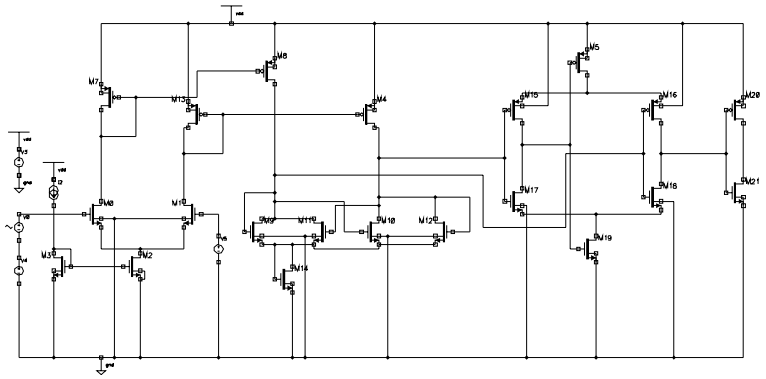

Figure 6.4: The Circuit Diagram for Comparator(Regenerative)

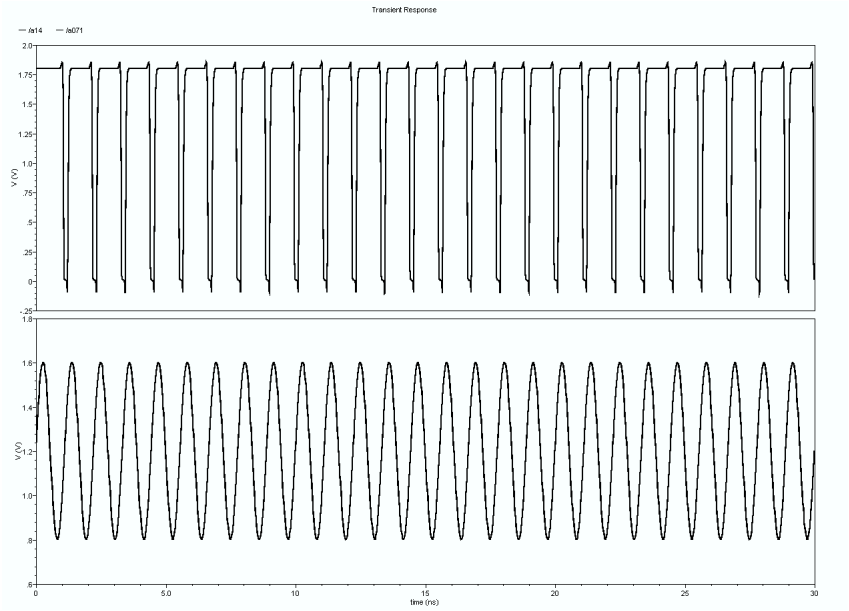

Figure 6.5: The output of the open-loop comparator when reference voltage is low

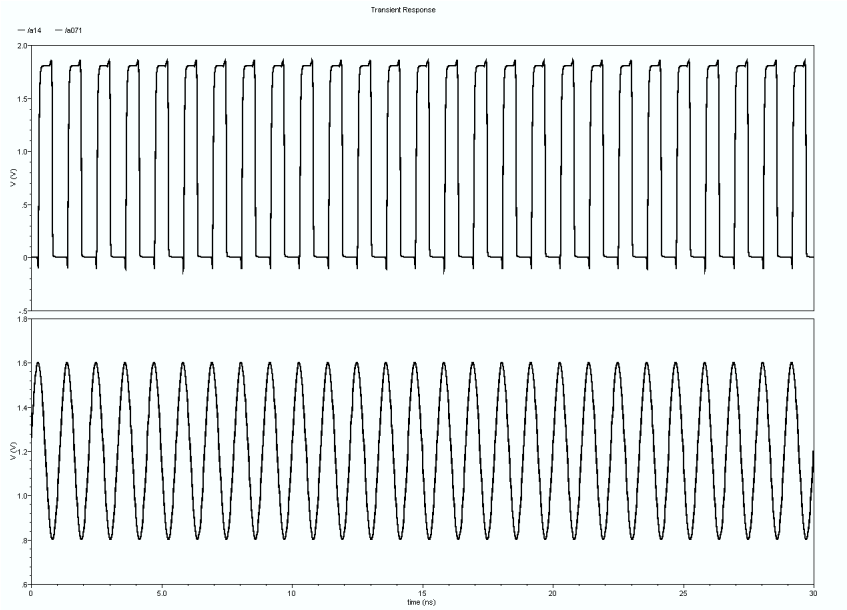

Figure 6.6: The output of the open-loop comparator when reference voltage is high

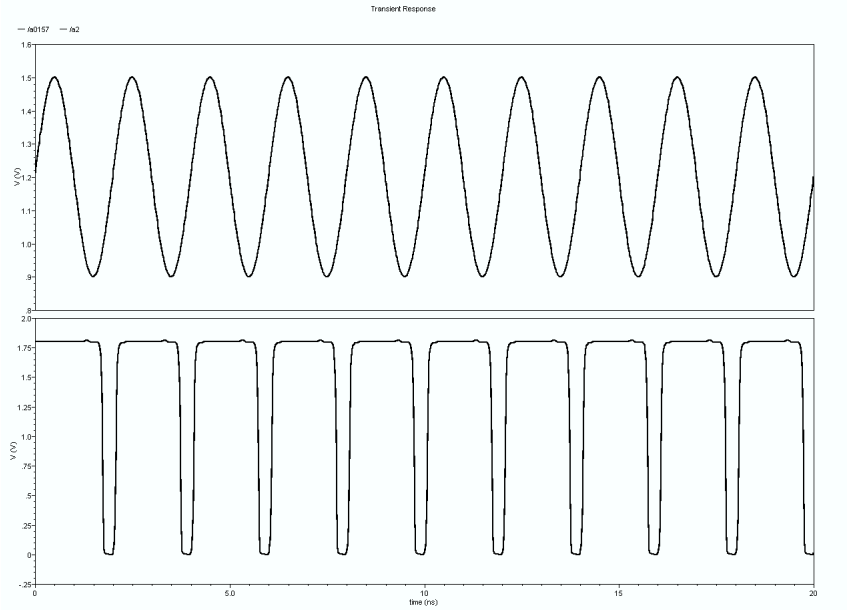

Figure 6.7: The output of the regenerative comparator when reference voltage is low

6.4 Flash ADC

The designed Flash ADC is a 3-bit ADC. The already designed sample-hold and the comparator are used to design the flash ADC. Figure 6.9 shows the basic architecture of a flash ADC. For 3-bit we need 8 comparators. The threshold of different comparators are different and generated by a resistor-array. As the same sample-

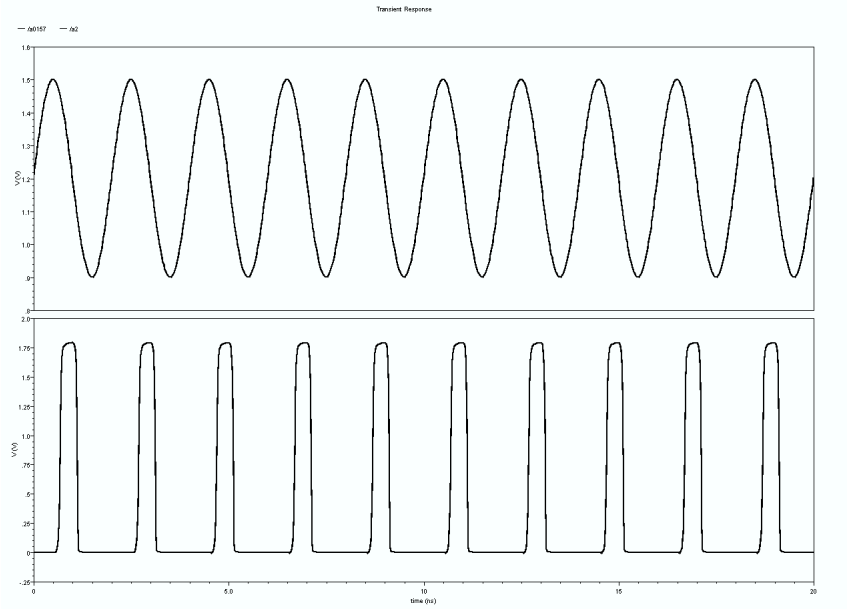

Figure 6.8: The output of the regenerative comparator when reference voltage is high

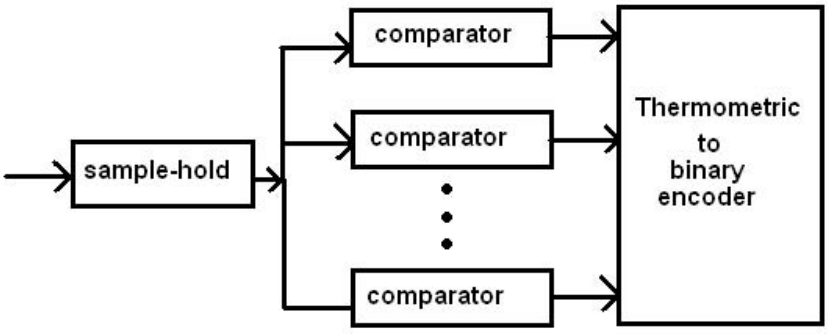

Figure 6.9: Block Diagram of Flash ADC

hold signal is going to many comparators hence the comparators should have less input capacitance to reduce the loading effect. Otherwise the input signal is loaded and the signal is distorted. Figure 6.10 shows the output of the flash ADC. The dynamic range of the Flash-ADC is around $256mV$.

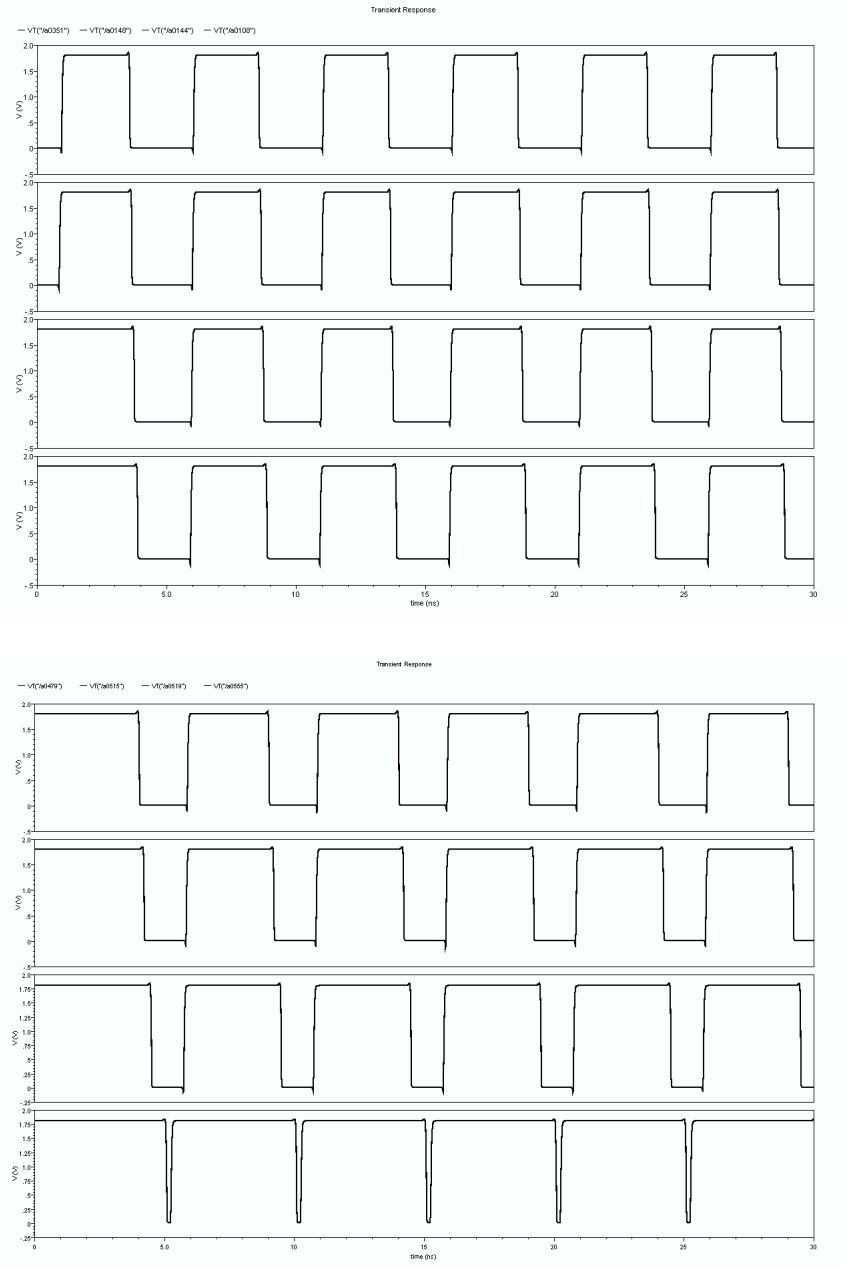

Figure 6.10: The output of the 3-bit flash ADC (from top to bottom is MSB to LSB)

Chapter 7

Reconstruction

7.1 Introduction

After analog-to-digital conversion the signals from different bands are to be combined to get the whole reconstructed signal. Just addition of signals from different bands will not give the reconstructed signal. The error due to aliasing and overlapping filter are to be minimized by some numerical methods (i.e., in circuit by some digital filtering) as done for perfect reconstruction filter [22]. In my thesis, I am mainly concerned about the analog front-end which will break the signal in bands. Reconstruction of the signals from different bands is studied in algorithmic level only. The circuit implementations are not done for this portion. MATLAB 7.0 is used to simulate the system and to check the performance of the heuristic used to reconstruct the signal from different bands.

7.2 Methodology of Reconstruction

If perfect brick-walled filters were used for breaking the signal then there is no overlap of bands. But the filters are not brick-walled. Again sampling creates signal in different bands. To remove the out-band contents of the signal due to sampling, we have to pass the signals through digital filters having the filter-characteristics same as that of the analog filter used for that band. After that just addition of the signals at different bands will approximately reconstruct the signal. The overlapping between bands is also removed due to digital filtering.

Here, In the first filter-bank architecture, the signals are overlapping and the

pass-bands are not fully flat. In second filter-bank they are not overlapped much, but then also the undesired signal appearing due to sampling are to be removed. And the pass-bands are more flat compared to the previous architecture but that also is not fully flat-band. So basically the problems which are to be solved are:

- The non-ideality due to overlapping filters is to be removed.
- The undesired signal obtained due to aliasing is to be removed.
- The non-flatness of the pass-band of the filter is to be removed.

7.2.1 The Main Concept

The main idea behind reconstruction is to use a filter whose transfer function is inverse of the transfer function of the analog filter in the pass band and zero otherwise. This filter is made as brick-wall as possible by using higher order. The first criteria ensures that the filtered signal which is not flat-band becomes flat-band; and the second criteria ensures that signal of undesired frequency is minimized. To estimate the inverse of the filter *invfreqz* function in MATLAB is used. Simulation is performed over three bands and the result is shown in next section.

7.3 Simulation and Result

A chirp signal (with frequency from $200MHz$ to $800MHz$) is passed through the filters. The spectrum of the original signal is shown in figure 7.1. Figure 7.2 shows the frequency response (magnitude only) of the analog filters. The three filters used are band-pass filters. Now if the three bands are just added we do not get back the actual signal as there are significant overlap as well as different filters produce different delay. Figure 7.3 show the spectrum of the signal when the three bands are just added. Obviously this is much different from the original spectra. So we have to design digital filters which will help to reconstruct the signal properly. Figure 7.4 shows the desired frequency response (magnitude only) of the FIR filters for each band. Figure 7.5 show the inverse response of the digital filters, approximated in MATLAB by *invfreqz* function. Figure 7.6 shows the spectrum after applying the digital filter and then adding the signal.

To quantify the performance enhancement, I define a quantitative measure mean square error (MSE). The spectrum of the actual signal is found out. The

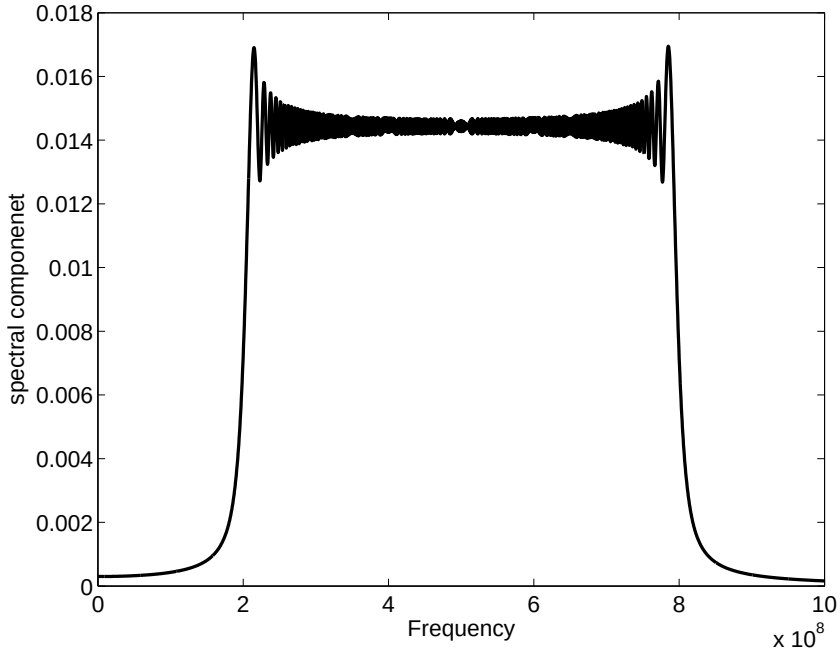

Figure 7.1: Spectrum of the Input Chirp Signal

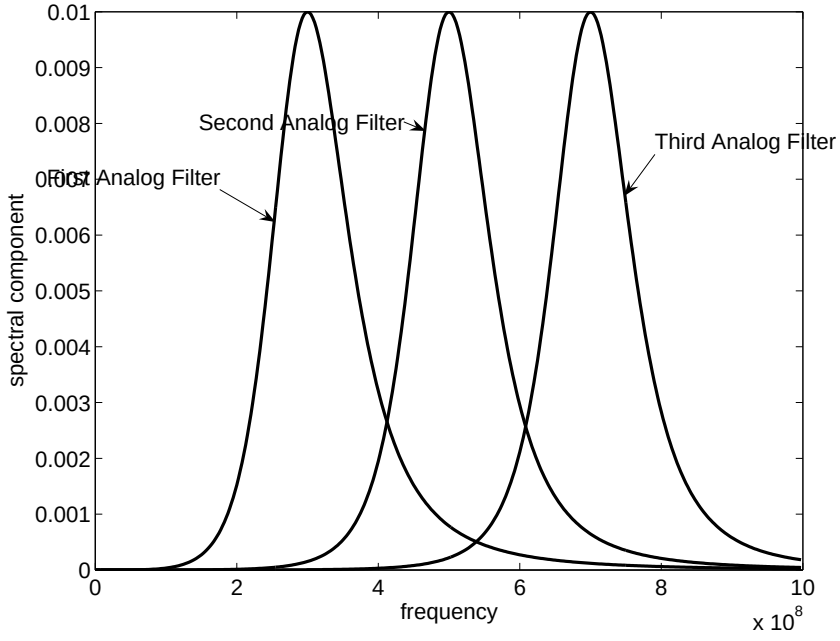

Figure 7.2: Magnitude Response of three analog filters

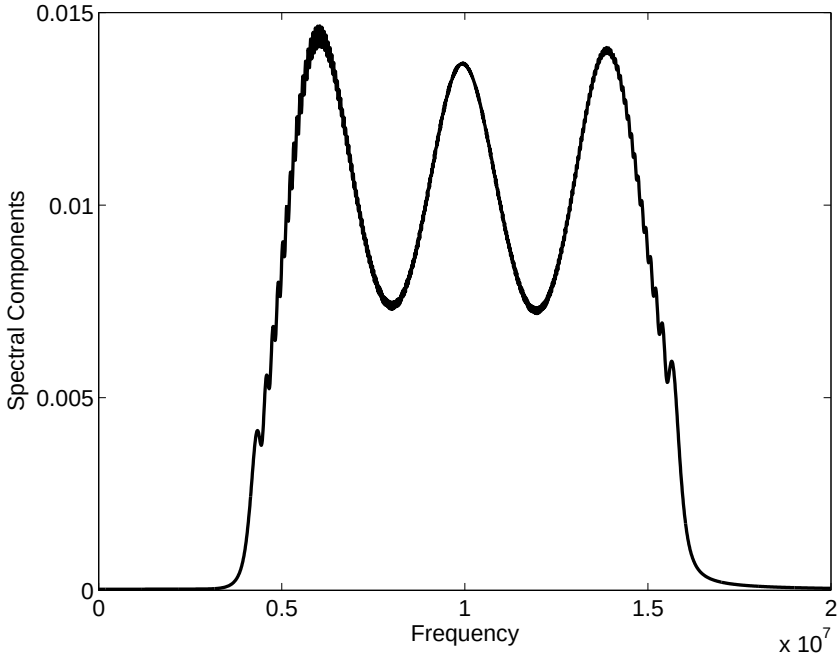

Figure 7.3: The Spectrum of the signal when the three bands are just added

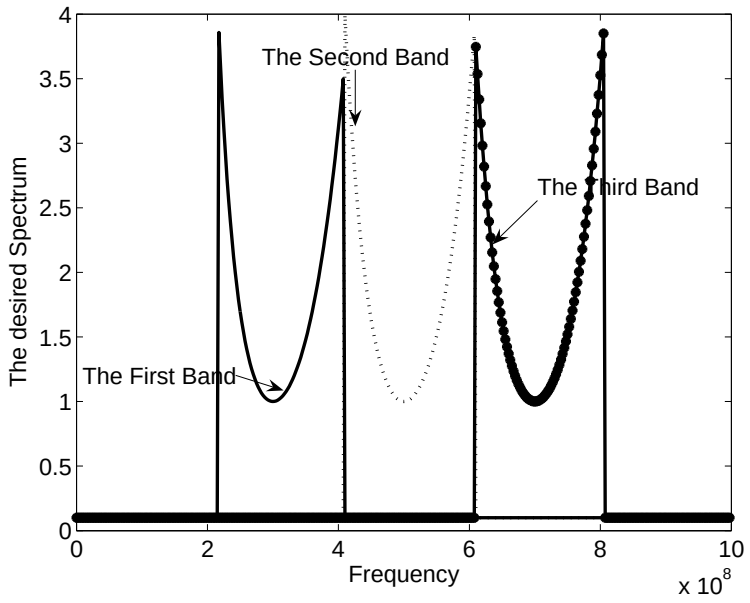

Figure 7.4: The Desired Response of the FIR filters for all three bands

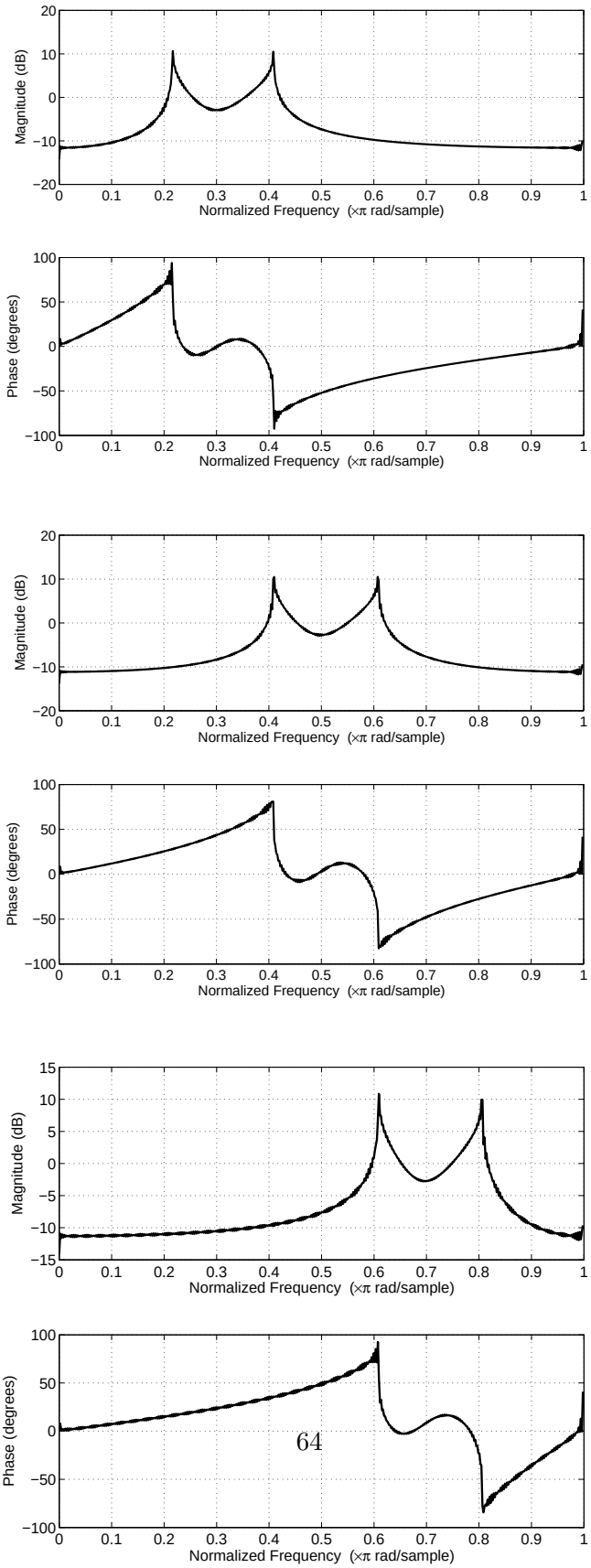

Figure 7.5: The response of three digital filters as designed in MATLAB

Table 7.1: MSE of the signal after applying the reconstruction technique and the performance enhancement with filter order (Just adding MSE is 1.7694×10^{-5})

Filter Order	MSE after Reconstruction	Performance Enhancement
150	7.9731×10^{-6}	$6.9240dB$
250	7.4584×10^{-6}	$7.5036dB$
350	7.7800×10^{-6}	$7.1369dB$
550	7.9325×10^{-6}	$6.9683dB$

spectrum of two signals (one just adding the different bands and the other adding bands after applying reconstruction technique) are also found out. The MSE finds the distortion by subtracting two spectrum and taking the square of the error. The FIR filter orders are changed and table 7.1 shows the MSE and the performance enhancement due to reconstruction heuristic.

Here we can observe that withe filter order the performance is not increasing much. Even then the filter orders are very high from practical implementation point of view. But exploiting the concept of trans-multiplexer the complexity of digital filters can be reduced [23].

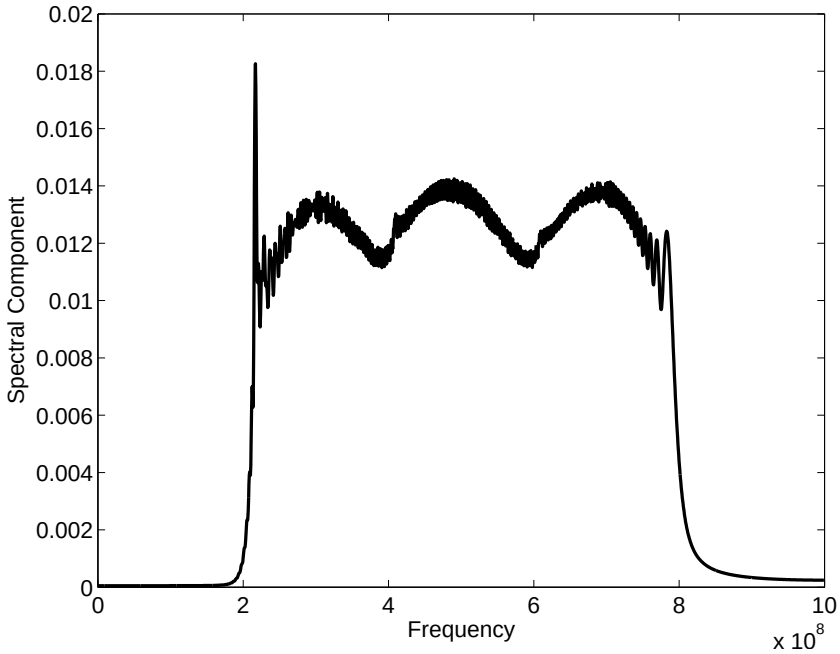

Figure 7.6: The Spectrum of the signal after applying the digital filtering technique

Chapter 8

Other Supplementary Works

8.1 Introduction

In course of studying and designing the sub-band ADC, some other things are also designed. They are not exactly relevant to the main discussion of the thesis. Hence they are put in a different chapter.

8.2 Sub-sampling

I first planned to down-convert the signal to base-band so that the required sampling frequency is less. To down-convert the signal, idea of sub-sampling (bandpass sampling) is used. The incoming signal (which is bandpass) is sampled at a frequency less than its nyquist frequency but at a frequency more than twice the band-width of the signal. It can be proved that if f_c is the carrier frequency and f_s is the sampling frequency then the f_{IF} where the signal will be down-converted is given by the following relations. If $\lfloor \frac{f_c}{f_s/2} \rfloor$ is even then

$$f_{IF} = rem(f_c, f_s) \tag{8.1}$$

and if $\lfloor \frac{f_c}{f_s/2} \rfloor$ is odd then

$$f_{IF} = f_s - rem(f_c, f_s) \tag{8.2}$$

The result of sub-sampling is shown in figure 8.2. This is simulated in MATLAB Simulink. Figure 8.3 shows the model used to simulate the sub-sampling receiver.

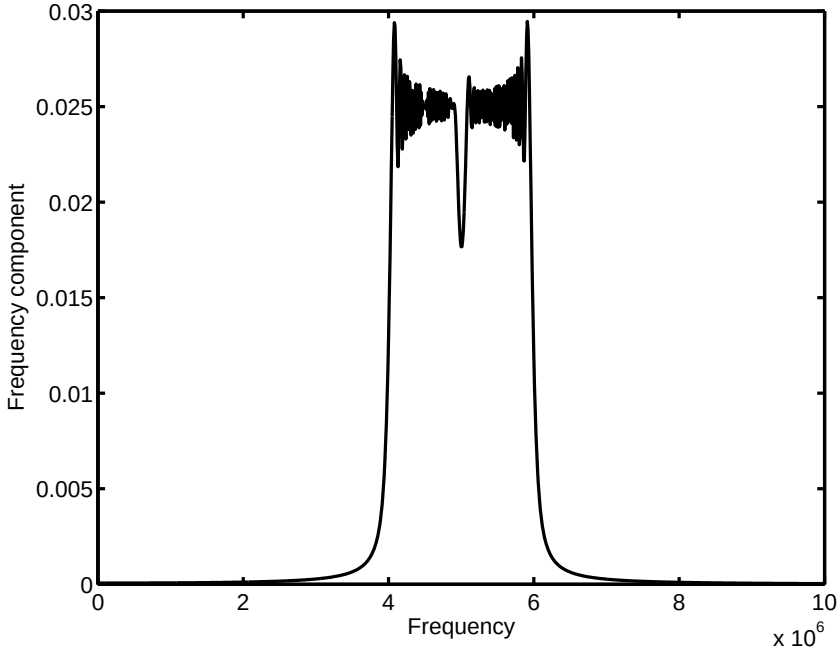

Figure 8.1: Input spectra of the sub-sampling receiver output

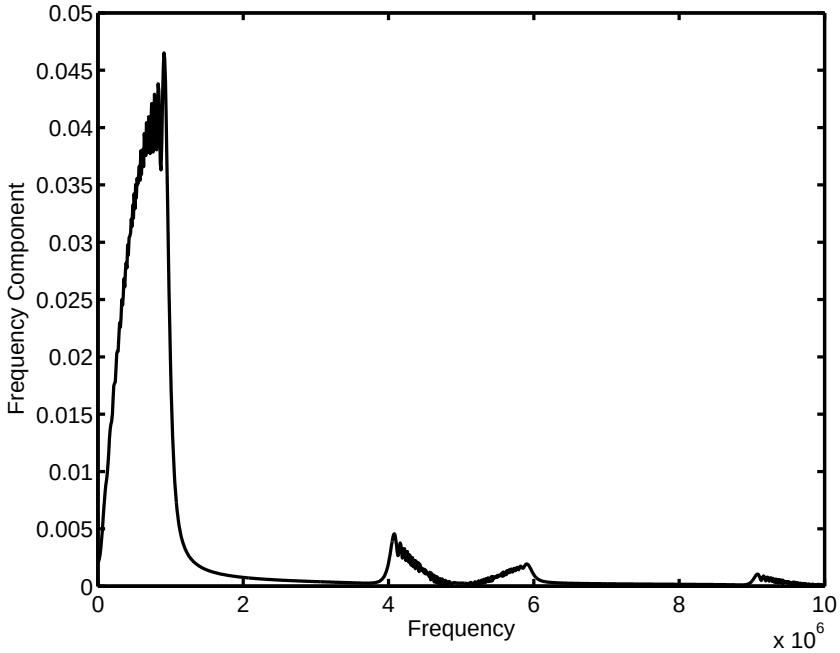

Figure 8.2: Output spectra of the sub-sampling receiver output

8.2.1 Implementation in silicon

This sub-sampling receiver is also designed and simulated in CADENCE. The circuit for sub-sampling receiver as (shown in the figure 8.4) consists of mainly a sample-hold circuit followed by a buffer and a low-pass filter. Figure 8.5 shows the input and output spectra of the signal.

8.3 Low-pass Sigma-Delta Modulator

It is a over-sampling analog to digital converter and it is basically used to increase the resolution and to reduce the quantization noise. Figure 8.6 shows the circuit for sigma-delta modulator and figure 8.7 shows the output of sigma-delta modulator. This is a one bit and single loop implementation.

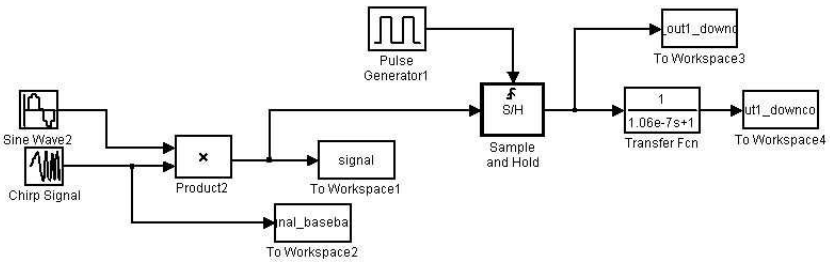

Figure 8.3: Architecture simulated in MATLAB Simulink for sub-sampling receiver

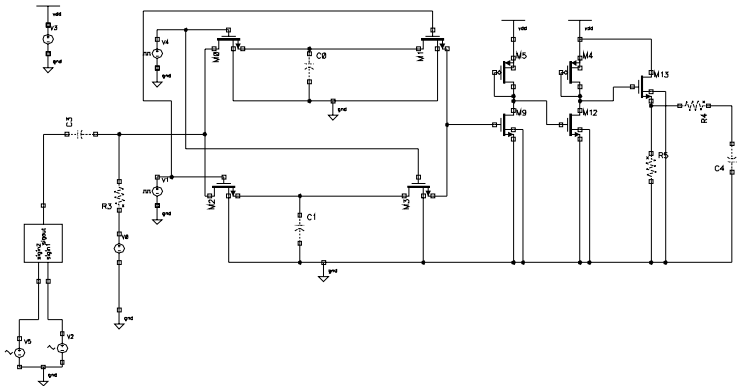

Figure 8.4: The Circuit Diagram for Sub-sampling

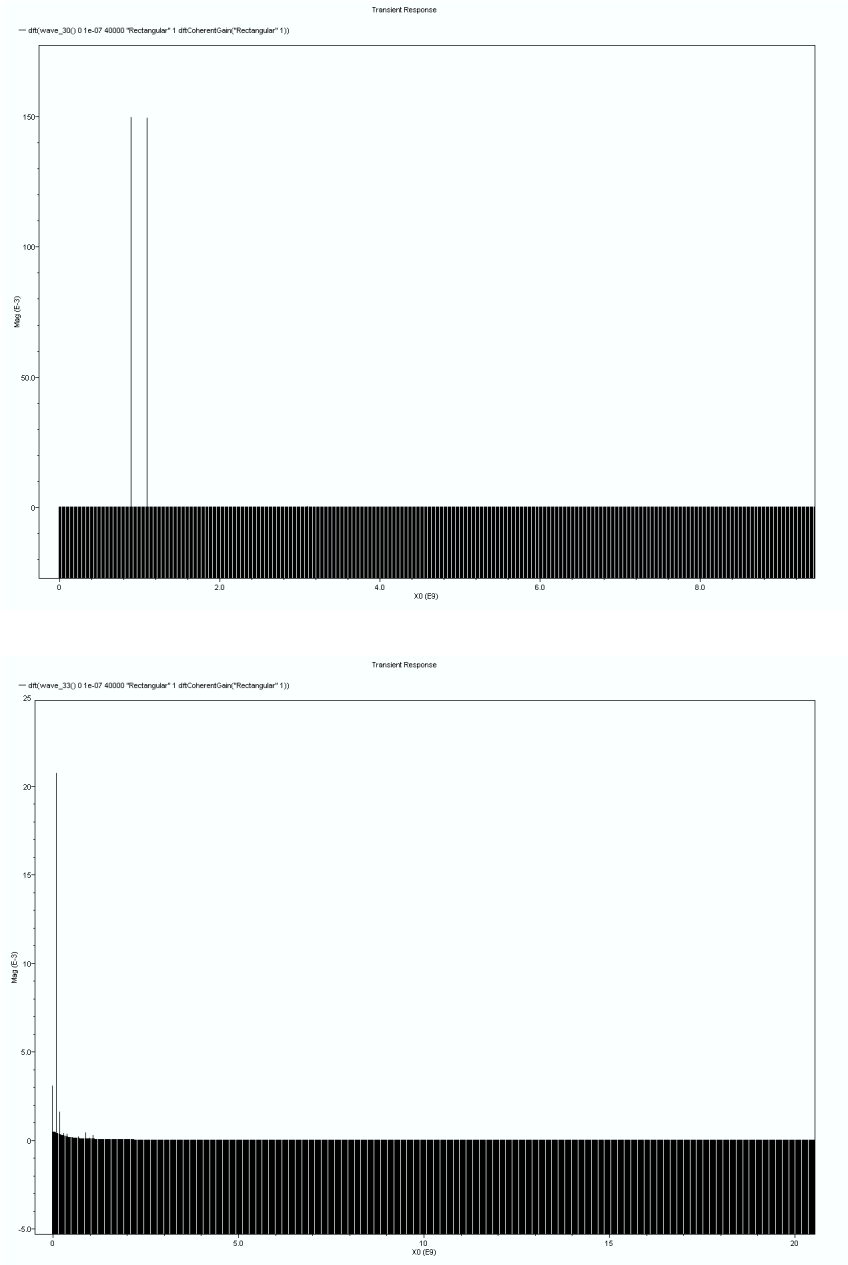

Figure 8.5: The Input and Output Spectra for Sub-sampling as simulated in CADENCE

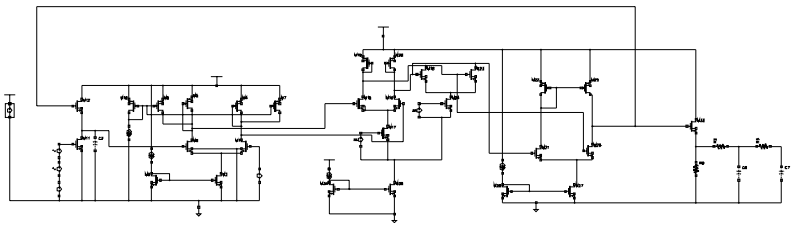

Figure 8.6: Circuit for sigma-delta modulator (low-pass)

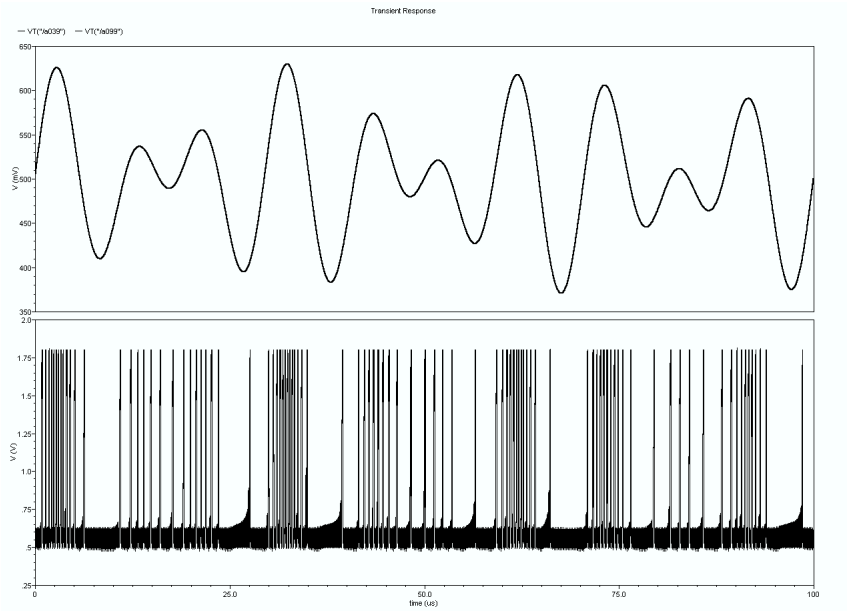

Figure 8.7: Output of Sigma-Delta Modulator

8.4 Band-pass Filters

In previous chapters the design of band-pass filters is described in details. Here two other approaches are described. By cascading one low-pass and one high-pass filter a flat-band band-pass filter can be obtained. Its response is shown in figure 8.8.

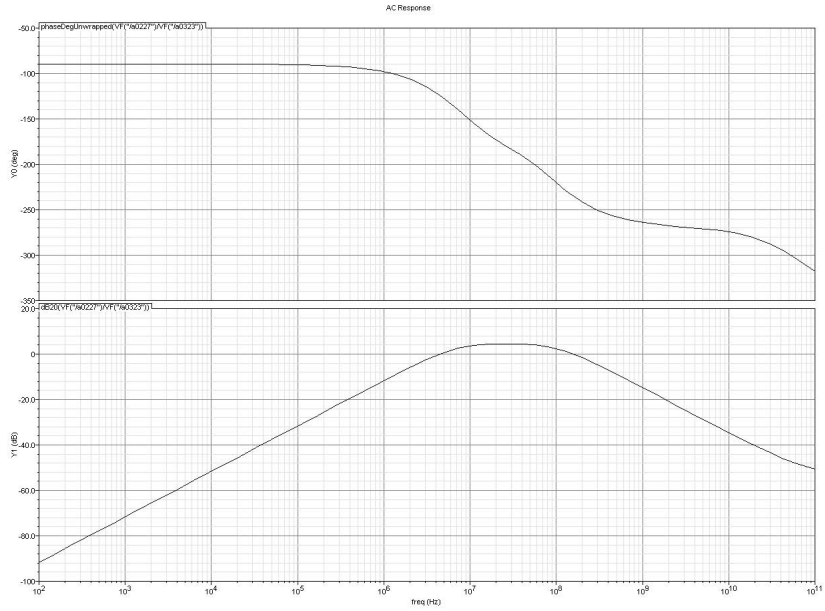

Figure 8.8: Filter Band-pass Response (Flat-band)

Another type of polyphase band-pass filter is implemented by $g_m - C$ topology. Its response is shown in figure 8.9. This type of filter produce quadrature output as shown in figure 8.10.

8.5 Folding Architecture

To produce multi-bit in the flash bit the folding architecture is also studied. Figure 8.12 shows the architecture of the folder and figure 8.11 shows the output of the folder.

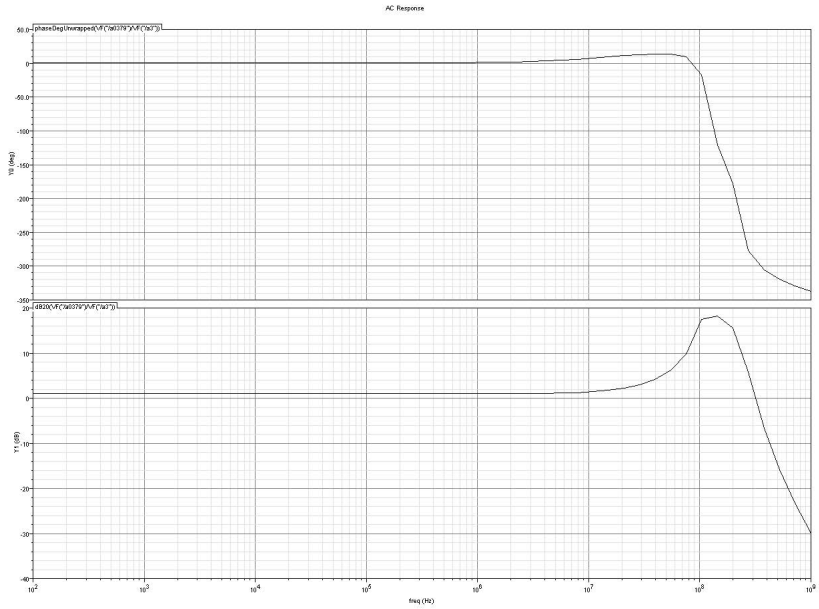

Figure 8.9: Filter Band-pass Response (this can generate quadrature output)

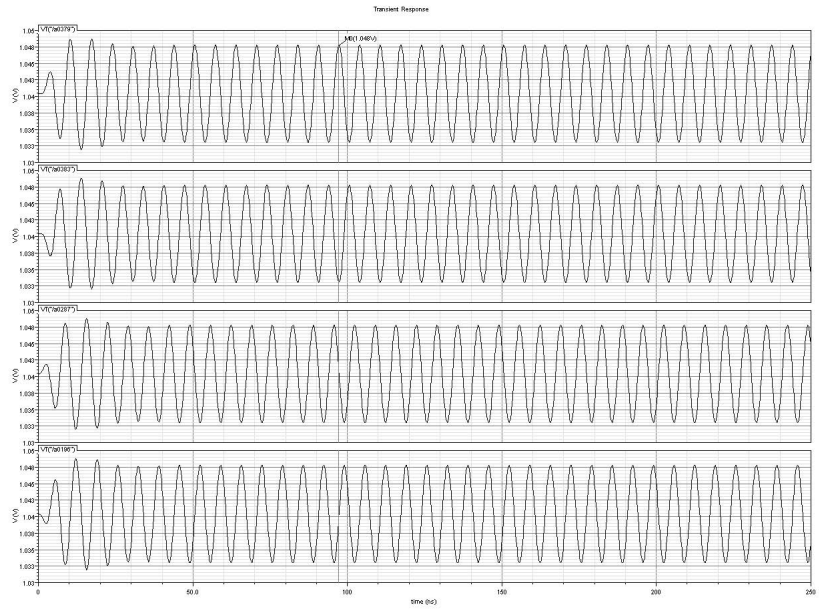

Figure 8.10: Quadrature wave-forms for the band-pass filter

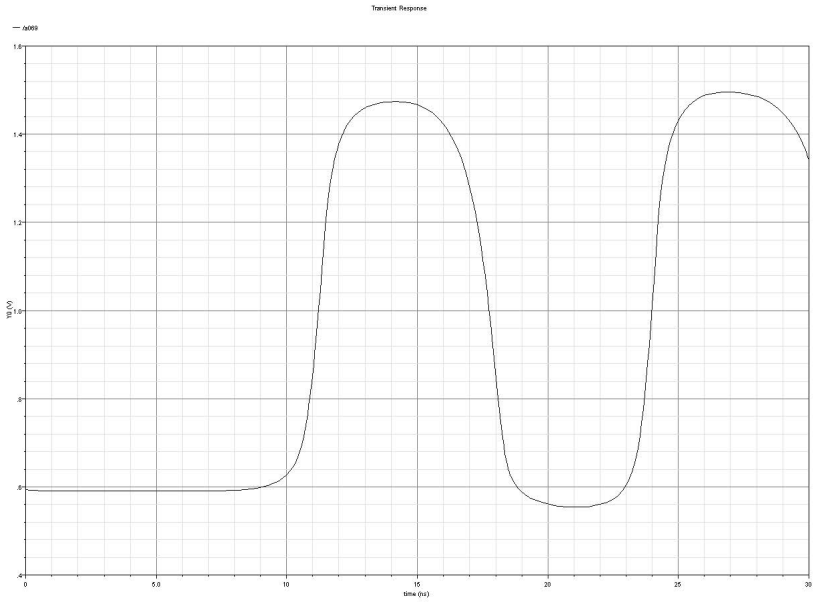

Figure 8.11: The output of folder circuit

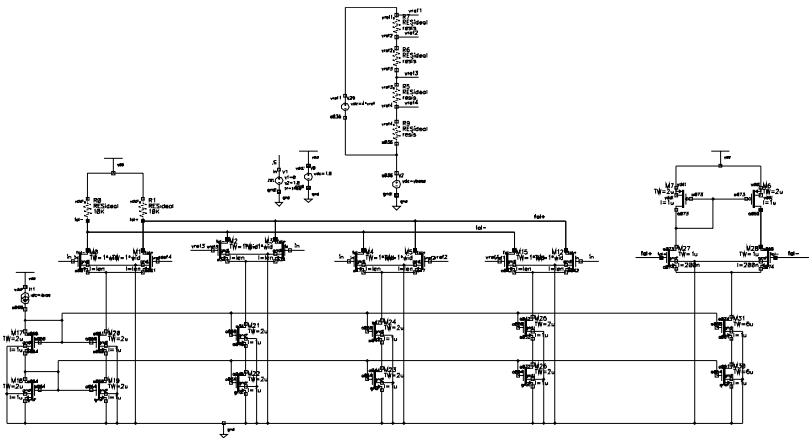

Figure 8.12: The Folding Circuit

Chapter 9

Conclusion and Future Work

9.1 Summary

This thesis mainly talks about the implementation of the filter-bank in a new type of ADC, i.e., sub-band ADC. In some literature the concept of sub-band ADC is proposed, but no literature deals with the practical implementation of this ADC in silicon.

The performance enhancement due to sub-band ADC is reported in chapter 2 of this thesis. Mathematically the reason behind performance enhancement is established and system level simulation affirms the theory. These simulations also point to many design criteria, important for sub-band ADC. The possible practical problems faced during implementation in silicon is elaborated. One of the main parts of the ADC, i.e., the filter bank is designed. Two different architectures have been proposed and both are implemented in silicon and simulated in CADENCE. These along with the outputs are described in chapter 4 and 5. The advantages of the second architecture is established. Also the difficulties in implementing the analog delay are described here. A possible implementation of analog delay in silicon is also described and theoretically the amount of delay is found out. Chapter 7 discusses the digital back-end which is used to recombine the bit-stream. For this a new heuristic is found out. That heuristic give satisfactory performance. This part is simulated and the result is also reported.

9.2 Future Work

But this is not the end of the game. This is just a beginning of the work, I wanted to complete. But due to lack of time I could not finish the whole work. This system has lots of potential and it can be used with little variations for many applications. The future work can be listed below:

1. The delay used here can be made tunable by using NMOS and PMOS in place of resistors or making the capacitances switched. But the performance is not measured by implementing them. That can be done to make the delay tunable.

2. Apart from the filter-bank, some part of ADCs are designed. Those can be integrated to the filter-bank to make the whole ADC. Again the reconstruction algorithm can be mapped to digital circuit and that will complete the whole ADC.

3. The whole system can be fabricated and tested, so that the performance improvement, which is predicted theoretically and by system level simulation, can also be obtained in silicon.

4. Here I have excluded the possibility of down-converting the signal at the higher bands. In fact, if the signal has center frequency and band-width comparable to each other, then down-conversion is difficult. But if the whole band is situated at some higher center frequency then down-conversion is possible. This aspect can be investigated.

5. Without using the conventional ADCs for each band, we can use zero-crossing ADCs. As the band-width in bands are small, from zero-crossings the signal can be reconstructed easily.

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