Proceedings of Modeling and Simulation of Microsystems, MSM99, San Juan, Puerto Rico, USA, April 1999

A Compact Model for an IC Lateral Diffused MOSFET Using the Lumped-Charge Methodology

Y. Subramanian[1*], P.O. Lauritzen[**] and K.R.Green[*]

[*]Texas Instruments, Inc, 8505 Forest Lane, Dallas, TX 75243, USA, y-subramanian@ti.com
[**]University of Washington, Seattle, WA 98195, USA, plauritz@ee.washington.edu
[1]Author was a graduate student at the University of Washington during the course of this work.

ABSTRACT

A compact model for an IC Lateral Diffused MOSFET is developed using the Lumped-Charge Methodology[1]. Model equations and key performance characteristics are documented. They satisfy the requirements of Power MOSFET models[2], unlike the competitive macromodels developed from short-channel, low-power MOSFET models.
Keywords: LDMOS Model, Lumped-Charge, Power, MOSFET

INTRODUCTION

An important measure of the utility of a compact model is its ability to accurately represent *external* device behavior in a simple (computationally inexpensive) and physically based manner. This principle was central to the development of the Lumped-Charge Methodology (or L-C Methodology) for compact device modeling in the early 1990s[1].

The L-C Methodology enables the accurate representation of complete external device behavior using a set of simple, physically based equations that use total charge corresponding to specific regions of a device as a fundamental quantity. A figurative description of the L-C Methodology is given in Fig. 1. The L-C Methodology is generally applicable to compact models of most semiconductor devices.

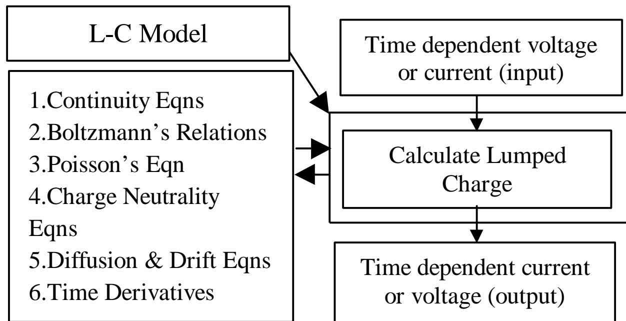


Figure 1: The Lumped-Charge Methodology

The equations and performance of a Lumped-Charge based compact model are here given for an IC Lateral Diffused MOSFET (Fig. 2), excluding bipolar parasitics.

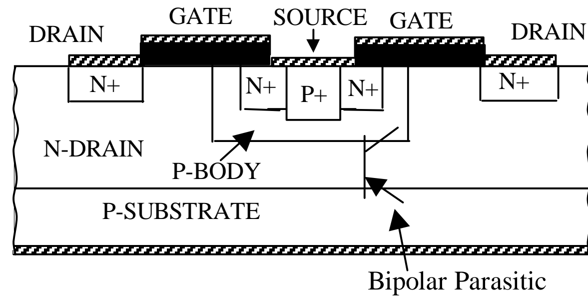


Figure 2: The IC Lateral Diffused MOSFET

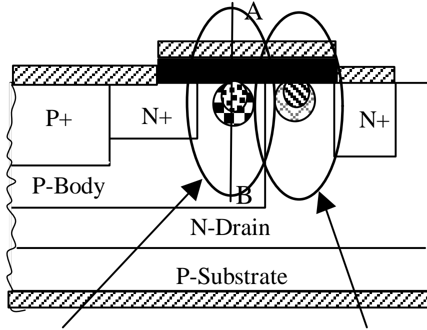
MODEL EQUATIONS

Since simplicity is required of physically based compact models, their equations must balance circuit simulation requirements with the physics of internal device operation. To be physically based, they *must* include *all* internal behavior whose external I-V manifestations are important in circuit design. Conversely, to be simple, they *must not* include internal device behavior whose external I-V manifestations are unimportant in circuit design. In the L-C Methodology, this balance is easily achieved by minimizing the number of discretized charge packets (or *L-C nodes*-see Fig. 3) used to represent a device, subject to the minimum model accuracy desired for circuit simulation. For the L-C LDMOS model, DC as well as AC simulations were obtained with sufficient accuracy by using the Lumped-Charge representation shown in Fig. 3. In this representation, the LDMOS structure is divided into two MOS substructures-*the body substructure* and *the drain substructure* using a minimum number of *nodes* (see Fig. 3).

Figures 1 and 3 form the basis of equation formulation for the L-C LDMOS Model. The equations use a robust set of six parameters directly obtainable from process

This project was a two-year effort supported by the NSF-CDADIC Industry-University Research Consortium. Experimental data for model validation was provided by Texas Instruments, Inc.

information, six physically significant parameters that require optimization for extraction, and four fitting parameters. These parameters are summarized in Table 1.



Body Substructure   Drain Substructure

Lumped Body Inv. Chg, q_{iB} Lumped Body Dep/Acc. Charge, q_{adB}

Lumped Drain Inv. Chg, q_{iD} Lumped Drain Dep/Acc Charge, q_{adD}

Figure 3: L-C Representation of the IC LDMOSFET

Process Dependent Parameters	
W	Width
L_B, L_D	Body, Drain Lengths
T_{OX}	Oxide Thickness
N_B,N_D	Body, Drain Doping Concentrations
Parameters with Physical Significance Requiring Optimization	
μo	Room Temperature Mobility
TEMPEXP	Coeff for Mobility-Temperature reln.
VFB_B	Body Flatband Voltage
LAMBDA	Channel Length Modulation Param.
THETA	Mobility Reduction Factor
VMAX	Velocity Saturation Voltage
Fitting Parameters	
p1	Determines horizontal position of vertical axis (line AB-see Fig. 3) where Poisson's Eqn is solved for each VDS,VGS (see eqs (2) and (3)).
p2, p3, p4	Together determine the influence of Drain Resistance on DC performance

Table 1: Parameters of the L-C LDMOS Model

The Body Substructure

In the body substructure, the lumped body inversion charge, q_{iB} (see Fig. 3) is assumed to represent the average conductance of the channel (for DC behavior) as well as total inversion charge in the body (for capacitive behavior). The total depletion/accumulation charge in the body is represented by q_{adB}..

q_{iB} is calculated by assuming that it can be represented consistent with the above definition by directly relating it to total channel conductance per unit channel length (or, equivalently, total one-dimensional inversion charge per unit channel length) along a vertical line AB (Fig. 3). The horizontal position of AB is represented electrically by assuming that it bears a fixed relationship with terminal voltage. For the purpose of obtaining close fits between model characteristics and device data, flexibility is introduced into this relationship through the use of fitting parameter *p1* (see Table 1). q_{adB} is calculated by assuming that it can be represented by the total one-dimensional depletion/accumulation charge per unit channel length along AB (Fig. 3). The mathematical equations to calculate q_{iB} and q_{adB} are derived from the solution of Poisson's Equation along line AB (assuming the boundary condition that total gate-bulk voltage drop along AB is the instantaneous gate-source voltage, VGS). More information on this derivation is available in [3]. Eqs (1)-(5) must be solved iteratively to calculate q_{iB} and q_{adB}.

$$q_{adB} = -\sqrt{2q\varepsilon N_B} W L_B \times \left[\exp(\frac{\psi_{sB}}{\phi_t}) - \frac{\psi_{sB}}{\phi_t} - 1 \right] \quad (1)$$

where: ψ_{sB} = interface-to-bulk potential along AB
ϕ_{FB} = body fermi potential ;ϕ_t = thermal voltage;
q = electronic charge; ε= permittivity of silicon;

Let *vc* = voltage drop across the channel. Then,

$$q_{iB} = -\sqrt{2q\varepsilon N_B} W L_B \times \sqrt{A + B} - q_{adB} \quad (2)$$

where

$$A = \exp(\frac{\psi_{sB}}{\phi_t}) - \frac{\psi_{sB}}{\phi_t} - 1 \quad (2a)$$

$$B = \exp(\frac{-2\phi_{FB}}{\phi_t}) \times \left[(\exp(\frac{\psi_{sB} - p1 \times vc}{\phi_t}) - \frac{\psi_{sB}}{\phi_t} - \exp(\frac{-p1 \times vc}{\phi_t}) \right] \quad (2b)$$

vc, the voltage drop across the channel is calculated from terminal voltage by using the following empirical expression:

$$vc = \left(\left(\frac{p4}{VDS} \right)^{\frac{1}{p3}} + \left(\frac{p2}{\ln(1+\exp(VGS - VTB))} \right)^{\frac{1}{p3}} \right)^{-p3} \quad (3)$$

where VTB, the nominal threshold voltage is calculated as:

$$VTB = 2\phi_{FB} + \frac{\sqrt{4q\varepsilon N_A}T_{ox}}{\varepsilon_{ox}WL_B} \quad (4)$$

An empirical approach was chosen because any approach based on first principles would be too complicated to derive and evaluate for a diffused body.

$$\psi_{sB} = VGS - VFB_B + \frac{(q_{iB} + q_{adB})T_{ox}}{\varepsilon_{ox}WL_B} \quad (5)$$

where: ε_{ox}= permittivity of oxide

The Drain Substructure

The drain substructure is modeled in a similar manner as the body substructure, but because significant DC conduction through this substructure occurs only when it is in accumulation or depletion, sufficient overall accuracy is obtained by de-linking lumped drain charge (for AC behavior) and drain resistance (for DC behavior). Drain DC behavior is accounted for by the fitting parameters used in eqs. (1)-(3). This assumption simplifies the drain equations, without losing accuracy. Eqs (6)-(8) are solved iteratively to calculate q_{iD} and q_{adD}.

$$q_{adD} = \sqrt{2q\varepsilon N_D}WL_D \times \left[\exp\left(\frac{\psi_{sD}}{\phi_t}\right) - \frac{\psi_{sD}}{\phi_t} - 1 \right] \quad (6)$$

where: ψ_{sD} = interface-to-drain potential; ϕ_{FD} = drain fermi potential ;

$$q_{iD} = \sqrt{2q\varepsilon N_D}WL_D \times \sqrt{C+D} - q_{adD} \quad (7)$$

where

$$C = \exp\left(\frac{\psi_{sB}}{\phi_t}\right) - \frac{\psi_{sB}}{\phi_t} - 1 \quad (7a)$$

$$D = \exp\left(\frac{-2\phi_{FD}}{\phi_t}\right)\left[\left(\exp\left(\frac{\psi_{sD}}{\phi_t}\right) - \frac{\psi_{sD}}{\phi_t} - 1 \right] \quad (7b)$$

$$\psi_{sD} = VGD - VFB_D + \frac{(q_{iD} + q_{adD})T_{ox}}{\varepsilon_{ox}WL_D} \quad (8)$$

where :

VGD= Gate-Drain Voltage;

VFB_D= Drain Flatband Voltage and is calculated as:

$$VFB_D = VFB_B + \phi_{BD} \quad (8a)$$

where ϕ_{BD} is the approximate body-drain built-in potential calculated using the nominal body and drain doping concentrations, N_B and N_D.

Current Calculation

The conduction and displacement components of currents corresponding to the two substructures are calculated and “allocated” to the terminals of the composite LDMOSFET in the manner shown in Fig. 4. This establishes the connection between the body and drain substructures. Note that the drain inversion charge is supplied through the source-body terminal, and not the drain terminal.

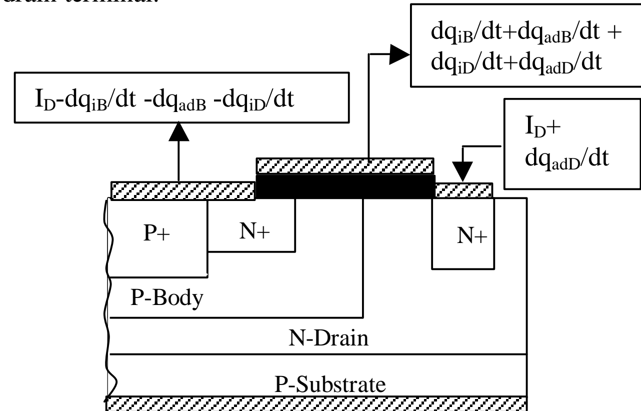


Figure 4: Terminal Allocation of Conduction and Displacement Currents.

In Fig 4:

$$I_D = \frac{vc\frac{q_{iB}}{L_B{}^2}\mu_o\left(\frac{T}{T_o}\right)^{-TEMPEXP}\left(\frac{1}{1+LAMBDA \times VDS}\right)}{1+THETA(VGS - VTB)} \quad (9)$$

PERFORMANCE

Figures 5-10 show the key performance characteristics of the LDMOS model versus device data (provided by Texas Instruments, Inc.). These figures show that LDMOS DC as well as non-DC behavior can be represented with reasonable accuracy using an equation set (eqs (1)-(9)) that

is simple, fully continuous and substantially physically based.

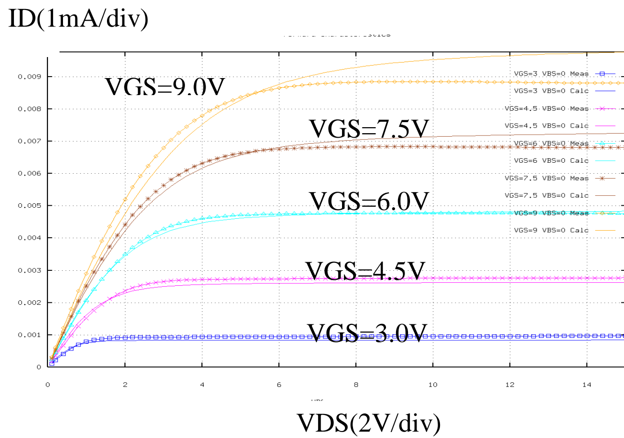


Figure 5: Output DC Characteristics at 300K for model(solid) and data(dotted).

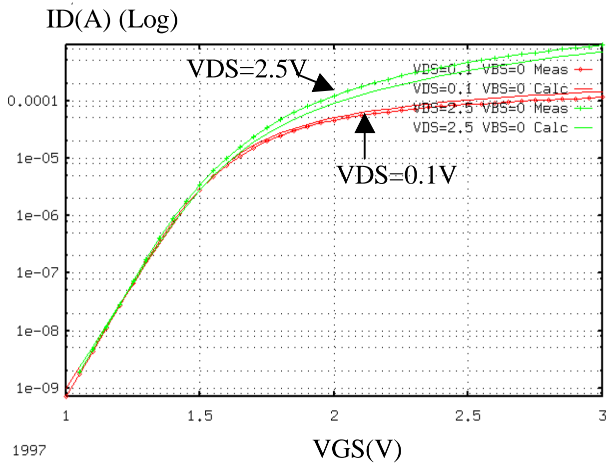


Figure 6: Subthreshold Characteristics at 300K for model(solid) and data(dotted)

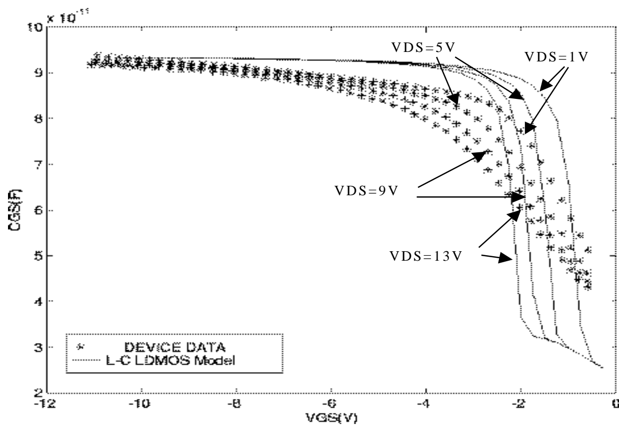


Figure 7: CGS vs VGS for model(solid) & data(stars)

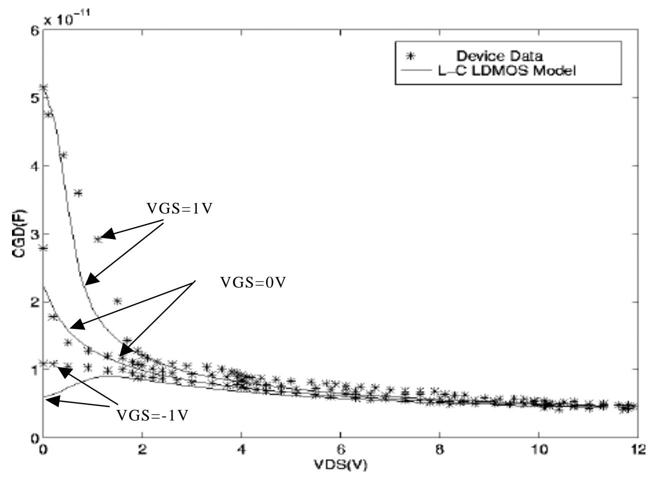


Figure 8: CGD vs VDS for model(solid) & data(stars)

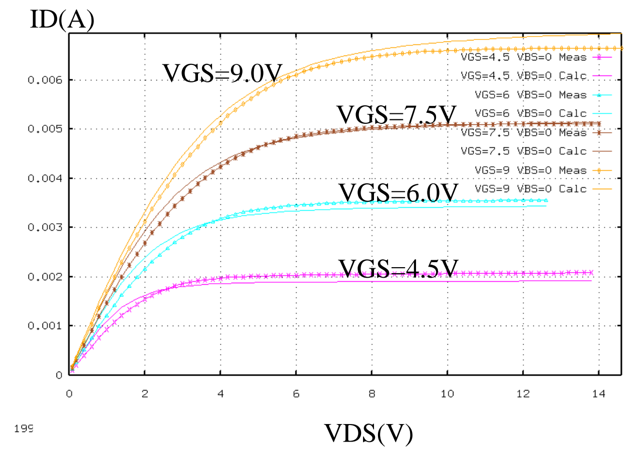


Figure 9: Output DC Characteristics at 423K for model(solid) and data(dotted).

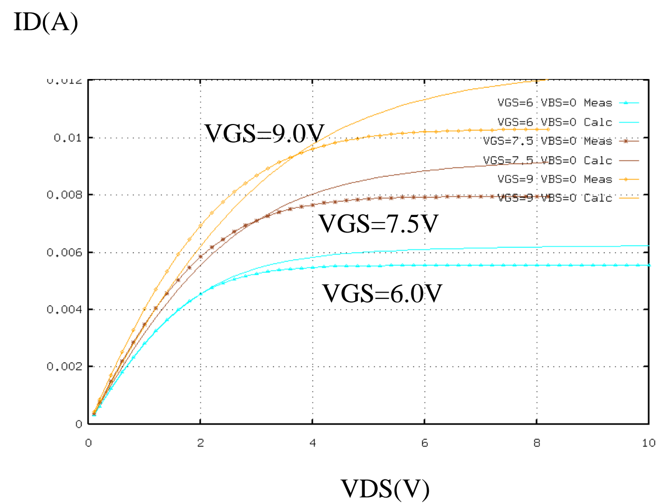


Figure 10: Output DC Characteristics at 233K for model(solid) and data(dotted).

CONCLUSIONS AND FUTURE WORK

The L-C Methodology is able to accurately represent DC as well as non-DC behavior in an IC LDMOSFET using a single set of simple equations with a substantial physical basis. Since the central variable is charge, the L-C LDMOS equations represent composite LDMOSFET behavior in a fundamentally sound fashion, and satisfy the requirements of power MOSFET modeling[2], unlike traditional subcircuit-based approaches involving models of short-channel, low-power MOSFETs. More information on the L-C methodology, including its application to a vertical DMOSFET, as well as a comparison of L-C LDMOS DC performance to the subcircuit-based approach is available in [4]. The simplicity of the L-C approach should ensure its usefulness for compact model development, especially when standard modeling languages (e.g., VHDL-AMS and Verilog-AHDL) become available.

Currently, the L-C LDMOS model is being evaluated with help from circuit design engineers.

A new version of this model has been developed in which the number of fitting parameters is reduced from four to one, but this new model has not yet been validated. Parasitic bipolar models have also been developed for this structure[5].

Future work also includes the addition of self-heating effects.

REFERENCES

[1] Ma, C.L., Lauritzen, P.O., Pao-Yi Lin, Budihardjo, I., Sigg, J, "A Systematic Approach to Modeling of Power Semiconductor Devices based on Charge Control Principles" PESC '94 Record, vol. 1 pp. 31-37, 1994.

[2] Budihardjo, I.K., Lauritzen, P.O., Mantooth, H.A., "Performance Requirements of Power MOSFET models", in IEEE Trans. Power Electronics, vol. 10., no. 3, pp. 36-45, May 1995.

[3] Tsividis, Yannis, "Operation and Modeling of the MOS Transistor", McGraw Hill, 476-477, 1987.

[4] Y. Subramanian, P.O. Lauritzen, K.R. Green, "Two Lumped-Charge Based Power MOSFET Models", to be published in Proceedings of the Sixth IEEE Workshop on Computers in Power Electronics, Como, Italy, July 1998.

[5] Bi, Yafei, "Compact Modeling of Power Bipolar Transistor and Parasitic Bipolar Transistor", M.S.E.E. Thesis, University of Washington, Seattle, 1998.