

# The Lumped-Charge Power MOSFET Model, Including Parameter Extraction

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**Abstract**—A fundamentally new, physically-based power MOSFET model features continuous and accurate curves for all three interelectrode capacitances. The model equations are derived from the charge stored on two internal nodes and the three external terminals. A straightforward parameter extraction technique uses the standard gate-charge plot or process data and is matched with interelectrode capacitance measurements. Simulations are in excellent agreement with measurements. The model is used to design a snubber for a flyback converter.

## I. INTRODUCTION

THE interelectrode capacitances of power MOSFET's are important to model accurately, especially the variation of gate transfer capacitance  $C_{GD}$  which dominates the output switching waveforms through the "Miller" effect. Most power MOSFET models use the basic SPICE MOSFET model as a core element with added active and passive components to form a subcircuit. These models tend to be complex with a narrow range of accuracy. Numerous models have been proposed since 1980 [1]. Simas *et al.* [2] were the first to model the nonlinearities in the gate-source capacitance as well as the gate-drain capacitance followed by Xu [3] and Cordonnier [4]. Scott and Franz [5] were the first to model the three interelectrode capacitances and their interaction for all device operating states in a special subcircuit model. Most of these models produce discontinuous  $C-V$  curves. Continuous derivative of charge (capacitance) curves are important for accurate simulation of current waveforms during switching. A simple physical model of the power MOSFET is needed, where the interelectrode capacitances are continuous and can be directly determined from measurement or databook information.

This paper describes such a compact, physical power MOSFET model which is designed by discretizing the internal physical structure, enabling simple charge expressions to be functions of the three terminal voltages. This approach represents an extension of the Charge Control [6] and the Lumped Model method introduced by Linvill in the early 1960's [7]. Thus, it is called the *lumped-charge* approach.

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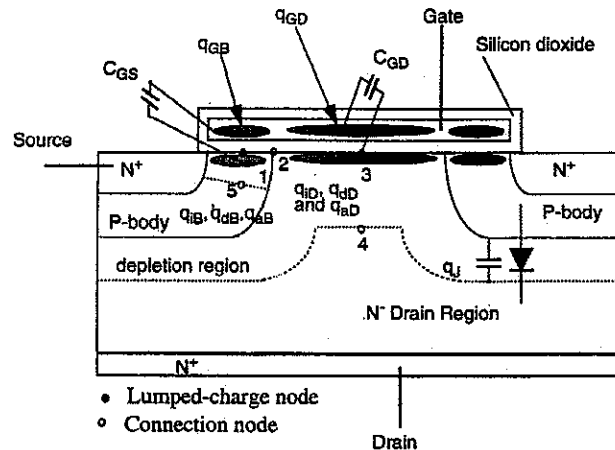


Fig. 1. Location of the nodes containing discretized charges (1, 3) and the internal connection nodes (2, 4, 5).

## II. THE ART OF THE LUMPED CHARGE APPROACH

The lumped-charge modeling technique has recently been established as a powerful method of building power device models. The art is in choosing the model structure to retain the accuracy of physical modeling.

The lumped-charge MOSFET model [8] is based on localizing the internal charge into the separate but key locations shown in Fig. 1. The surface charge is assumed to be lumped into a node at the p-body surface (node 1) and at the n-drain surface (node 3). The internal connection nodes (nodes 2, 4, 5) represent additional nodes needed for defining internal voltages.

The charges at node 1 are calculated using the standard delta-depletion approximation and at node 3, the moderate depletion approximation. These two *lumped-charge* nodes experience accumulation, depletion and inversion as determined from external and internal node potentials. The location of these nodes is carefully chosen to produce relatively simple charge expressions for all operating states of the power MOSFET. Capacitive currents in the terminals of the MOSFET are determined by differentiating these charges with respect to time.

The internal charges are identified as

Body node 1: ~~5~~

$q_{aB}$  = accumulation charge in the body

$q_{dB}$  = depletion charge in the body

$q_{iB}$  = inversion charge in the body.

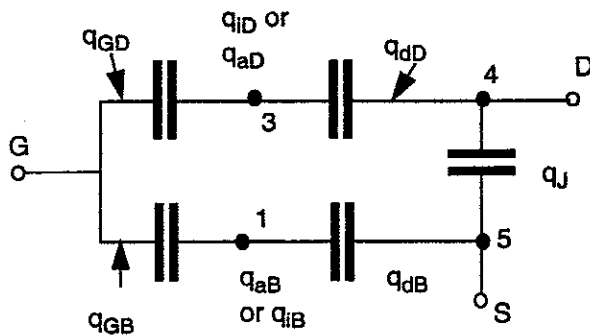


Fig. 2. MOSFET equivalent circuit for the OFF or non conducting state.

Drain node ~~3~~ 4.

$q_{aD}$  = accumulation charge in the drain

$q_{dD}$  = depletion charge in the drain

$q_{iD}$  = inversion charge in the drain

$q_{daD} = q_{dD} + q_{aD}$  = combined depletion and accumulation charge in the drain.

The charges on the gate are:

$q_{GB}$  = gate-body charge

$q_{GD}$  = gate-drain charge.

The charge at the drain-body p-n junction:

$q_J$  = Drain-body junction depletion charge.

### III. EQUIVALENT CIRCUIT

An equivalent circuit for the MOSFET model can be derived from the interaction of the internal charges with the three external terminal voltages. The equivalent circuit for a MOSFET in the nonconducting state is shown in Fig. 2. Overall charge is conserved as the charges on each node appear or disappear as operating states change from one to another.

When all operating states of the device are considered, and the equivalent circuits of all states superimposed, the complete internal equivalent circuit shown in Fig. 3 is obtained. Lumped-charge node 1 contains the charges  $q_{aB}$ ,  $q_{dB}$ , and  $q_{iB}$  which produce the gate capacitance. Also, the charge  $q_{iB}$  determines the channel conductance for the current  $I_D$ . This charge determines the static device I-V characteristics for both the saturation and nonsaturation regions. The drain-body diode is modeled using the Lauritzen-Ma model [9] to include reverse recovery. The complete MOSFET model provides the basic forward and reverse I-V characteristics as well as all inter electrode capacitance variations.

### IV. DERIVATION OF THE CHARGE MODEL

The p-body interface charges are modeled by the standard delta-depletion, strong inversion approximation. Then, channel current  $I_D$  can be simply determined [12] from  $q_{iB}$  which produces equations similar to those in the standard SPICE (level 1) MOSFET model. As the gate bias  $v_{GS}$  sweeps from a highly positive to a lower voltage, the p-body surface goes through inversion to depletion and finally accumulation. At high  $v_{GS}$  the body surface potential  $\psi_{sB}$  remains at the

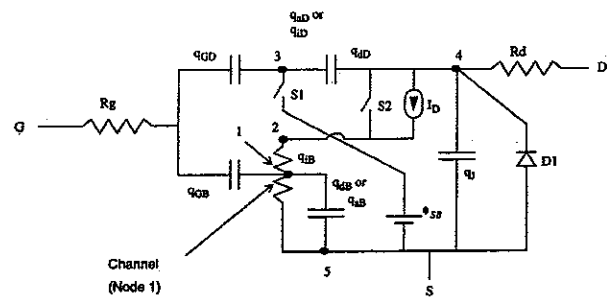


Fig. 3. The complete lumped-charge equivalent circuit for the power MOSFET. NOTE: The switch S1 represents the internal connection between body and drain surface when drain inversion occurs. The switch S2 represents the transition from nonsaturation to saturation operation.

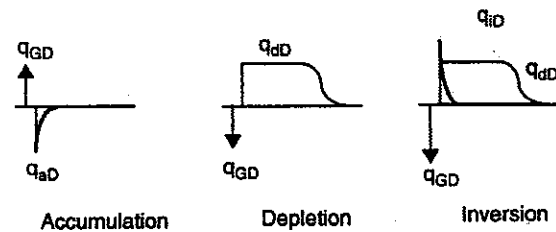


Fig. 4. The charge distributions for the n-drain interface using the moderate approximation.

constant potential  $\phi_{sB}$  while the surface is in *inversion*. The surface potential  $\psi_s$  is defined as the potential change from the bulk to the surface in MOS devices [12] and  $\phi_{sB}$  is the maximum surface potential between body and source regions. The lumped charges (node 1) at the gate-body interface can be determined from the following equations:

$$\psi_{sB} = \phi_{sB} + \frac{v_{2S}}{2} \quad (1)$$

$$q_{GB} = C_{GSon} \times (v_{GS} - V_{fbB} - \psi_{sB}) \quad (2)$$

$$q_{dB} = -C_{GSon} \gamma_B \sqrt{\psi_{sB}} \quad (3)$$

$$q_{aB} = 0 \quad (4)$$

$$q_{iB} = -(q_{GB} + q_{dB}) \quad (5)$$

where

$$\gamma_B^2 = \left[ \frac{(V_{TB} V_{fbB} - \phi_{sB})^2}{\phi_{sB}} \right] = G_B, \text{ the "body effect" term and } \quad \times$$

$C_{GSon}$  = gate-source oxide-capacitance,  $V_{fbB}$  = body flat-band voltage,  $V_{TB}$  = body threshold voltage,  $\phi_{sB}$  = built in voltage between body and source regions

The constants represent model parameters which are listed in Table I.

Once  $v_{GS}(t)$  drops below the *threshold voltage*  $V_{TB}$ , the p-body surface changes from *inversion* to *depletion*, and the surface potential  $\psi_{sB}$  becomes a function of  $v_{GS}$ :

$$\psi_{sB} = v_{GS} - V_{fbB} + \frac{G_B}{2} \left[ 1 - \left( \frac{4(v_{GS} - V_{fbB})}{G_B} + 1 \right)^{1/2} \right] \quad (6)$$

$$q_{dB} = -C_{GSon} \sqrt{(G_B \times \psi_{sB})} = -q_{GB} \quad (7)$$

$$q_{iB} = 0 \quad (8)$$

$$q_{aB} = 0. \quad (9)$$

TABLE I  
COMPARISON OF PARAMETERS WITH SPICE LEVEL 1 POWER MOSFET MODEL

SPICE MOSFET level 1	L-C power MOSFET parameters		COMMENTS
	Discrete device Simulation	Equations for Power IC Design (see Appendix B)	
dc Characteristics			
vto (V <sub>TO</sub> )	V <sub>TB</sub>	(B7)	body threshold voltage
kp (K <sub>p</sub> )	K <sub>p</sub>	(B8)	transconductance
phi (φ)	(φ <sub>SB</sub> ), (φ <sub>DB</sub> )	N <sub>Emitter</sub> , N <sub>Body</sub> , N <sub>Drain</sub>	source-body and drain-body built-in voltages, N = doping
lambda (λ)			if desired see [15]
gamma (γ)	G <sub>B</sub> , G <sub>D</sub>	(B9, B10)	body effect G <sub>B</sub> = γ <sub>B</sub> <sup>2</sup> , G <sub>D</sub> = γ <sub>D</sub> <sup>2</sup>
	delta (δ)	δ (γ)	body effect (see Appendix B) for extraction procedure see [12]
Capacitances			
C <sub>GBO</sub>	C <sub>gov</sub>	t <sub>ox</sub> , W, L <sub>overlap</sub>	gate-source overlap capacitance, t <sub>ox</sub> = thin oxide thickness, W = channel width, L <sub>overlap</sub> = gate overlap length
C <sub>GD0</sub>	C <sub>GDon</sub>	t <sub>ox</sub> , A <sub>drain</sub> (B11)	gate-drain ON-state capacitance, A <sub>drain</sub> = drain area
C <sub>GSO</sub>	C <sub>Gson</sub>	t <sub>ox</sub> , A <sub>body</sub> (B12)	gate-source ON-state capacitance, A <sub>body</sub> = body area
C <sub>j</sub>	C <sub>j0</sub>	W <sub>n</sub> , A <sub>junction</sub>	body-drain diode zero bias capacitance W <sub>n</sub> = N-drain depletion layer width, A <sub>junction</sub> = body-drain junction area
	m		junction gradient factor
	V <sub>fbD</sub> , V <sub>TD</sub>	(B13)	drain flatband and threshold voltages
Body-Drain Diode			
I <sub>s</sub>	I <sub>so</sub>		body-drain diode reverse saturation current
	no		emission coefficient
	tau		carrier lifetime
	T <sub>M</sub>	(B14)	diffusion transit time
Parasitic Resistances			
	R <sub>g</sub>		gate parasitic resistance
R <sub>s</sub>			source parasitic resistance
R <sub>d</sub>	R <sub>d</sub>	N <sub>D</sub> , t <sub>N-drain</sub> , A <sub>drain</sub>	drain parasitic resistance, t <sub>N-drain</sub> = bulk N <sub>drain</sub> thickness, N <sub>D</sub> = drain-bulk doping concentration

As the gate bias  $v_{GS}(t)$  drops below the *body flat-band voltage*  $V_{fbB}$ , the surface enters *accumulation*:

$$\psi_{sB} = 0 \tag{10}$$

$$q_{aB} = C_{Gson} \times (v_{GS} - V_{fbB}) = -q_{GB} \tag{11}$$

$$q_{iB} = 0 \tag{12}$$

$$q_{dB} = 0. \tag{13}$$

If drain interface charges are modeled using the standard delta-depletion approximation, discontinuities and bumps occur in the  $C(v)$  plots [11]. Using the moderate-depletion approximation [8], the charge expressions and the  $C(v)$  plots become continuous for all values of terminal voltage. The charge distributions for the n-drain interface using the moderate approximation are shown in Fig. 4.

As the gate bias  $v_{GD}$  sweeps from a highly positive to a very low voltage, the n-drain interface starts in accumulation with the *drain surface potential* on the n-drain interface  $\psi_{sD} \geq 0$ . Once  $v_{GD}$  drops below the *drain flat-band voltage*  $V_{fbD}$  the n-drain surface changes to depletion with  $\psi_{sD} < 0$ . No discontinuity occurs in this transition since the charges decrease or increase exponentially. Finally, when the gate

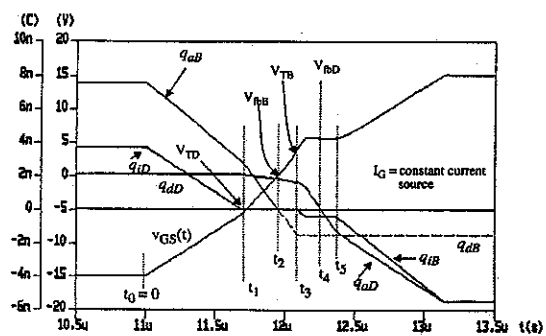


Fig. 5. Simulation of  $v_{GS}(t)$  and the charge conditions at drain and body interfaces.

to drain bias  $v_{GD}$  goes below the *drain threshold voltage*  $V_{TD}$ , the inversion layer starts to build up. The following simple equation describes the n-drain interface charge for both accumulation and depletion conditions.

$$q_{aD} = \mp C_{GDon} \gamma_D \sqrt{(\phi_t \times e^{(\psi_s/\phi_t)} - \psi_s - \phi_t)} \tag{14}$$

The inversion charge  $q_{iD}$  which depends upon  $V_{DS}$ , is ex-

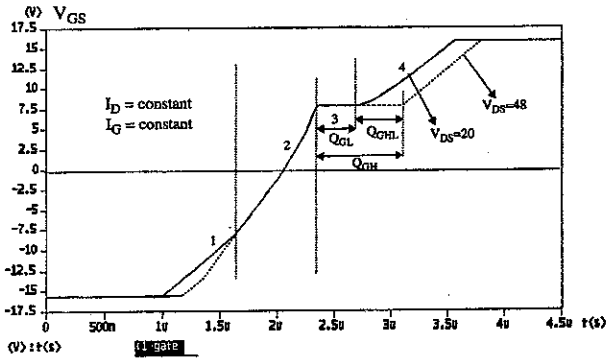


Fig. 6. MOSFET gate charge plot. Four parameters can be obtained from this gate charge plot ( $C_{GDon}$ ,  $C_{GSon}$ ,  $V_{fbD}$ ,  $V_{TD}$ ). Plots in databooks also can be used even though they contain only positive values of  $V_{GS}$ .

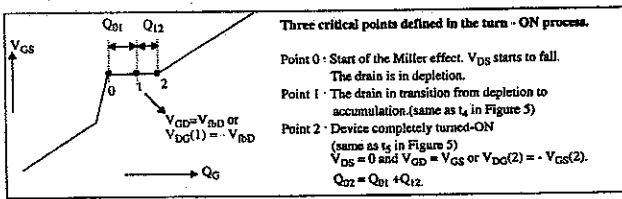


Fig. 7 The three critical points in the turn-ON process within the Miller effect.

pressed by

$$q_{iD} = Q_{CD} - q_{adD} \quad (15)$$

where

$C_{GDon}\gamma_D = \sqrt{2q\epsilon_s N_D} A_{drain}$  (drain area)  
 $\gamma_D$  = gate to drain body effect,  
 $\phi_t$  = thermal voltage,  
 $C_{GDon}$  = the gate-drain oxide-capacitance.

Equations (14) and (15) are explained in Appendix A. The surface potential  $\psi_{sD}$  is expressed by

$$\psi_{sD} = v_{GD} - V_{fbD} + \frac{(q_{iD} + q_{adD})}{C_{GDon}} \quad (16)$$

By inspection of the equivalent circuit in Fig. 3, the drain current  $i_D$  can be expressed as

$$i_D = -\left(\frac{K_p}{C_{GSon}}\right) q_{iB} v_{2S} - \frac{d(q_{daD} + q_J)}{dt} - i_{DD} \quad (17)$$

for operation in both the nonsaturation and saturation regions. Here:

$K_p$  = the empirical "transconductance parameter" used in the SPICE MOSFET model

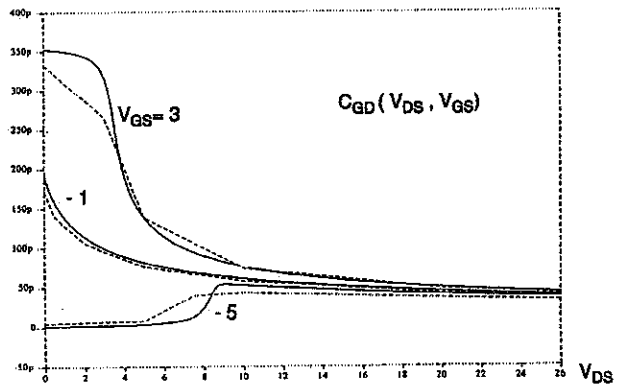
$v_{2s}$  = the voltage between node 2 and the source.

$i_{DD}$  = the body diode current.

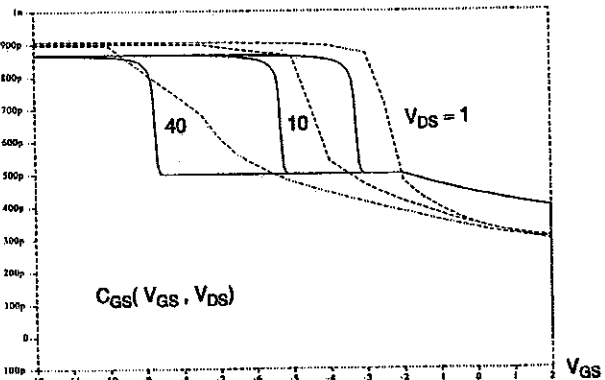
Also, the gate current

$$i_G = \frac{d(q_{GB})}{dt} + \frac{d(q_{GD})}{dt} \quad (18)$$

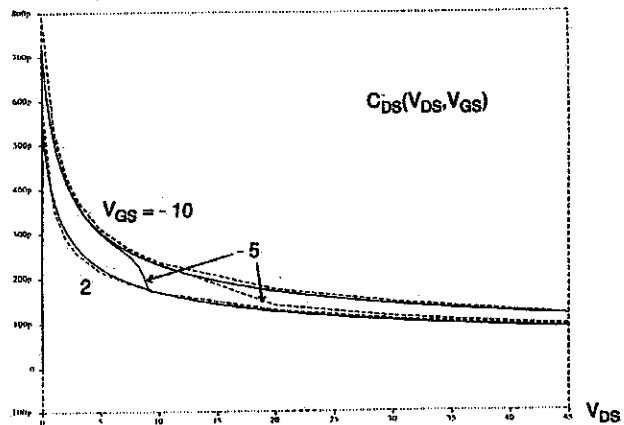
Dependence of mobility on vertical electric field, channel length modulation, velocity saturation and temperature effects are not included in this basic power MOSFET model. However, they can be easily added [15]



(a)



(b)



(c)

Fig. 8. (a) Gate transfer capacitances  $C_{GD}(V_{DS}, V_{GS})$ . Simulations are solid lines, measurements are dotted. (b) gate-to-source capacitances  $C_{GS}(V_{GS}, V_{DS})$ . Simulations are solid lines, measurements are dotted. (c) drain-to-source capacitances  $C_{DS}(V_{GS}, V_{DS})$ . Simulations are solid lines, measurements are dotted.

### V. IMPLEMENTATION

The equations are implemented in the Saber circuit simulator using its MAST modeling language. Simulation of the various internal charges is shown in Fig. 5 as the MOSFET makes the transition from OFF to ON state. A unique feature of the lumped-charge model is the insight given to device operation by simulating the dynamic charge variations at the drain and body regions during this turn-ON process.

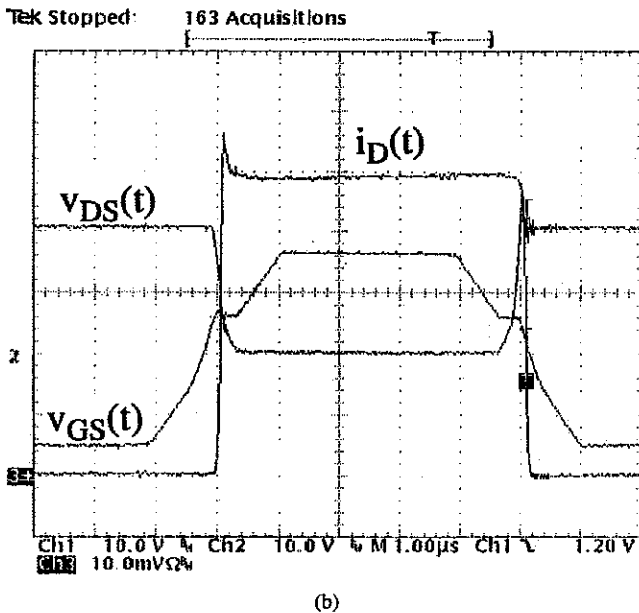
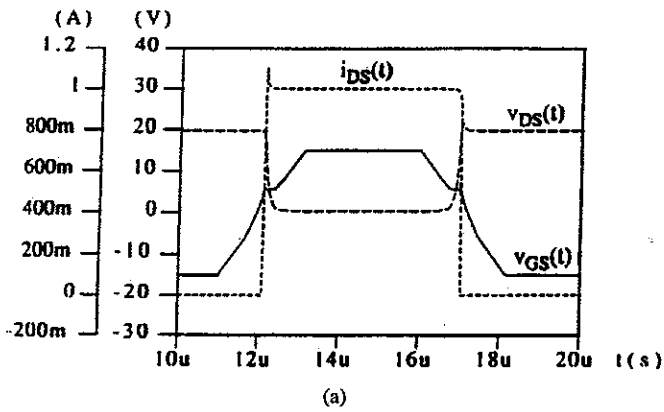


Fig. 9. (a) Simulated gate charge plot. (b) measured gate charge plot.  $i_D(t) = 1$  A,  $i_G(t) = 12$  mA.

At time  $t = t_0$  the constant current source  $I_G$  starts charging the gate. The initial condition for the gate voltage  $v_{GS}(t_0) = -15$  V.

$t_1$ : Drain in transition from inversion to depletion  $V_{GD} = V_{TD}$ , drain threshold voltage. The drain inversion charge is zero ( $q_{iD} = 0$ ).

$t_2$ : Body in transition from accumulation to depletion  $V_{GS} = V_{fbB}$ , body flatband voltage.  $q_{aB} = 0$  and  $q_{dB} = 0$ .

$t_3$ : Body in transition from depletion to inversion  $V_{GS} = V_{TB}$ , body threshold voltage.  $q_{iB} = 0$ .

$t_4$ : Drain in transition from depletion to accumulation  $V_{GD} = V_{fbD}$ , drain flatband voltage.  $q_{daD} = 0$ .

$t_5$ : The "Miller" effect ends, the drain is in strong accumulation; the body is in strong inversion.  $C_{GD}$  is constant at its maximum value as  $v_{GS}(t)$  increases up to +15 V.

## VI. EXTRACTION OF THE PARAMETERS

The lumped-charge power MOSFET model has a similar dc characteristic as the SPICE level 1 MOSFET model with

addition of the power MOSFET interelectrode capacitances. Table I compares the electrical parameters for the SPICE level 1 model to those in the new lumped charge power MOSFET model. For discrete device simulation, electrically measurable parameters are desired. For power IC device simulation, process based parameters are desired. This model provides both electrical and process based parameters to cover both applications.

The gate capacitance parameters can be extracted from the gate charge plot in Fig. 6. This plot at two values of  $V_{DS}$  contains sufficient information to obtain all the gate capacitance parameters.

In regions 1 and 4:

$$C_{GSon} + C_{GDOn} = \frac{I_G}{\frac{dv_{GS}}{dt}} \quad (19)$$

In region 2:

$$C_{GSon} = \frac{I_G}{\frac{dv_{GS}}{dt}} \quad (20)$$

In region 3, the gate-source voltage  $V_{GS}$  is constant during the Miller effect. The length of this period depends upon the magnitude of the applied drain-source voltage  $V_{DS}$ . The values of  $Q_{01}$  and  $Q_{12}$  defined in Fig. 7 can be calculated by

$$Q_{12} = C_{GDOn}(V_{GS}(2) - V_{fbD}). \quad (21)$$

At point "0" we have

$$-\psi_{sD}(0) = -V_{GD}(0) - \frac{q_{daD}(0)}{C_{GDOn}} + V_{fbD} \quad (22)$$

where

$$q_{daD}(0) = C_{GDOn}\{G_D[-\psi_{sD}(0)]\}^{1/2}. \quad (23)$$

Note that  $Q_{01} = q_{daD}(0)$  is the depletion charge in the drain region and  $G_D$  represents the body effect. Substituting  $-\psi_{sD}(0)$  from (22) into (23) we obtain

$$q_{daD}(0) = C_{GDOn} \left[ G_D \left( -V_{GD}(0) - \frac{q_{daD}(0)}{C_{GDOn}} + V_{fbD} \right) \right]^{1/2}. \quad (24)$$

Solving for  $q_{daD}(0)$ :

$$q_{daD}(0) = \frac{C_{GDOn} G_D}{2} \cdot \left[ -1 + \left( 1 - \frac{4(V_{GD}(0) - v_{fbD})}{G_D} \right)^{1/2} \right]. \quad (25)$$

Applying (25) to two values of  $V_{DS}$  (the high value is  $V_{DSH}$  and the low value is  $V_{DSL}$ ), the following equations are obtained, where  $Q_{GHL}$  and  $Q_{GL}$  are defined in Fig. 6:

$$Q_{GHL} = q_{daD}(V_{DSH}) - q_{daD}(V_{DSL}). \quad (26)$$

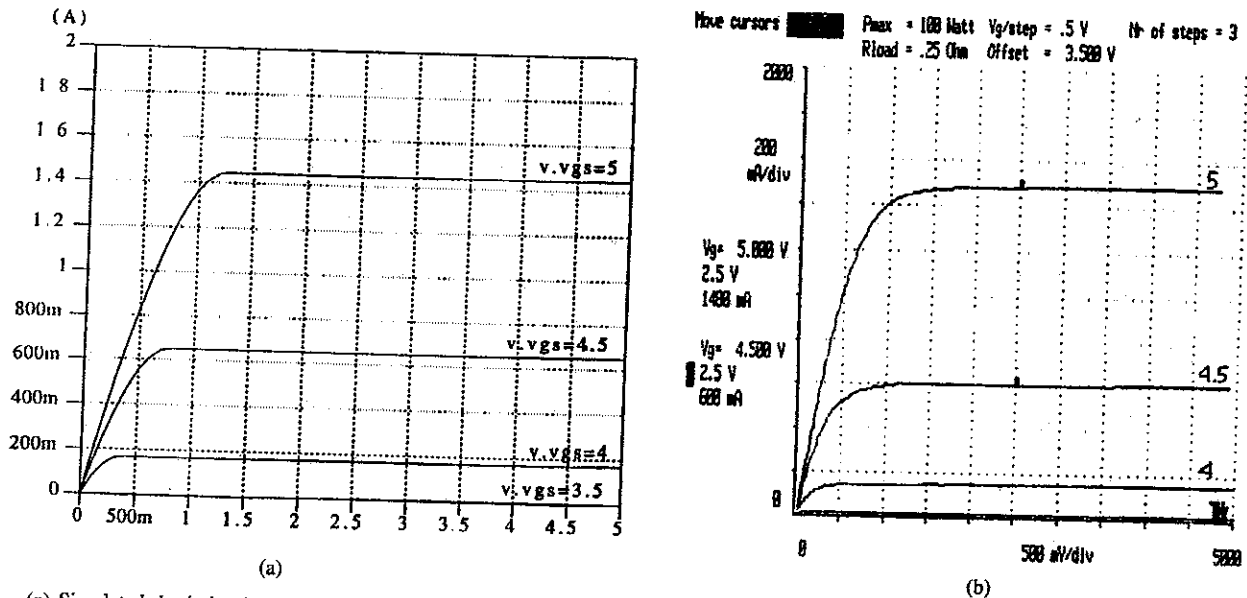


Fig. 10. (a) Simulated dc drain characteristics (Motorola MTP8N08), (b) measured dc drain characteristics (Motorola MTP8N08).

*X*  $V_{GDH}$  &  $V_{GDL}$  are the gate-drain voltages at the intersections of 4 & 3 in Fig. 6.

For normal voltages (26) can be approximated as

$$Q_{GHL} = (C_{GDon} G_D^{1/2}) [(-V_{GDH})^{1/2} - (-V_{GDL})^{1/2}] \quad (27)$$

Equation (27) can be solved directly for  $G_D$ . Then

$$Q_{GL} = \frac{C_{GDon} G_D^{1/2}}{2} \left[ -1 + \left( 1 - \frac{4(V_{GDL} - V_{fbD})}{G_D} \right)^{1/2} \right] + C_{GDon}(V_{GSM} - V_{fbD}) \quad (28)$$

*X* and "Miller" voltage in Fig. 6

$$G_D = \frac{(-V_{TD} + V_{fbD} - \phi_{DB})^2}{\phi_{DB}} = \gamma_D^2 \quad (29)$$

where

$\phi_{DB}$  = built in voltage between body and drain regions (approximately =  $2\phi_{FN}$ )

Equation (28) can be solved for  $V_{fbD}$  and, (29) for  $V_{TD}$ .

As an example the parameters for MOTOROLA P8N08 Power MOSFET are determined from its databook using  $V_{DSH} = 48$  and  $V_{DSL} = 20$ , to give

$$Q_{GHL} = 1.5 \times 10^{-9} \text{ Coulomb}$$

$$Q_{GL} = 5.5 \times 10^{-9} \text{ Coulomb.}$$

From (19) to (20) and (28) to (29) we obtain

$$C_{GSon} = 370 \text{ pf}$$

$$C_{GDon} = 600 \text{ pf}$$

$$V_{fbD} = 0.775 \text{ Volt}$$

$$V_{TD} = -0.433 \text{ Volt.}$$

Parameters for dc characteristics like  $V_{TB}$ ,  $K_p$  and the drain-source capacitance parameters  $C_{j0}$ ,  $m$ ,  $\phi_{DB}$  are found conventionally [10].

### VII. SIMULATION AND MEASUREMENT RESULTS

Using parameters extracted from the gate-charge plot, simulated interelectrode capacitances are compared with measured values in Fig. 8. The interelectrode capacitances are measured at 1 MHz using a three terminal measurement technique. Simulated and measured gate charge plots are shown in Fig. 9. In the gate charge plot, both gate and drain are driven by a constant current sources. Simulated and measured dc drain characteristics are in Fig. 10.

To demonstrate an application, the MOSFET model is used to design a snubber for a flyback converter operating in the discontinuous conduction mode. Fig. 11(a) shows switching waveforms without the snubber installed and Fig. 11(c) shows the simulated waveform. Note that the peak switch voltage is approximately 120 V in both plots. Fig. 11(b) and Fig. 11(d) show measurement and simulation of the flyback converter with the snubber designed using the simulator. Note the excellent match between simulation and measurements.

### VIII. CONCLUSION

This power MOSFET represents a fundamentally new model which is equivalent in complexity to the SPICE MOSFET model used for low voltage devices. The model is compact with all static and dynamic effects combined into a single set of equations. The capacitances  $C_{GD}(v)$  and  $C_{GS}(v)$  are continuous functions with continuous derivatives, yet capacitance parameters can be directly extracted from the simple gate charge plot found in data books or from simple measurements. This power MOSFET model demonstrates that the lumped-charge approach, which was first demonstrated on the P-I-N diode [9] is also valid for MOS devices. The availability of new, accurate power device models will change the design methodology in power electronics and eliminate much of the need for prototyping new circuits.

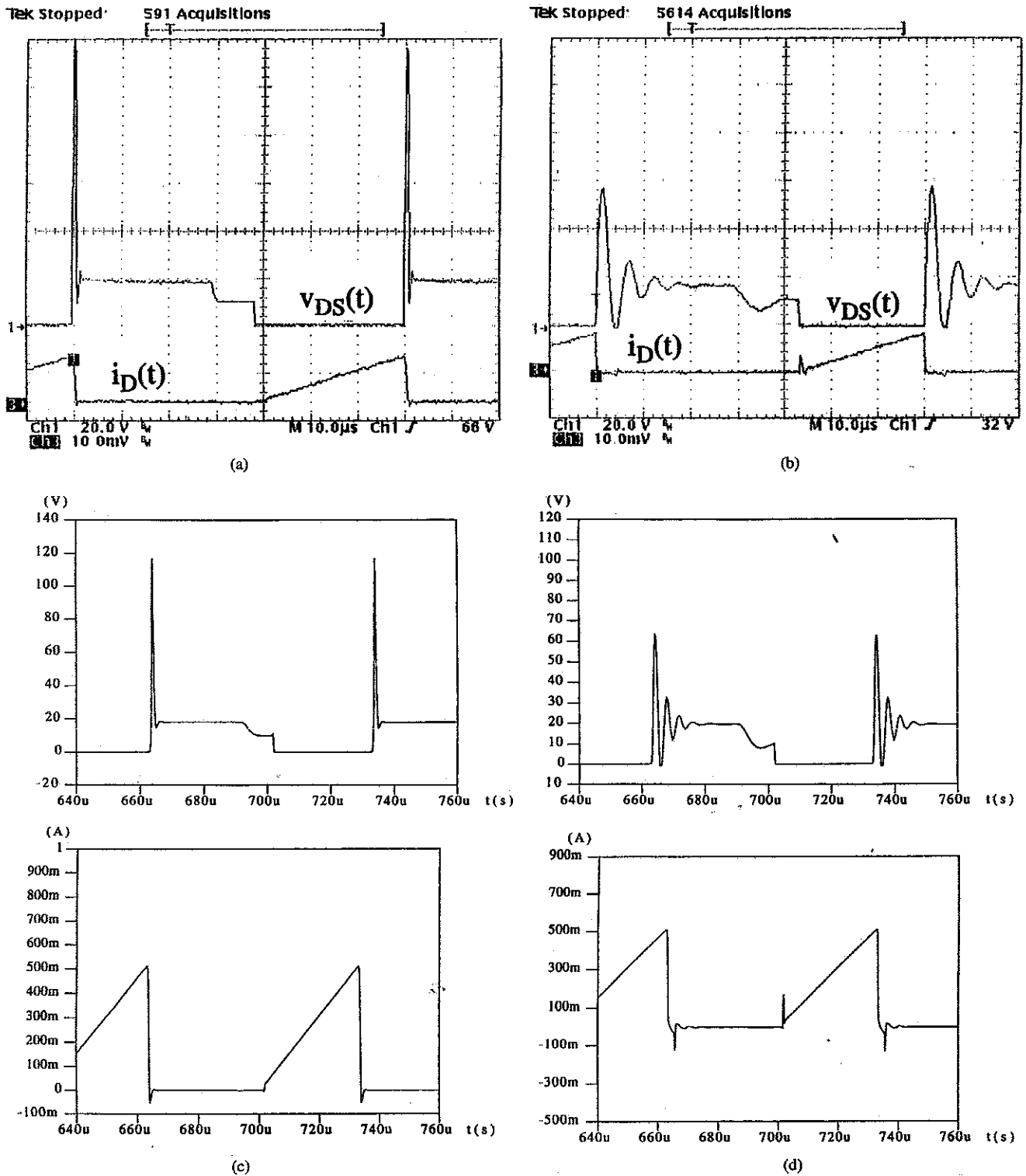


Fig. 11. (a) Measurement of  $v_{DS}(t)$  and  $i_D(t)$  in flyback converter. (Without Snubber.) Scale for  $i_D(t)$ : 0.5 Ampere/division. (b) measurement of  $v_{DS}(t)$  and  $i_D(t)$  in flyback converter. (With Snubber.) Scale for  $i_D(t)$ : 0.5 Ampere/division. (c) simulation of  $v_{DS}(t)$  and  $i_D(t)$  in flyback converter. (Without Snubber.) (d) simulation of  $v_{DS}(t)$  and  $i_D(t)$  in flyback converter. (With Snubber.)

APPENDIX A

DERIVATION OF THE INTERFACE CHARGES AT THE N-DRAIN SURFACE

The interface charge  $Q_{CD}$  described in Appendix of [12] for an N-type substrate can be expressed by

$$Q_{CD} = \mp \sqrt{2q\epsilon_s N_D} A_{drain}$$

$$\left\{ \begin{aligned} &\phi_t \exp\left(\frac{\psi_{sD}}{\phi_t}\right) - \psi_{sD} \\ &- \phi_t + \exp\left(\frac{-2\phi_{FN}}{\phi_t}\right) \end{aligned} \right. \quad (A1)$$

$$\left[ \phi_t \exp\left(\frac{-\psi_{sD} + V_{BD}}{\phi_t}\right) + \psi_{sD} - \phi_t \exp\left(\frac{V_{BD}}{\phi_t}\right) \right]$$

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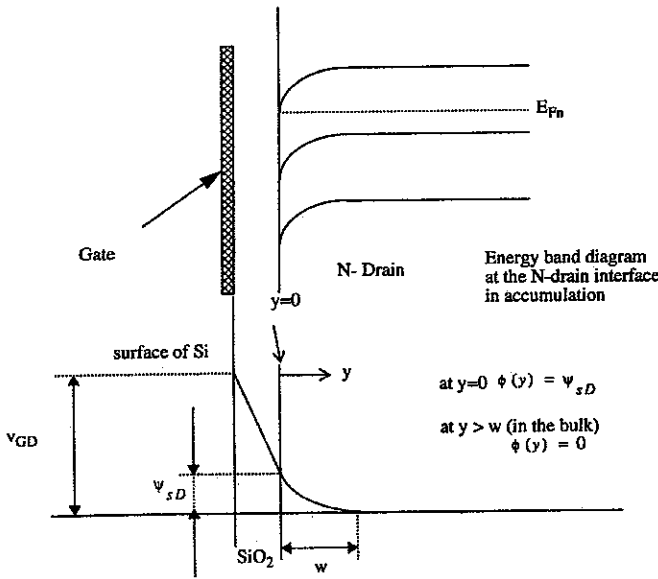


Fig. 12. Energy band and potential  $\Phi(y)$  diagrams as function of distance  $y$  from the drain surface interface. The surface is in accumulation mode.

In the moderate depletion approximation, the inversion layer charge increases exponentially when the surface potential  $\psi_{sD}$  is approximately  $2\phi_{FN}$ .

The accumulation and depletion charges must be separated from the inversion charge because their dynamic behavior is different.

Equation (A1) can be simplified for  $e^{(2\phi_{FN}/\phi_t)} \ll 1$  to separately describe the interface accumulation and depletion charge  $q_{adD} = q_{aD} + q_{dD}$  from the inversion charge  $q_{iD}$ .

$$q_{adD} = \mp C_{GD_{on}} \gamma_D \sqrt{(\phi_t \times e^{(\psi_s/\phi_t)} - \psi_s - \phi_t)} \quad (A2)$$

The inversion charge  $q_{iD}$  which also depends upon  $V_{DS}$ , is expressed by

$$q_{iD} = Q_{CD} - q_{adD} \quad (A3)$$

and  $\gamma_D$  = gate to drain body effect,  $\phi_t$  = thermal voltage,  $C_{GD_{on}}$  = the gate-drain oxide capacitance where the N-drain static surface potential  $\Phi(y)$  can be obtained from

$$\psi_{sD} = \frac{V_{GS} - V_{fb}}{V_{GD}} + \frac{q_{iD} + q_{adD}}{C_{GD_{on}}} \quad (A4)$$

APPENDIX B

THE LINEARIZED BODY EFFECT PARAMETER  $\delta$

The width of the depletion layer in the channel varies due to the applied voltage  $V_{DS}$ . The body depletion charge is expressed by

$$Q_{dB} = -\gamma C_{GS_{on}} \sqrt{(\phi_{SB} + V_{CB})} \quad (B1)$$

Fig. 13 shows a plot of  $-(Q_{dB}/C_{GS_{on}})$  from (B1). To simplify (B1) the first two terms of the Taylor series expansion are chosen around the point  $V_{CB} = V_{SB}$  giving

$$-\frac{Q_{dB}}{C_{GS_{on}}} = \gamma \sqrt{(\phi_{SB} + V_{SB})} = \delta_1 (V_{CB} - V_{SB}) \quad (B2)$$

where  $\delta_1$  is the slope of  $-(Q_{dB}/C_{GS_{on}})$  versus  $V_{CB}$  evaluated at point  $V_{CB} = V_{SB}$ .

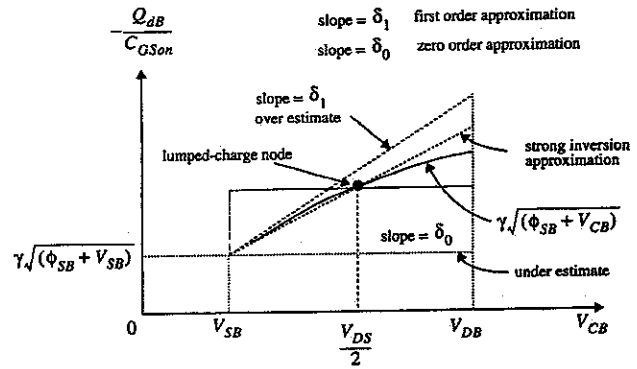


Fig. 13. The quantity  $-(Q_{dB}/C_{GS_{on}})$  in strong inversion versus effective reverse bias in the channel region.

The right hand side of (B2) gives the uppermost broken line in Fig. 13. The correct value and slope at  $V_{CB} = V_{SB}$  is obtained but  $-(Q_{dB}/C_{GS_{on}})$  is overestimated everywhere else.

A better approximation can be obtained by lowering the value of the slope to a value  $\delta < \delta_1$  as shown by the middle broken line:

The lumped-charge node is located at a fixed point located in the middle of the channel. At this point the expression becomes

$$-\frac{Q_{dB}}{C_{GS_{on}}} = \gamma \sqrt{(\phi_{SB} + V_{SB})} + \delta \frac{V_{DS}}{2} \quad (B3)$$

The lumped inversion charge (node 1) is

$$q_{iB} = -C_{GS_{on}} \left[ V_{GS} - V_{TB} - (1 + \delta) \frac{V_{DS}}{2} \right] \quad (B4)$$

and the static current  $I_D$  can be calculated by

$$I_D = -\frac{K_p}{C_{GS_{on}}} q_{iB} v_{2S} \quad (B5)$$

where

$$K_p = \frac{W \mu C_{GS_{on}}}{L A_{body}} \quad (B6)$$

A. Optional Process Structural Parameters for Lumped-Charge Power MOSFET Model

The linearized body effect has been added to the basic model and can be calculated from dc-measurements or from the following equations:

$$V_{TB} = V_{fbB} + \phi_{SB} + \sqrt{(G_B \phi_{SB})} \quad (B7)$$

$$K_p = \frac{W \mu C_{GS_{on}}}{A_{body}} \quad (B8)$$

$$\sqrt{G_B} = \gamma_B = \sqrt{\frac{2q\epsilon_s N_A}{C_{GS_{on}}}} A_{body} \quad (B9)$$

$$\sqrt{G_D} = \gamma_D = \sqrt{\frac{2q\epsilon_s N_D}{C_{GD_{on}}}} A_{drain} \quad (B10)$$

$$C_{GD_{on}} = \frac{\epsilon_{ox} A_{drain}}{t_{ox}} \quad (B11)$$

$$C_{GS_{on}} = \frac{\epsilon_{ox} A_{body}}{t_{ox}} \quad (B12)$$

$$V_{TD} = V_{fbD} + \phi_{DB} + \sqrt{(G_D \phi_{DB})} \quad (B13)$$

$$T_M = \frac{W_n^2}{2D_p} \quad (B14)$$



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