

**Weekly status report:**

Worked together with Chris and Gus on Thursday and Sunday on EKV model. The Verilog code of EKV is finished now but is being debugged.

**Next week plan:**

Will continue work with Chris and Gus to debug the EKV model code and program with VHDL next week. Also will work with Kishore to test the A/D converter using my Verilog Bsim model. I will also take some time to look at the VHDL Bsim code to see whether the trouble Bo's met is caused by my model.