#250: Rapid BSIM Model Implementation with VHDL-AMS/Verilog-AMS and MCAST Compact Model Compiler

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Abstract

VHDL-AMS and Verilog-AMS are behavioral languages extended from widely used VHDL/Verilog for the analog and mixed-signal applications. By describing models in behavioral language VHDL-AMS/Verilog-AMS and then compiling them with model compiler such as MCAST, we have successfully implemented the industry-grade device models (including BSIM, BSIMSOI) rapidly and with low cost, which was previously a tough and high cost work. The implementation for the first time demonstrated the capability and advantages of this new method compared to the traditional methods in device modeling.

1. Introduction

Device modeling is the foundation in circuit design and simulation. The traditional method of translating the device model equations to C/Fortran code requires a lot of inter-stages work and a large amount of expertise in software engineering. Such kind of work is tedious, error-prone and very time-consuming. Considering the device model may need to be updated after some important physical effects have been identified, the heavy burden and high cost of maintaining models prevent many innovative new models from being accepted into commercial simulators [1].

Using the new method of device modeling in VHDL-AMS/Verilog-AMS with model compiler, the above problem can be tackled in an efficient and robust way. We can easily translate the model equations from the model document into high-level description VHDL-AMS code, and use the model compiler MCAST [6] to generate C code that can be easily merged into target simulators. The entire process can take less than two hours.

To demonstrate the practical significance of this promising methodology, it must have the capability to handle industry grade device models. We have successfully implemented the most complex device models, such as BSIM3/BSIMSOI, in both VHDL-AMS and Verilog-AMS. With the model complier MCAST (currently only supports VHDL-AMS) or other Verilog-AMS model compiler, we obtain the automatically generated C code that can be directly compiled into circuit simulators such as SPICE3. The simulation results verified that our behavioral models have the same accuracy as the original BSIM models.

2. Device Model Implementation based on Model Compiler Methodology

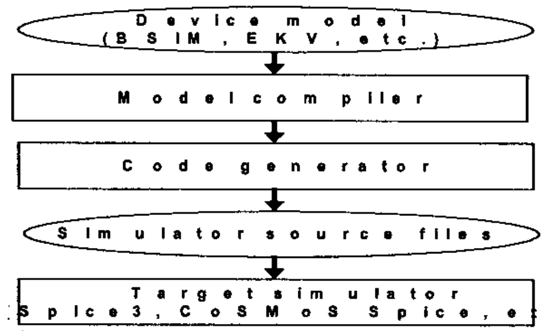

Figure 1. Compiler based model development paradigm.

Fig. 1 shows the flow of new device model development based on model compiler MCAST. It starts from the user input which is a VHDL-AMS file describing a device model. Model compiler parses the information and stores it in an intermediate format [6]. During the code generation, multiple device source codes are produced according to different target simulators. These codes will be compiled and linked with the source files of a target simulator to create a new simulator with the new device models. Using this new simulator allows circuit designers to simulate a circuit consisting of new device models.

3. Compact Device Modeling in Behavioral Languages VHDL-AMS/Verilog-AMS

VHDL/Verilog has been used extensively in the design and verification of digital systems since introduced in 1980s'[2]. The recent extensions to VHDL-AMS/Verilog-AMS greatly enhanced their capability to support the hierarchical description and simulation of continuous and mixed-continuous/discrete systems with conservative and

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nonconservative semantics [2]. A typical VHDL-AMS model has an **entity** with one or more **architectures**. The entity includes the description of the ports of the model and the definition of its generic parameters. The architecture part contains the detailed implementation of the model. Verilog-AMS has some similar properties as VHDL-AMS. The analog behavior described in **analog** module and the behavioral descriptions are mathematical mappings, which relate the input and signals in terms of a large signal or time-domain behavioral description.

4. Experimental Results

Twelve benchmark circuits from different sources were used to test the accuracy and stability of our new device models both in VHDL-AMS and Verilog-AMS. Table 1 shows the statistics of the models in different levels of VHDL-AMS code, where the source code of MCAST and SPICE3 only include code of setup, parameter-calculation and load part.

Table 1. Device Models

Device Model	# Nodes	# Parameters	Complexity (#line of VHDL-AMS code)	MCAST generated codes	SPICE3f5 source codes
MOS Level 1	4	2	40	901	1837
MOS Level 3	4	121	870	3768	2322
BSIM3	4	412	2228	10777	6637
BSIMSOI	6	787	2502	12801	9974

Fig. 2 shows the output waveforms of one test bench with our BSIM3 device models in VHDL-AMS compared to the original SPICE3. The example is an industry-grade class-E power amplifier design used by NeoCAD, which provides high current drive to a load. This example is also tested using the BSIMSOI device models, and MCAST is capable of capturing the same accuracy as SPICE3. The two curves are overlapped with numerical difference in the figure. For Verilog-AMS code, because our complier MCAST currently only supports VHDL-AMS, we only test the Verilog-AMS code model in the Cadence environment. Fig. 3 shows the comparison of CPU time of our BSIM3 model compiled by MCAST with SPICE3. The curves show the simulation times of the behavioral device model compiled by MCAST is about 70% as fast as hand optimized SPICE3 and even in some cases faster.

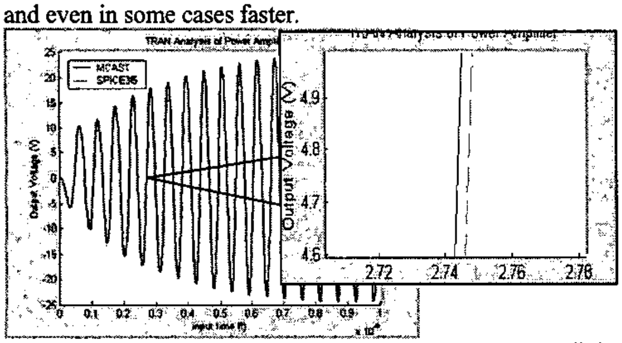

Figure 2. The simulation result of Power Amplifier using MCAST-compiled BSIM3 model and the manually implemented BSIM3 model

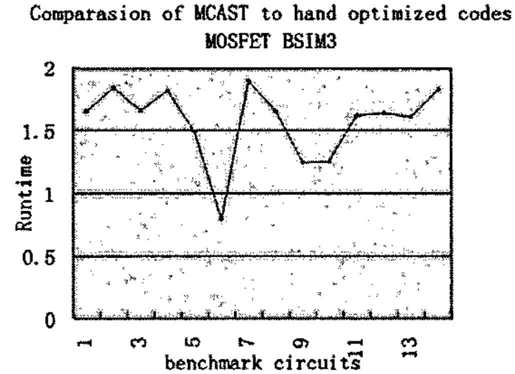

Figure 3. The comparison of CPU time of our BSIM3 model compiled by MCAST with SPICE3.

From these results, we can see that our new models match the manually implemented models accurately. For the sensitive RF circuits such as VCO, Power Amplifier and real industry designs such as Boeing's Comparator, our models are stable, accurate as the manually implemented models but with much lower cost.

5. Conclusions

In the paper, we presented device modeling based on behavioral language VHDL-AMS/Verilog-AMS. We for the first time successfully implemented the industry grade MOS device model BSIM3 and BSIMSOI rapidly and with low cost. And the experimental data shows the accuracy and practical significance of our models and the model compiler MCAST as well. It is quite promising that such kind of methodology could become a very important way for future model developers to shorten their model development cycle and to deliver better device models.

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