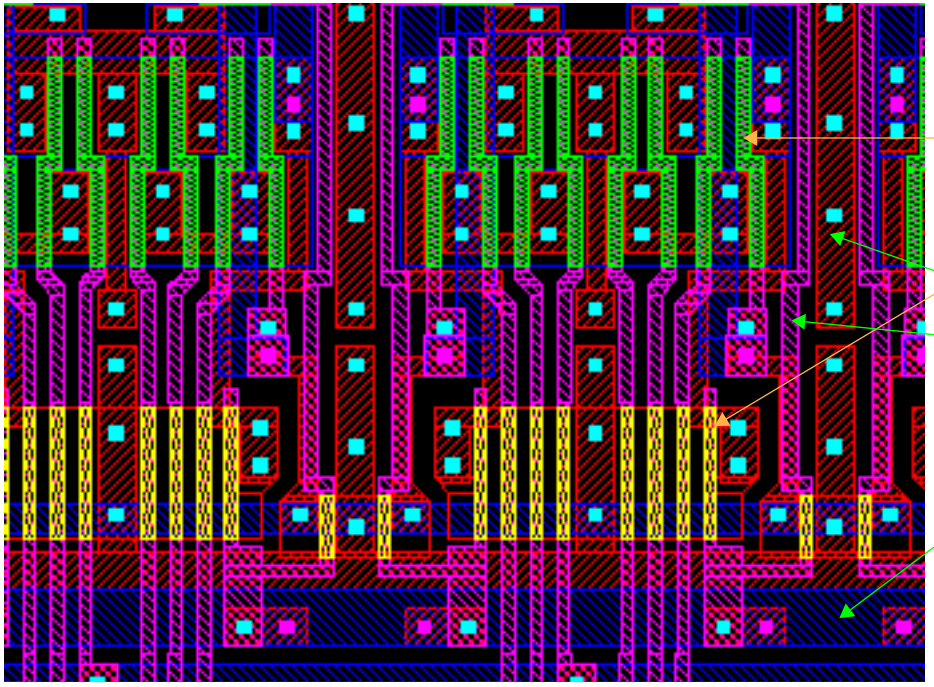
Practical RC Extraction Techniques

- **Why extraction?**
- **Interconnect model**
- **Resistance Extraction**
- **Capacitance Extraction**
- **Rule-based Approach**
- **Formula-based Approach**
- **Table-based Approach**
- **Field solvers**
- **Accuracy Comparison**
- **3D Effects**

Synopsys - Tak K. Young

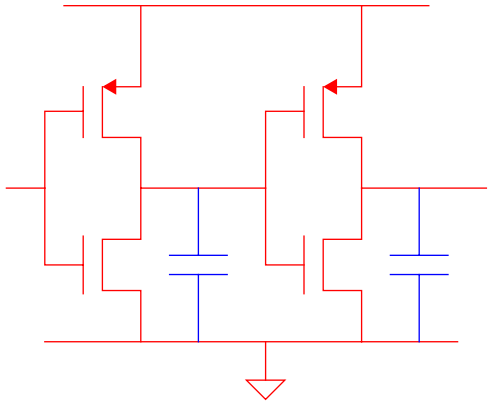
❑ Why extraction?

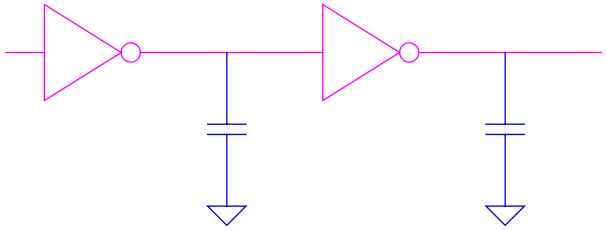
- Extraction is needed to support simulation of the effect due to "parasitic" elements.
- "Parasitic" effects are due to interconnect and are not intended part of the circuit function.
- "Parasitic" effects typically only affect the timing behavior of the circuit. The circuit should perform correctly if the frequency is slow enough.



Interconnect Model: Simple Capacitance

- Represent the interconnect with a simple capacitor.
- This has traditionally been sufficient, before the “sub-micron” circuits.
- This is also sufficient if the interconnect is not too long or the interconnect is not part of the critical path of the circuit.





- The capacitances are typically placed in a load file

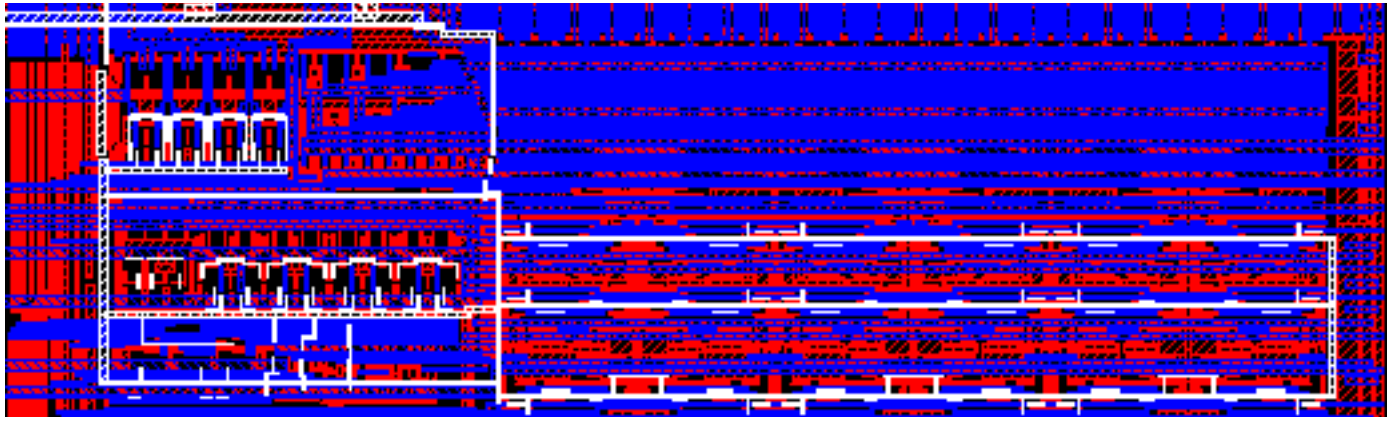
  Example:

  net1 0.235p

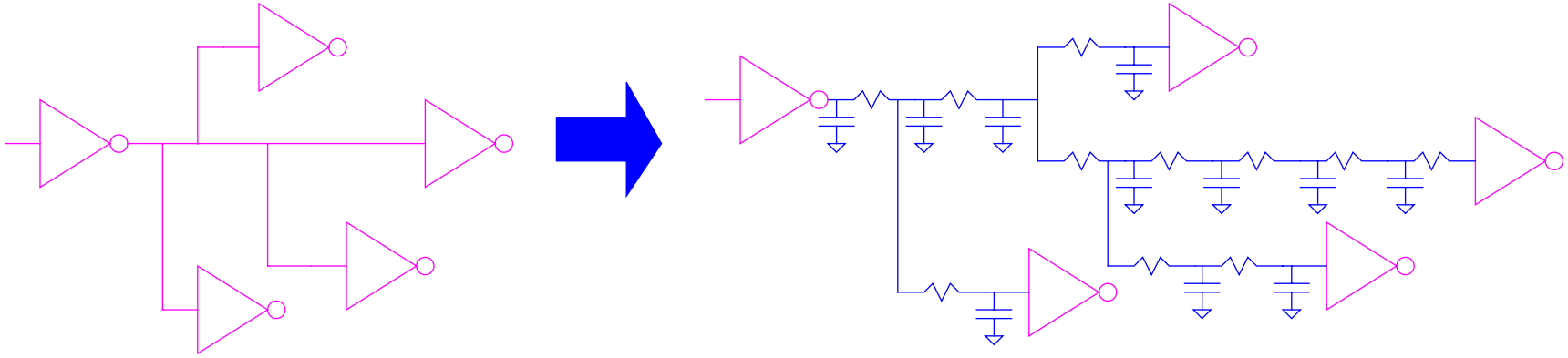
  net2 0.35p

Interconnect Model: Distributed RC

- With submicron circuits, many nets will be very long and will have significant resistance and capacitance.
- The resistance on the long nets will have effect (delay and slope) on the voltage waveforms.



- The interconnect is typically extracted as a RC tree

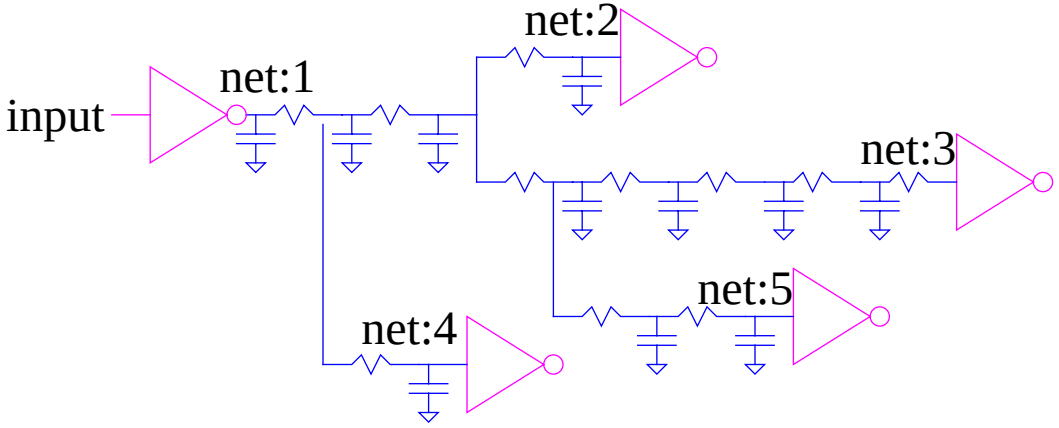


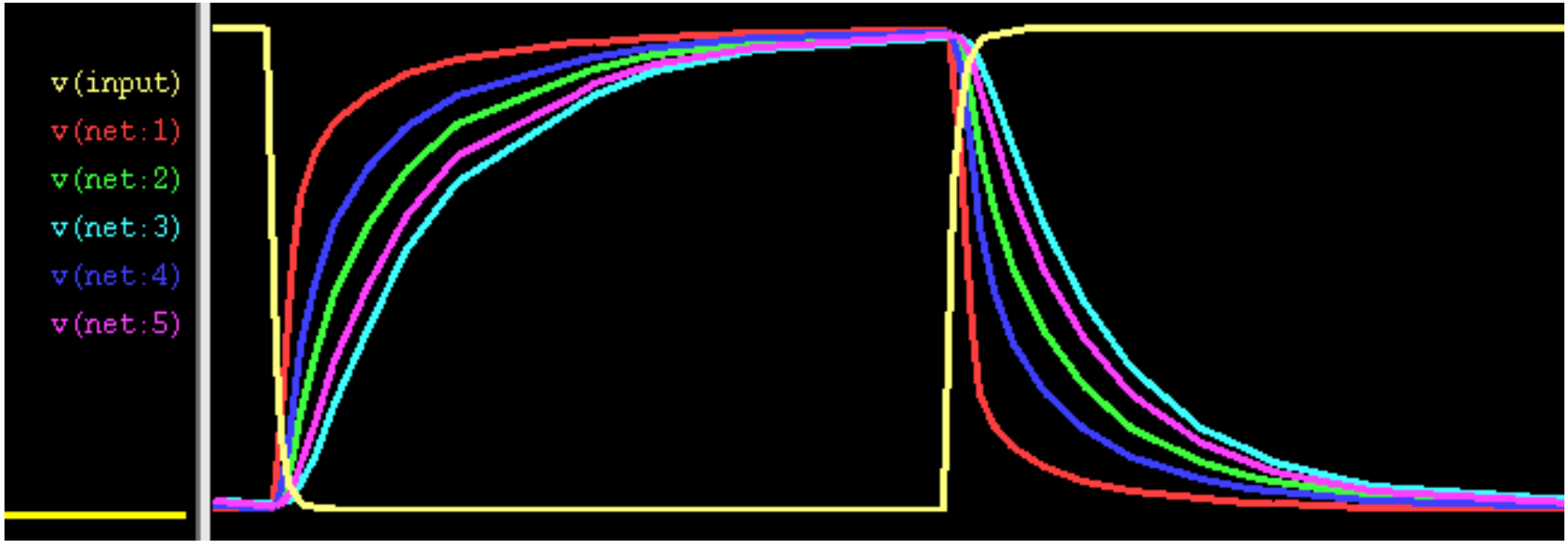
❑ Interconnect Model: Distributed RC (cont.)

- Several issues related for the simulator to use the extracted RC information:
  - One node in the original netlist is now expanded into multiple nodes.
  - The RC tree needs to be connected to the correct nodes
  - The circuit is now much bigger. A circuit of three thousand transistors (and one thousand nodes) can be expanded into a circuit of ten thousand (and sometimes much more) nodes.
- The extractor tool can provide:
  - A new SPICE (or EDIF) netlist with all transistors and RCs.
  - A Standard Parasitic Format (SPF) file
  - A transistor level simulator can annotate the SPF file to the original netlist.
  - For gate level simulator, a delay calculator can convert the SPF file into a delay file (typically in Standard Delay Format - SDF) for simulation.

Interconnect Model: Distributed RC (cont.)

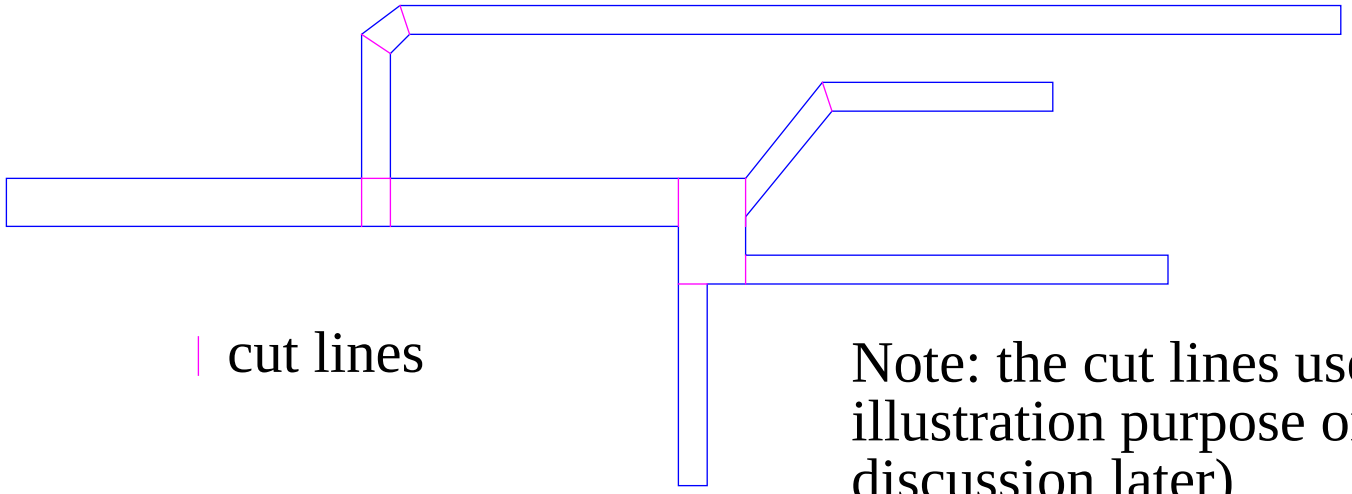
- Effect on simulation waveforms due to distributed RC
  - note the different delay and slope of the waveforms





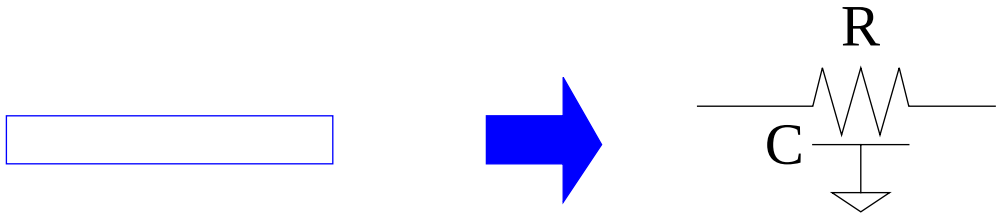
Interconnect Model: Decomposition

- A net needs to be divided into segments



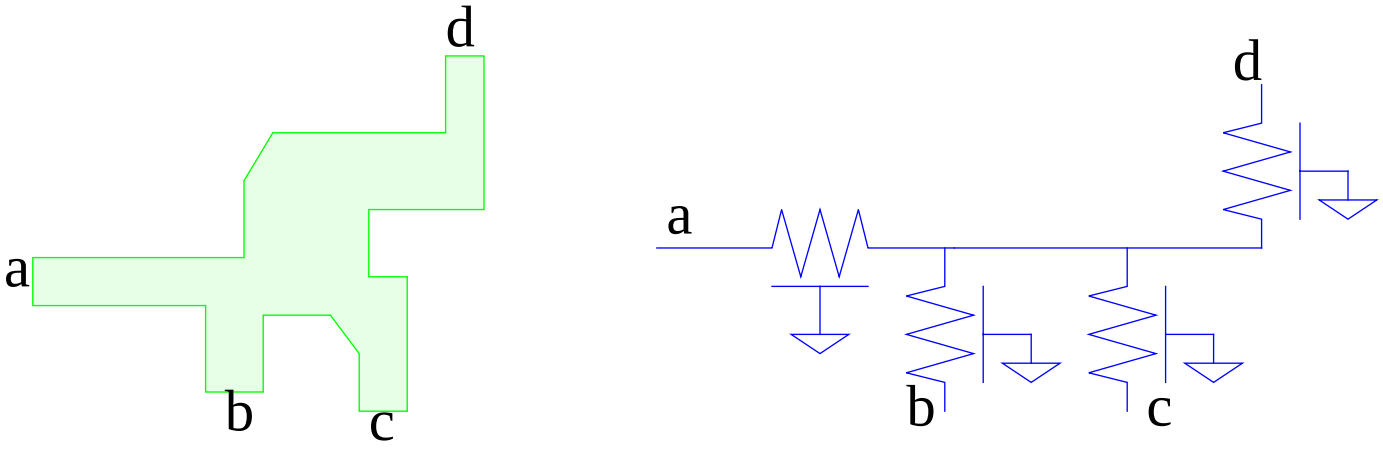
Note: the cut lines used are for illustration purpose only (more discussion later)

- Typically, the resistance value of the segments and the capacitance value of the segments are obtained separately.
- The R and C value for each segment is later combined to form a distributed RC model

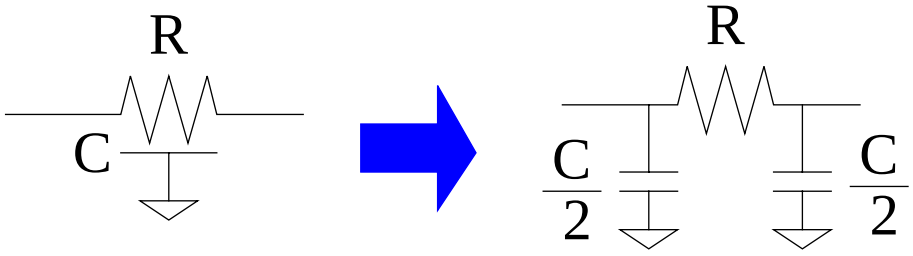


Interconnect Model: Decomposition (cont.)

- Some complex shapes may also need to be modeled

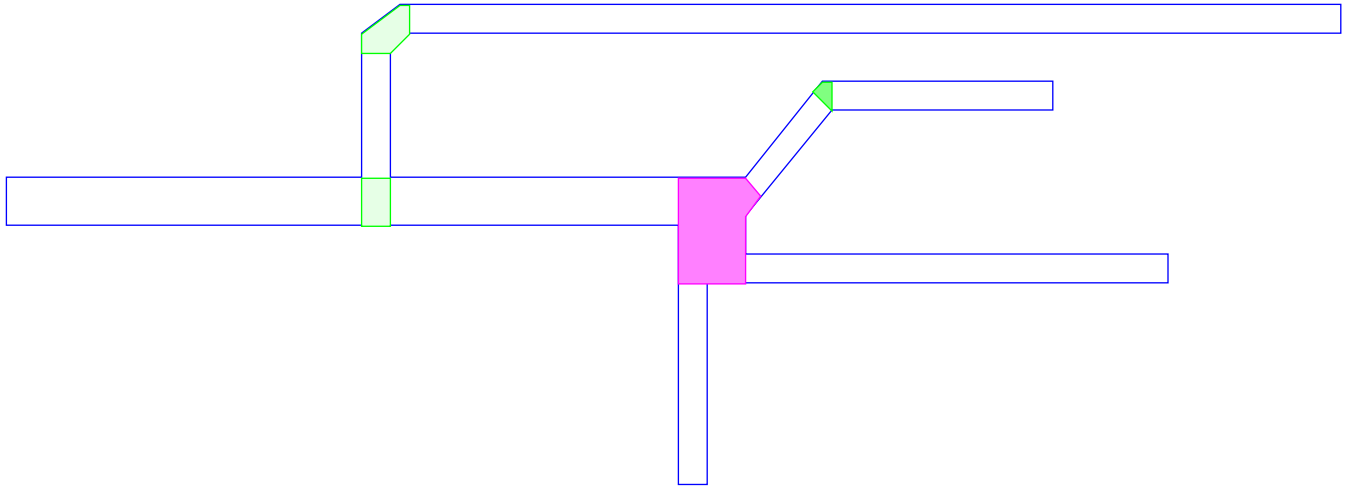


- Each distributed RC can then be modeled by RC
  - typically a Π (PI) model is used



Resistance Extraction

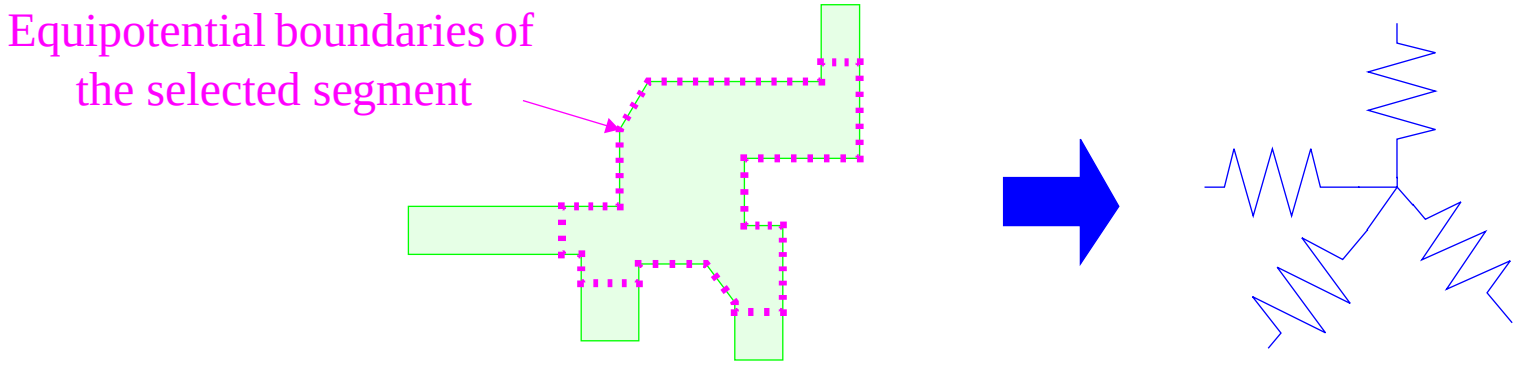
- Traditionally, the cutting is performed at the break points
- Some tool calculate resistance by counting squares
  - Some tools will ignored the non-rectangular shapes



- Some tools will derive the equivalent number of squares for the non-rectangular shapes
  - Some shapes may still be ignored (e.g. irregular shapes or non-45 degree edges)

Resistance Extraction (cont.)

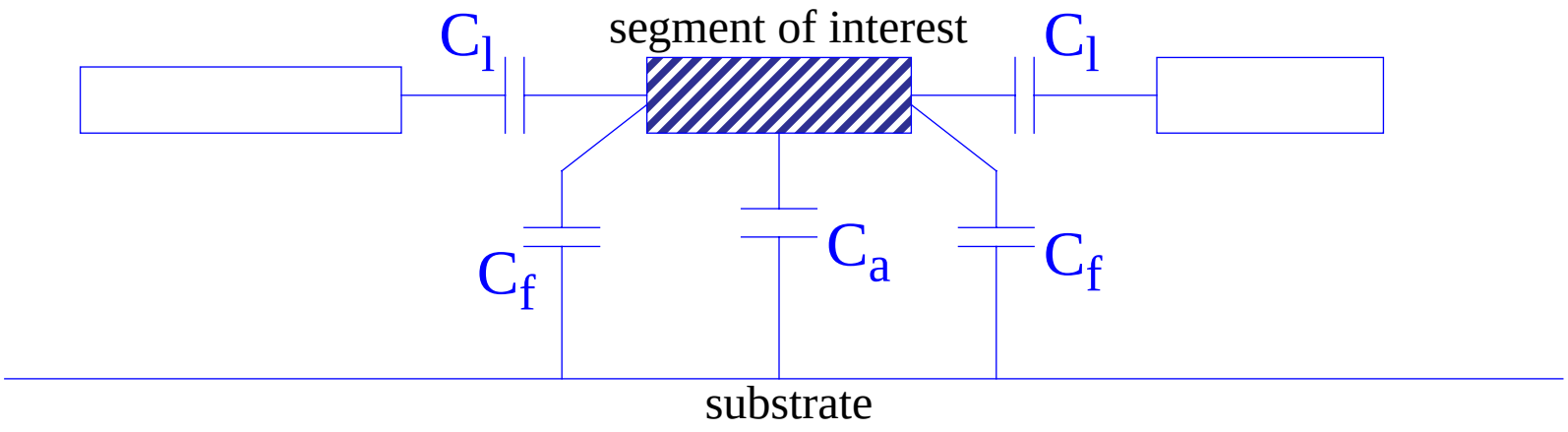
- However, cutting at the break points is not desirable since the electric fields are not uniform
  - Resistance will be more accurate if the cutting is away from the break points where electric fields can be uniform



  - Resistance of the irregular shape can be calculated with a 2D resistance field solver

Capacitance Extraction

- Capacitance of a segment of a net can be divided into three components: area C_a, fringe C_f and lateral C_l

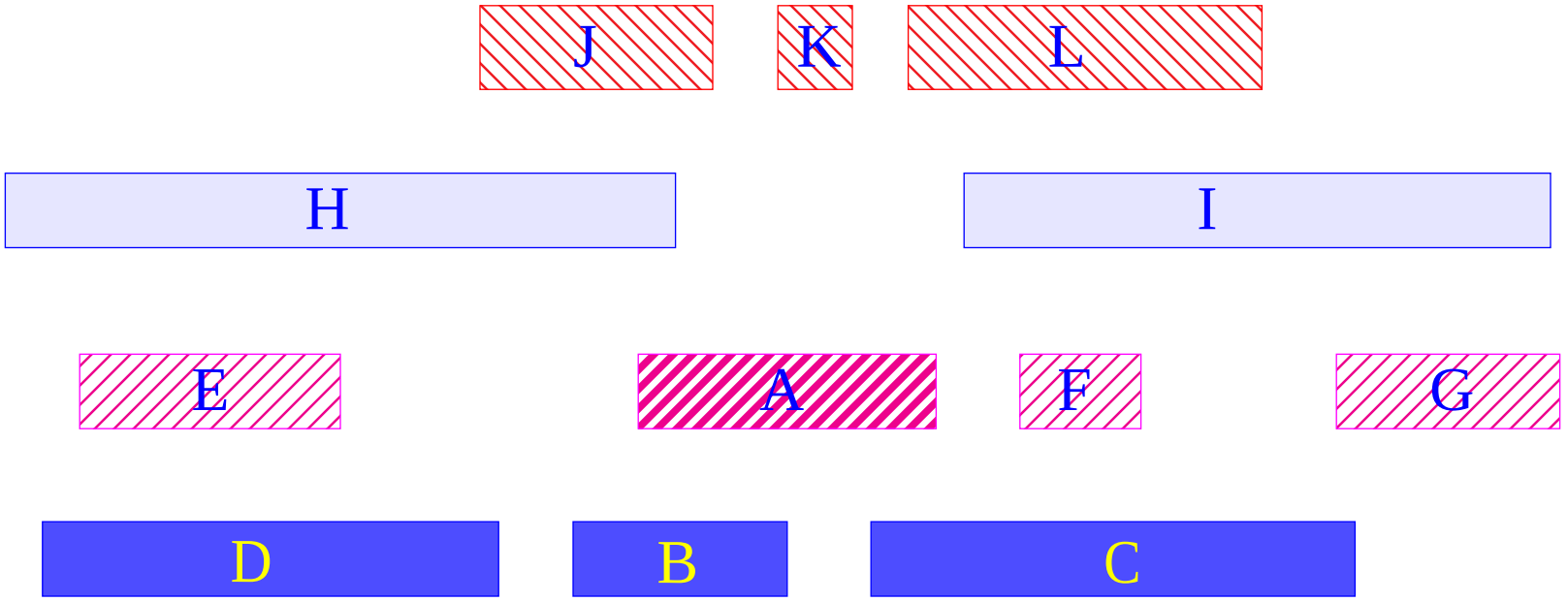


Simple view of the cross-section of a net with its neighbor

- C_a: overlap capacitance due to the overlap of two conductors in different layers
- C_l: lateral capacitance between two conductors in the same plane
- C_f: fringe coupling capacitance between two conductors in different planes.

Capacitance Extraction (cont.)

- In general, the environment for a segment of interest can be quite complicated



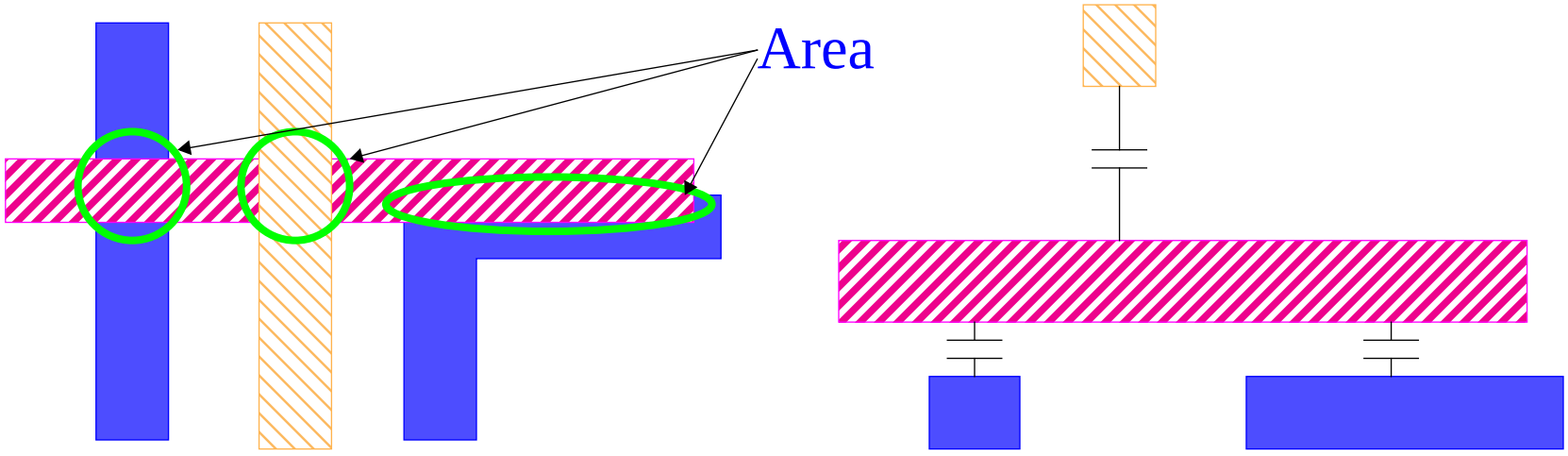
side view

A is the segment of interest
Area capacitance from A to B, C, J, K, L
Fringe capacitance from A to B, D, C, H, I, J, K, L
Lateral capacitance from A to E and F

metal4
metal3
metal2
metal1

Capacitance Extraction - Area Capacitance

- Formed by the surface overlap (in two dimensions) of two conductors in different layers



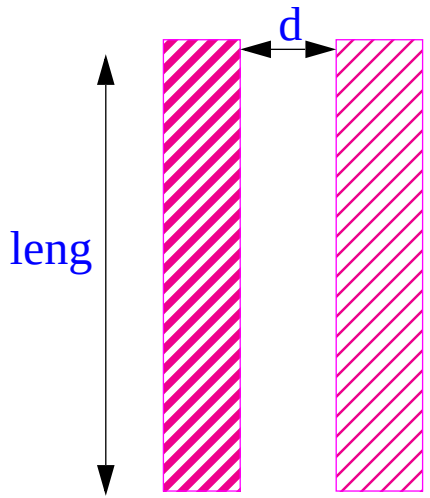
- $C_a = P_{area} * Area$

  where P_{area} is the area capacitance per unit area,

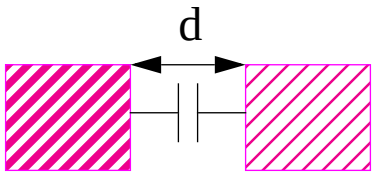
  Area is the overlapping area

Capacitance Extraction - Lateral Capacitance

- Formed by two parallel edges of conductors in the same plane



top view



side view

- $C_l = P_{lat} * leng$

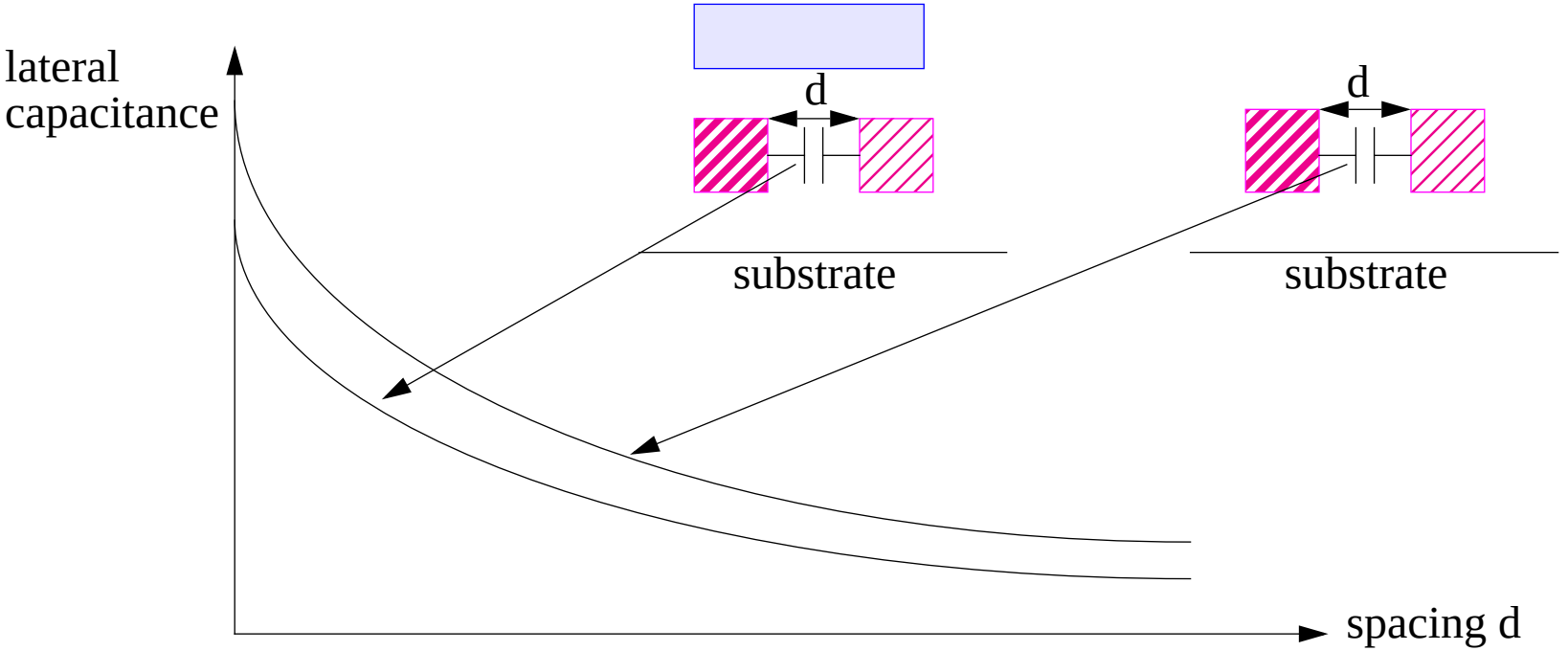
  where P_{lat} is the lateral capacitance per unit length,

  leng is the parallel length

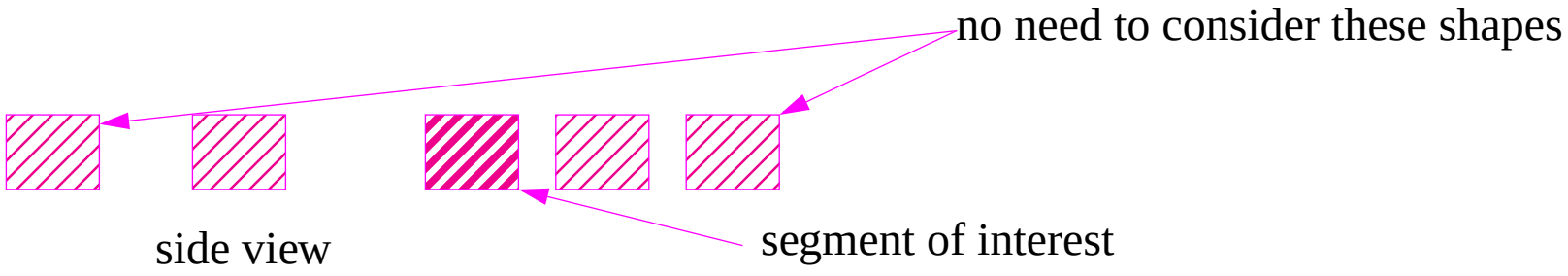
- The metal layers are getting thicker. The lateral capacitance is becoming the most dominating capacitance component, particularly for higher metal layers (e.g. metal3, metal4).

Capacitance Extraction - Lateral Capacitance (cont.)

- The lateral capacitance is reduced by the shielding effects from the layers above and/or below.

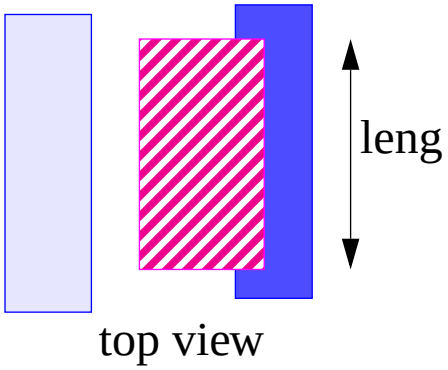


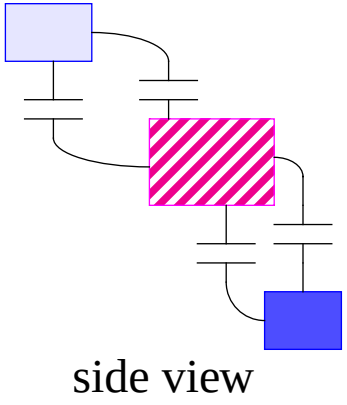
- Typically, only the neighboring shapes are needed



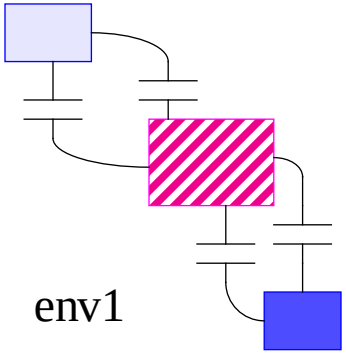
Capacitance Extraction - Fringe Capacitance

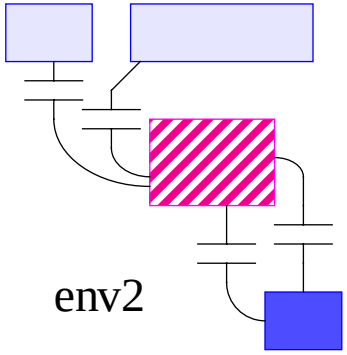
- Formed between the edge of one conductor and the surface of a second conductor above or below.

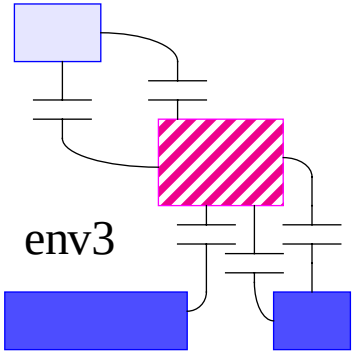




- $C_f = P_{fringe} * leng$
- The fringing capacitance is strongly dependent on the other segments in the environment.







❑ Rule Based Approach - Quick and Dirty

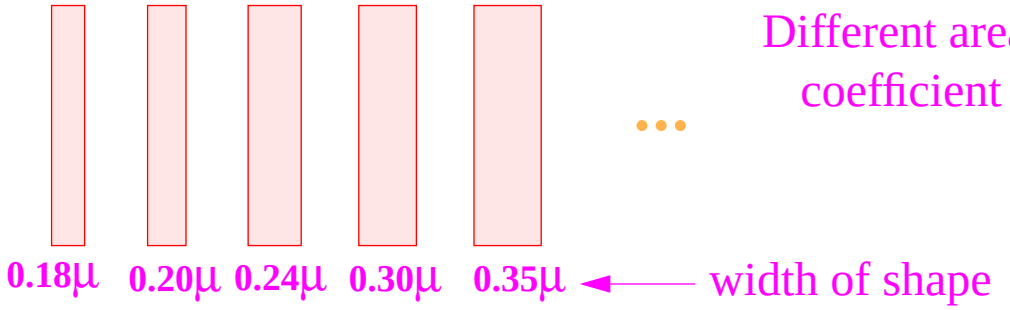
- A quick and dirty way to get capacitance:
  - get the area overlap, multiply by the corresponding area coefficient
  - get the edge length, multiply by the corresponding edge coefficient
  - ignore the lateral capacitance
- This approach is being used in P&R tools, Floorplanning tools and this is very simple and quick
- Limitation:
  - Ignoring of lateral capacitance
  - No accounting of shielding effect
  - Difficulty to obtain convergence on delays due to different extraction results.

❑ Rule Based Approach - Boolean Operations

- Boolean operations (AND, OR, XOR, ...)are applied to the layout. The individual configurations are then identified.
  - This requires boolean operation for each unique geometric configuration.
  - The capacitance is obtained by multiplying the area or length with the corresponding coefficient.
- The coefficient is obtained by using a 3D field solver on each configuration that is identified.
  - The accuracy is strongly dependent on the “expert” to set up the necessary configurations
  - Since a 3D field solver is used in the characterization step, this approach has been claimed to be 3D accurate.

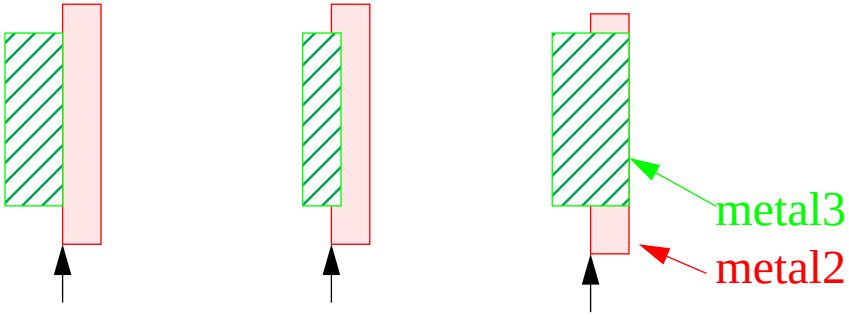
Rule Based Approach - Boolean Operations (cont.)

- Extensive effort is needed to achieve the desired accuracy
  - Due to submicron effects, the area and fringe coefficients are different for each width.
  - There is no interpolation between different configurations.



Different area and fringe capacitance coefficient for each width value

- The fringe capacitance coefficient is also dependent on the other layers

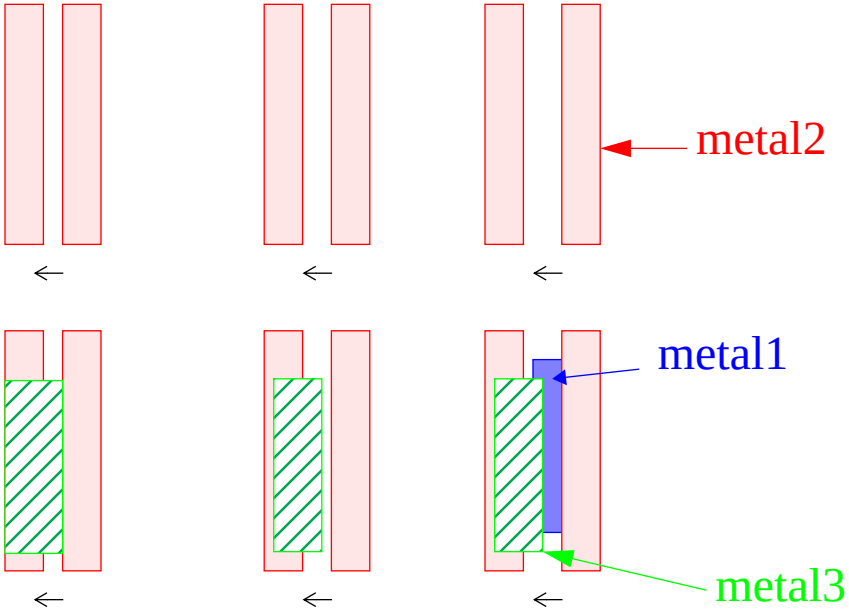


Different coefficient for each environment

Many (too many) combinations for multi-layer process

Rule Based Approach - Boolean Operations (cont.)

- Calculation for lateral capacitance coefficient is very difficult



Very difficult to define configurations for all the different spacings

Only one coefficient per configuration, no dependency on spacing

Very difficult to get adequate accuracy

The configurations and coefficients are different based on the environment

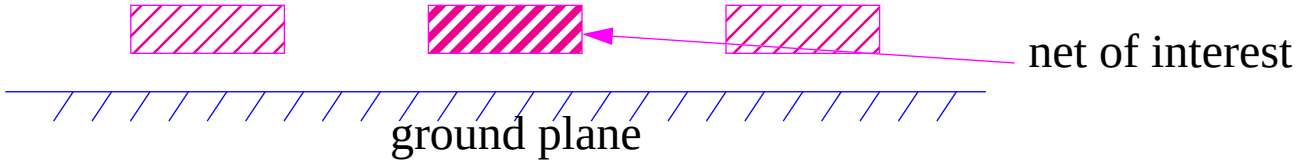
❑ Rule Based Approach - Boolean Operations (cont.)

- Advantages:
  - Supported by all existing layout verification (LPE) tools
  - Once it is set up, extraction is straight forward
- Disadvantages:
  - Requires extensive effort to set up the boolean operations for different configurations
  - Difficult to get required accuracy
  - For a new progress, a new rule file needs to be regenerated

Formula Based Approach - Empirical Equations

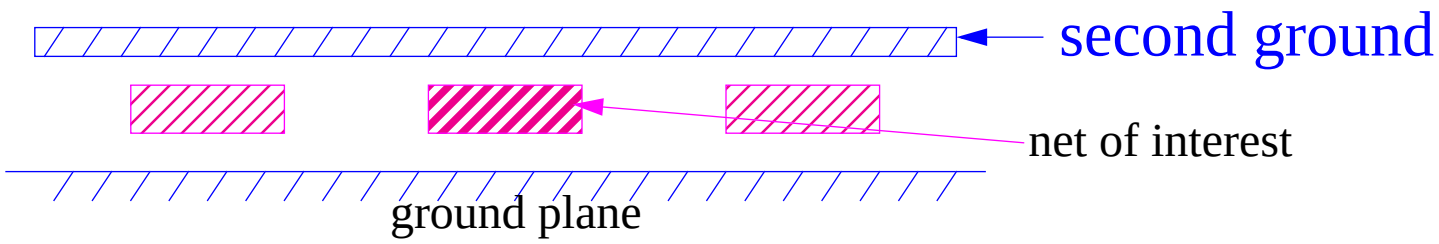
- The total capacitance is calculated based on a multi-term equation with pre-characterized coefficients
- The well known equation is the Sakurai equation:

  T. Sakurai and K. Tamaru, “Simple formulas for two-and three- dimensional capacitances”, IEEE Trans. Devices, vol. ED-30, pp.183-183, 1983 .



- An improved version with two ground planes was published by Liu:

  Yong Liu, “Formulas for Interconnect Capacitance Calculation”, VLSI Multi-level Interconnect Conference, June 1995.



❑ Formula Based Approach - Empirical Equations (cont.)

- Discussion
  - The capacitance calculated is a per unit length capacitance
  - There is an assumption that the conductors are infinitely long
  - This is typically considered to have 2D accuracy
- Advantages
  - The capacitance calculation is very quick
  - The characterization effort is not extensive
- Disadvantages
  - There is limited accuracy
  - Extraction for cross-coupling capacitance can be difficult

Formula Based Approach - Context Based

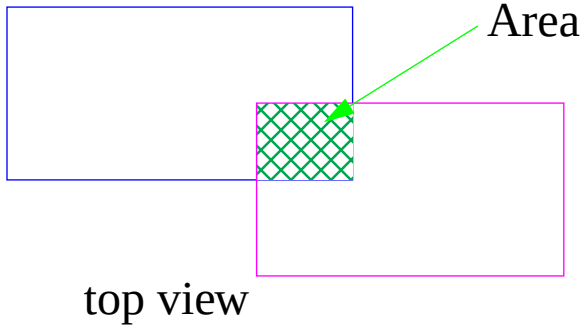
- This approach separates the three capacitance effects and uses a separate formulation for each of the effects

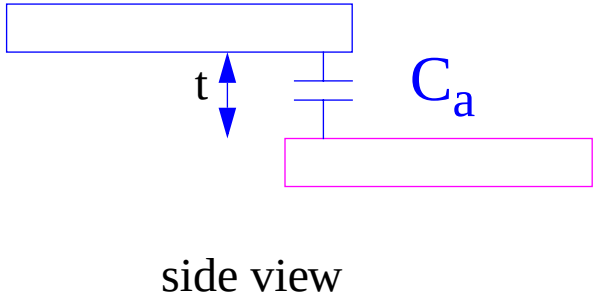
  N. Arora, K. Raol, L. Richardson, “Modeling and Extraction of Interconnect Capacitances for Multilayer VLSI Circuits”, IEEE Trans. Computer-Aided Design, Vol 15, pp.58-67, January 1996.

- The overlap capacitance is calculated with the parallel plate

$$\text{equation: } C_a = \frac{\varepsilon_0 \varepsilon_r}{t} \cdot Area$$

  - Area is the overlapping area
  - t is the thickness of the dielectric between the layers



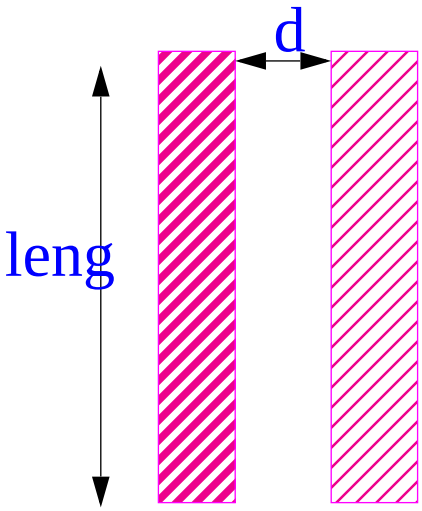


❑ Formula Based Approach - Context Based (cont.)

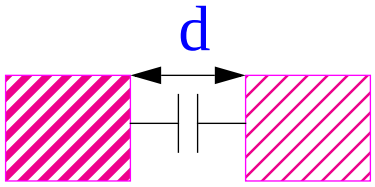
- The lateral capacitance is calculated

$$\text{by}C_l = \left(C_0 + \frac{C_1}{d} + \frac{C_2}{d^2} + \frac{C_3}{d^3} + \frac{C_4}{d^4} \right) \cdot \text{leng}$$

  - C_0, C_1, C_2, C_3, C_4 are constants after curve fitting to results from 2-D simulated lateral capacitance data



top view



side view

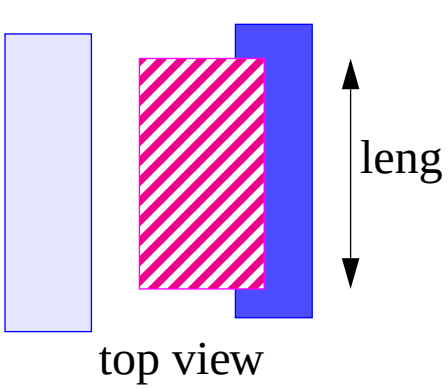
- There will be a separate set of constants for each vertical profile and will be retrieved through table look-up.

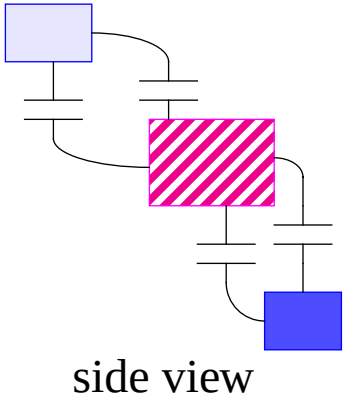
Formula Based Approach - Context Based (cont.)

- The fringe capacitance is calculated by

$$C_f = F \cdot A_e$$

  - F is the fringing model coefficient
  - A_e is the effective area for the surface of the conductor





- The Fringing model coefficient is based on each of the vertical profiles and will be retrieved through table look-up.

❑ Formula Based Approach - Context Based (cont.)

- Discussion
  - This approach uses a combination of equation calculation with table look-up
  - This is considered to have 2 1/2D accuracy
- Advantages
  - Good accuracy can be obtained with a well characterized table
  - The program will automatically identify the appropriate vertical profile
- Disadvantages
  - The characterization effort can be extensive and will require in-depth knowledge of the implementation
  - The accuracy of the result will have strong dependency on the characterization effort
  - Orthogonal 3D effect is not accounted for

Table Based Approach - Quasi-3D

- The Quasi-3D approach separates the layout into two orthogonal cross-sectional views
- In the following figure, the blue conductor is the interconnect of interest while the other conductors (green and magenta) form the environment.
- The A-A’ provides the cross-section x-view while the B-B’ and C-C’ provide two of the cross-section y-views.

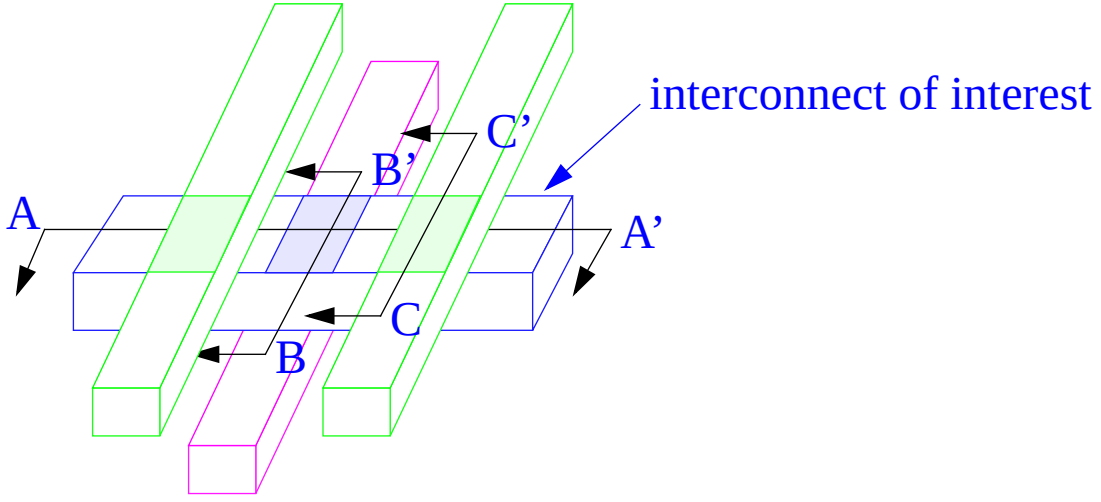
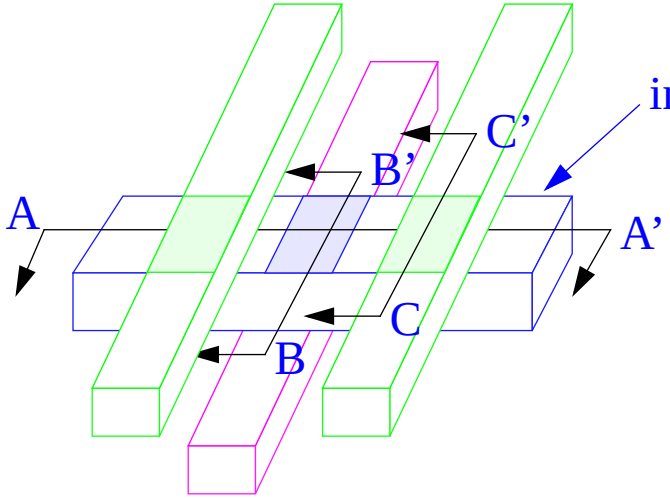
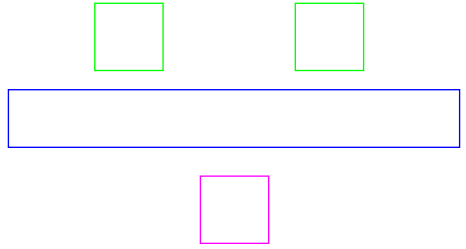


Table Based Approach - Quasi-3D (cont.)

- The A-A’ cross-sectional view is shown below. The capacitance value per unit length is obtained from the library.



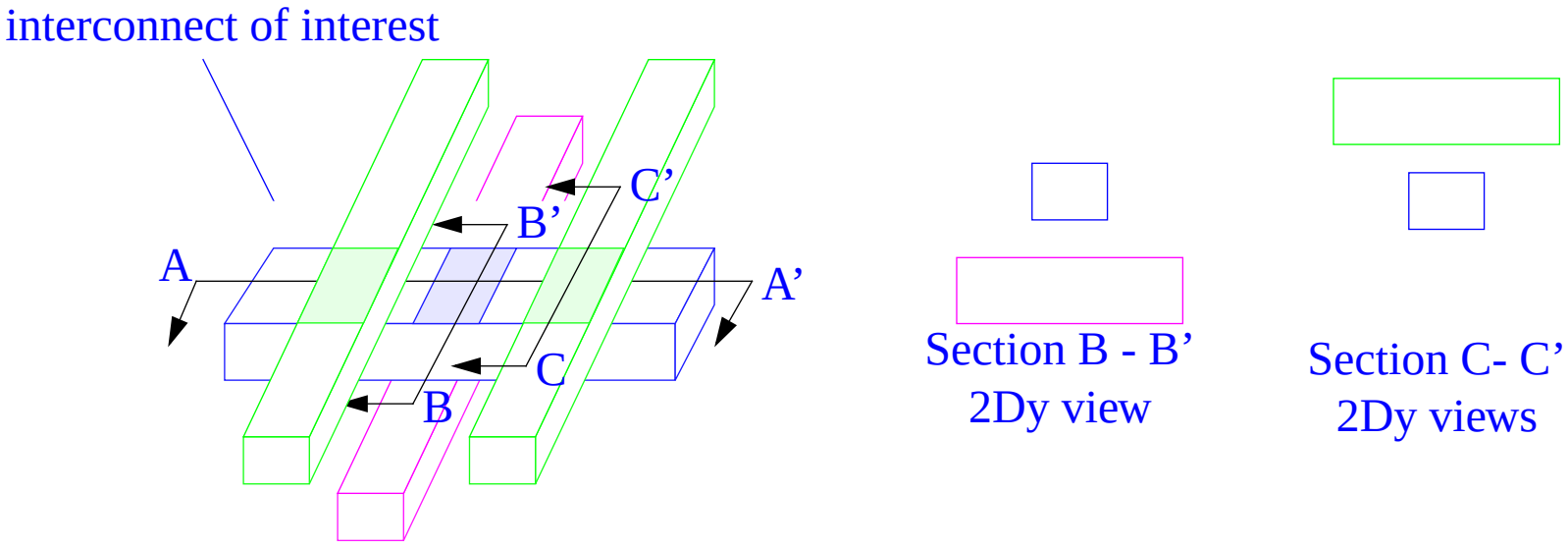


Section A - A’
2Dx view

- The capacitance value in the library was obtained by a 2D field solver. The area, fringe and lateral effects are obtained at the same time. This provide high accuracy for submicron structures.
- The capacitance from the x-view is obtained by multiplying the length for the A-A’ view.

❑ Table Based Approach - Quasi-3D (cont.)

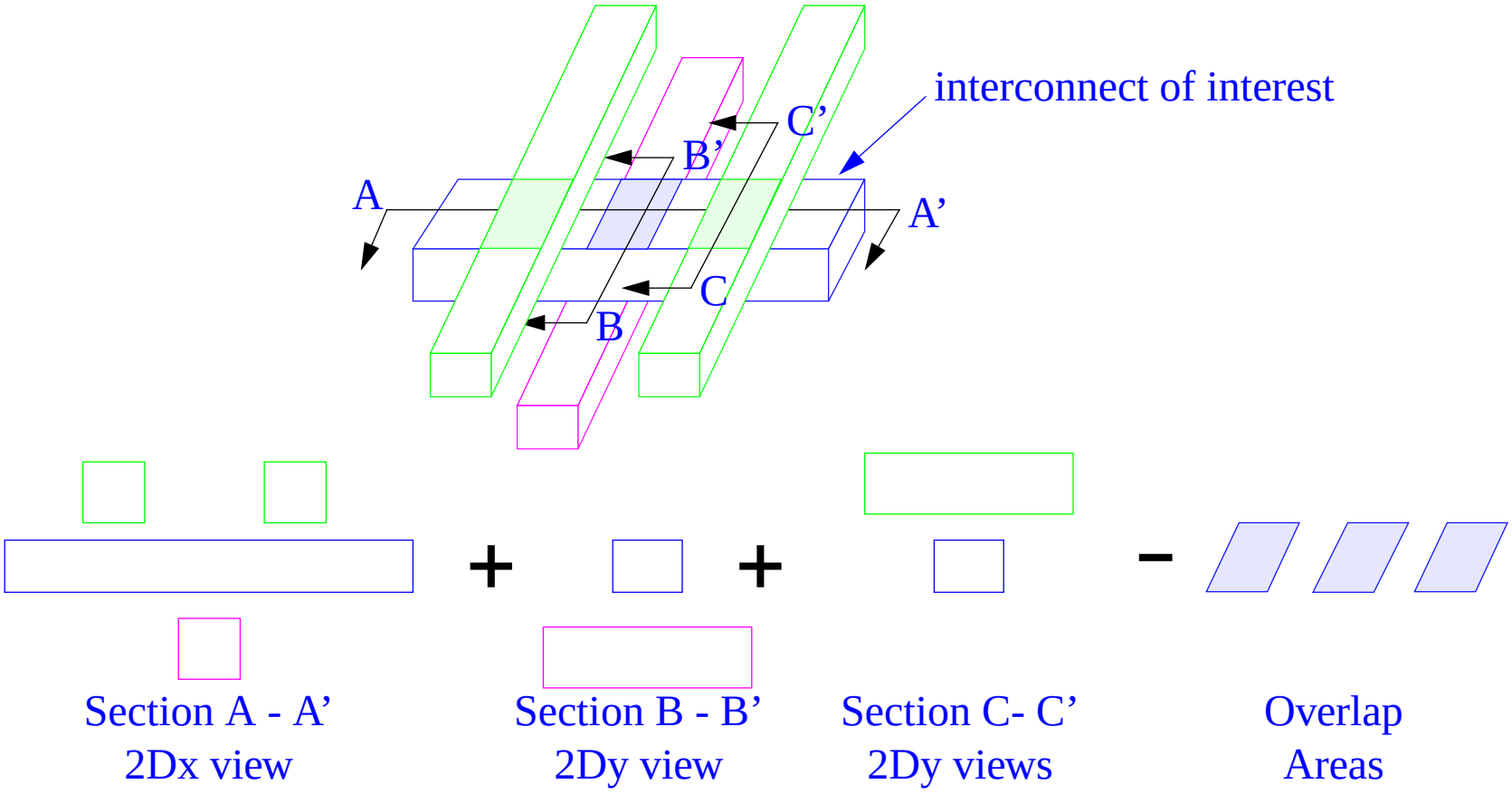
- There are several environments in the y cross-section views, two of them are B-B' and C-C'.
- The capacitance from each of the views is retrieved from the library and then multiplied by the corresponding length



- Since the "shaded" areas are covered by both x cross-section view and y cross-section view, the capacitance is counted twice. That will be substrated from the result.

Table Based Approach - Quasi-3D (cont.)

- The Quasi-3D includes area, fringe, lateral and shielding effects without need to calculate each independently.



❑ Table Based Approach - Quasi-3D (cont.)

- Discussion
  - Table look-up approach is used.
  - Interpolation is used for the views which do not match those in the library.
  - This is considered to have 2 1/2D accuracy
- Advantages
  - Good accuracy is obtained with very fast speed.
  - The library generation is automatic once the process parameters is defined.
  - The program will automatically identify the appropriate vertical profile
- Disadvantages
  - Orthogonal 3D effect is not accounted for
  - No ability by the user to adjust the results

Table Based Approach - 3D

- A typical library for a process with 3 layers of metal contains tens of thousands of entries.
- The interconnect is decomposed into the primitives to match with the patterns in the library.
- A 3D field solver is called for non-matched patterns.
- RC network is built from the electrical description of the primitives
- Advantages
  - 3D accuracy
- Disadvantages
  - Library building effort is huge
  - Difficult to develop “complete” patterns
  - Performance can be slow for a real design
  - Not proven

Field Solvers

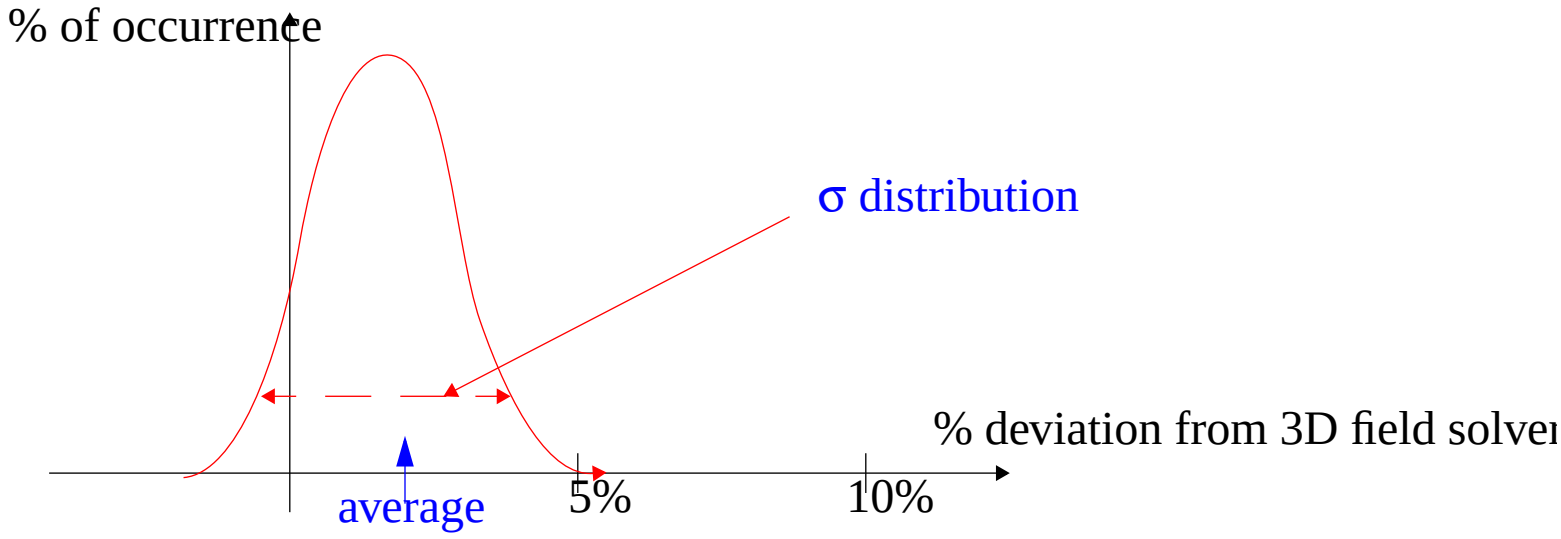
- Several field solvers are available in the market
  - finite difference method: Raphael from TMA
  - finite element method: Maxwell from Ansoft, Metal from OEA International
  - boundary element method: Arcadia from Synopsys, Fastcap from MIT, Fasthenry from MTI, UA3D from U of Arizona, SAP from U of Vienna
  - Monte Carlo: QuickCap (using Random Walk) from Random Logic
- Field solvers are mainly used to characterize the library
- Due to the slow speed, it is not practical to use field solvers to perform extraction.
- Field solver can be combined with table approach to provide acceptable performance.

Accuracy Comparison

- There are many claims to accuracy based on the approach, Quasi-3D, 3D-like, true 3D, etc
- All implementations contain a trade-off of accuracy for higher performance.
- Accuracy comparison should be based on real patterns coming from actual design. The patterns should not include those used in characterizing the library.
- The average difference from 3D field solver is a good measure.

Accuracy Comparison (cont.)

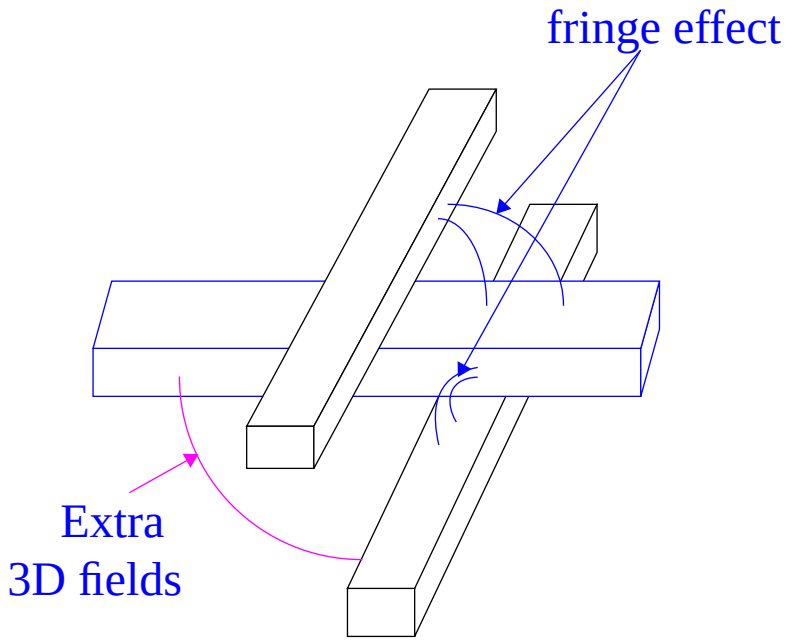
- The standard derivation of the difference from a 3D field solver would be a better measure.



- Comparison of the simulated timing by a circuit simulator with silicon on timing is the only meaningful metric.
- Services for generating the parameters for library characterization from wafers and for silicon comparison are available.

❑ 3D Effects

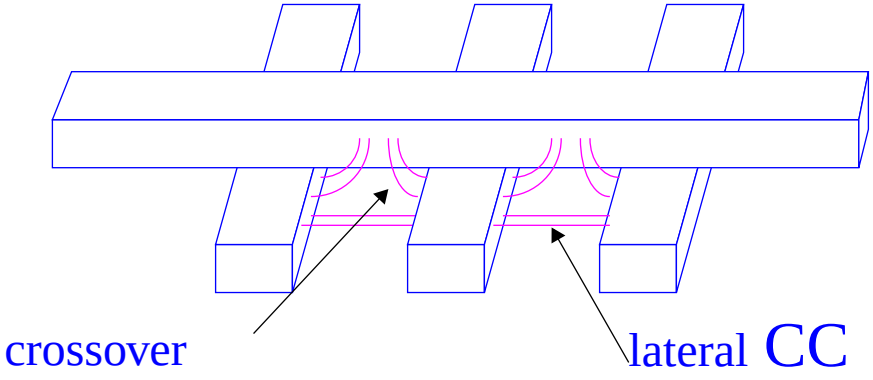
- Some 3D fields are not included in the equation or Quasi-3D approach



- The origin of the extra 3D effect is from the sides of the interconnects which are orthogonal to each other.

3D Effects (cont.)

- The Extra 3D fields have weak effect on total capacitance



- 3D effect is weaker when spacing is minimal

- Extra 3D effect increases with thickness > width
- Extra 3D effect influences cross-coupling cap (CC) of individual segments
- Extra 3D effect is weakest when spacing is minimal.
- Accuracy can be improved by applying 3D correction.