Interconnect Extraction and Analysis in High-Frequency, Sub-Micron, Digital VLSI Design

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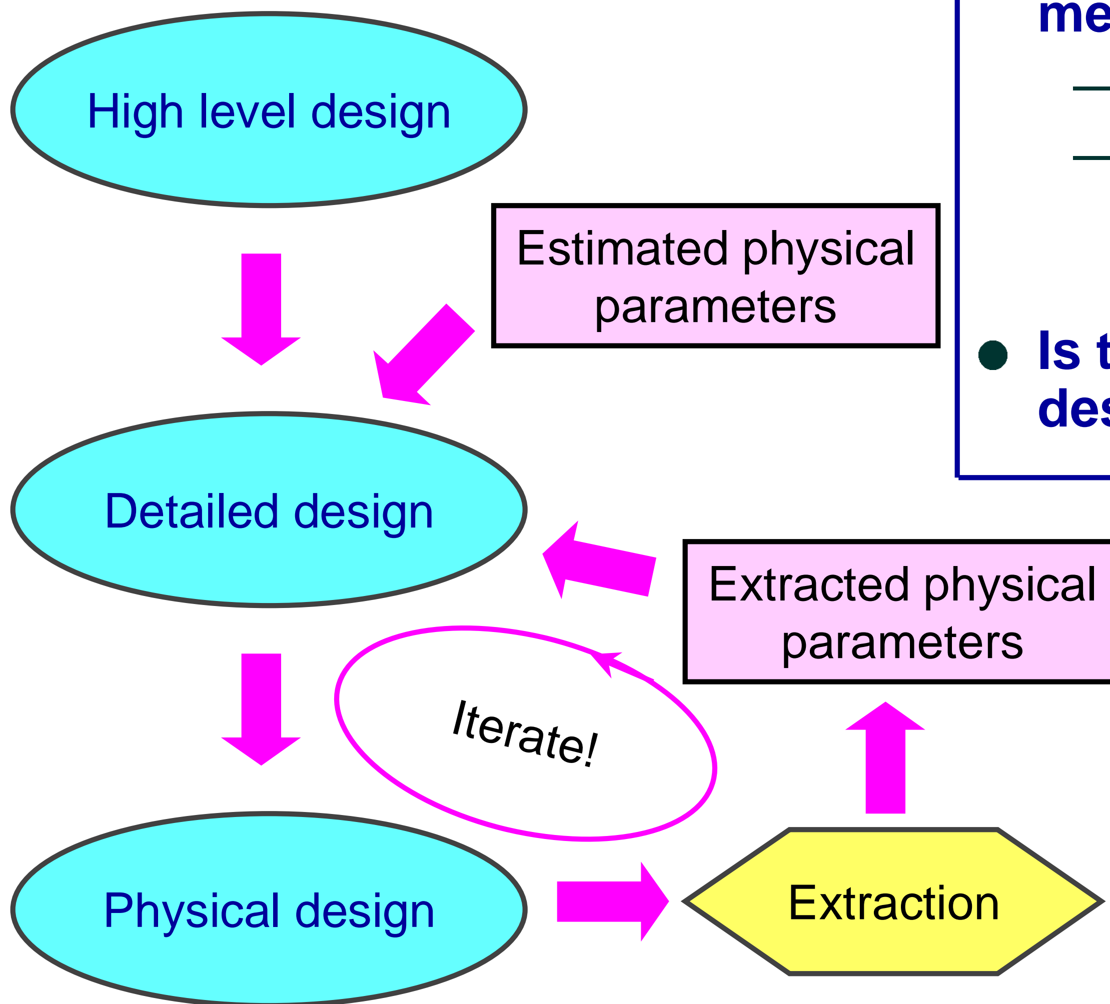
General outline

- Technology trends
- Practical RC extraction techniques
- Fundamental extraction algorithms
- Linear Model Reduction Techniques
- Role of extraction in the VLSI design flow
- Conclusion and outlook

VLSI design methodology



- **Traditional design methodology**
  - **functionality first**
  - **interconnect considered "parasitics"**
- **Is this still the right way to design?**

VLSI interconnect trends

- **Scaling Trends**
  - smaller feature size
  - increase of chip size
  - affected physical parameters
    - decrease of metal width/spacing
    - decrease of dielectric thickness
    - decrease of metal thickness
    - increase of interconnect length
  - increase in operating frequency
  - increase in chip complexity
- **Impact on Electrical Parameters**
  - capacitance
    - increase of total capacitance
    - coupling increasingly dominant
  - increase of interconnect resistance
  - inductance effects felt at chip-level

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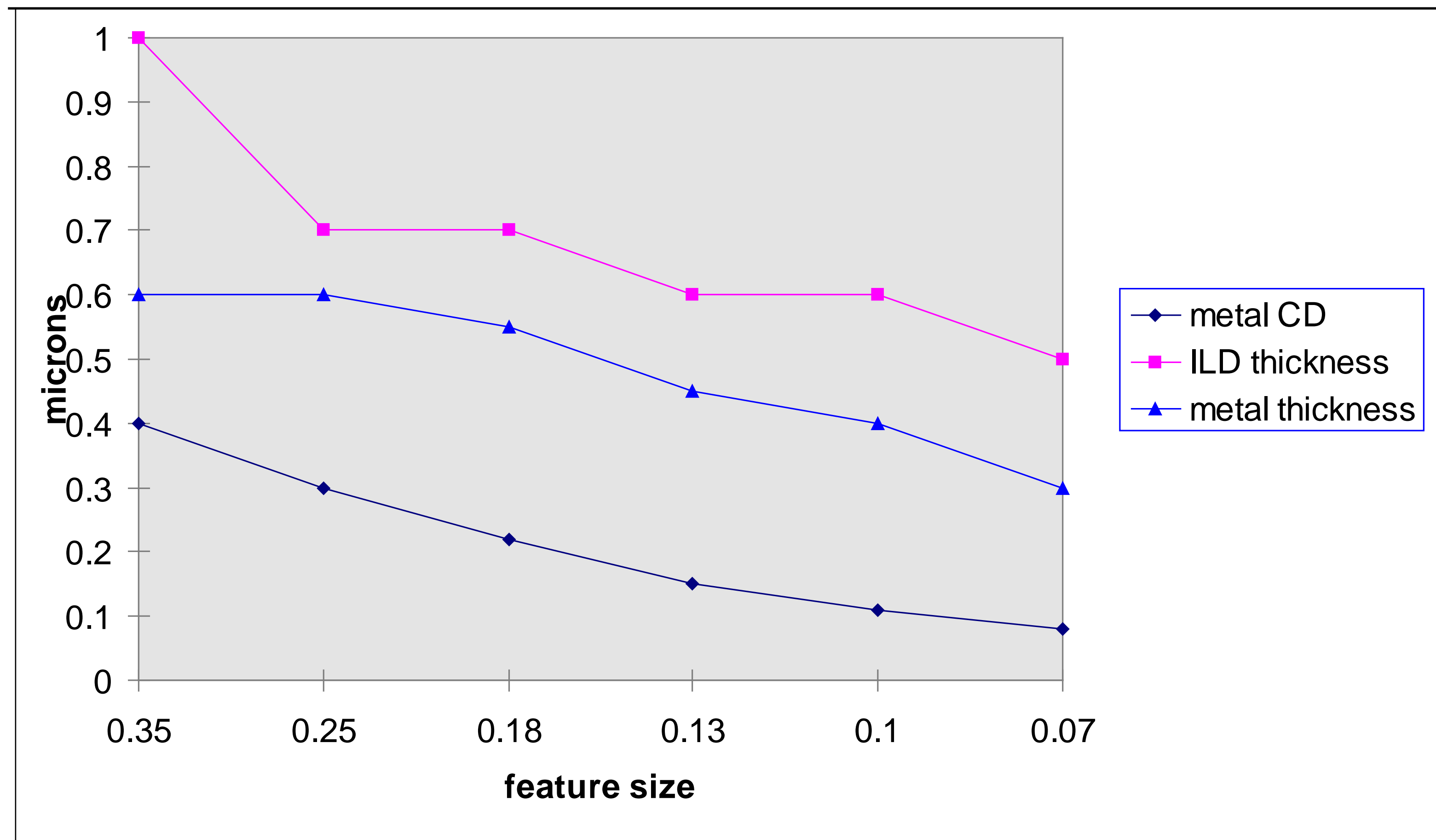
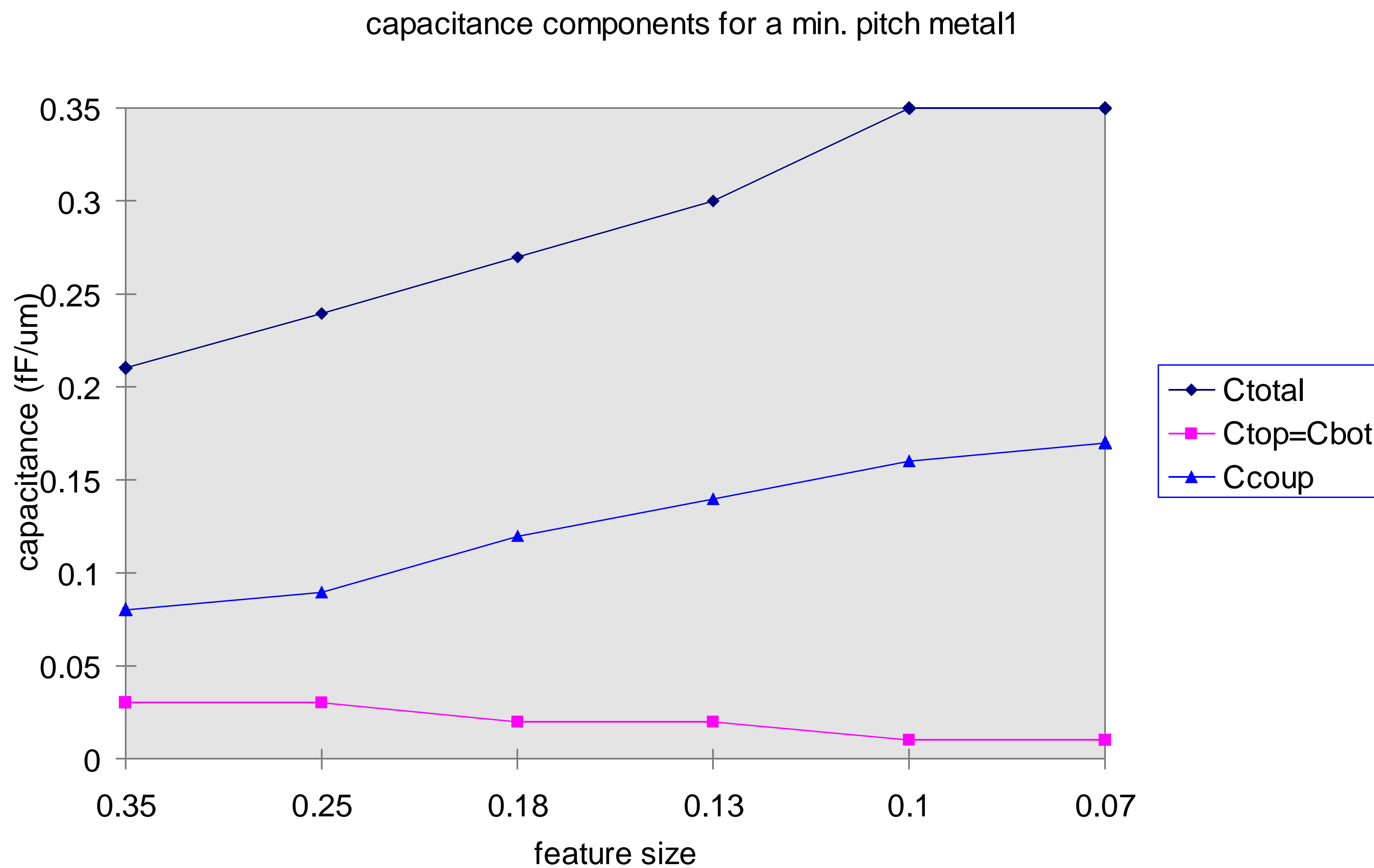
Metal interconect scaling

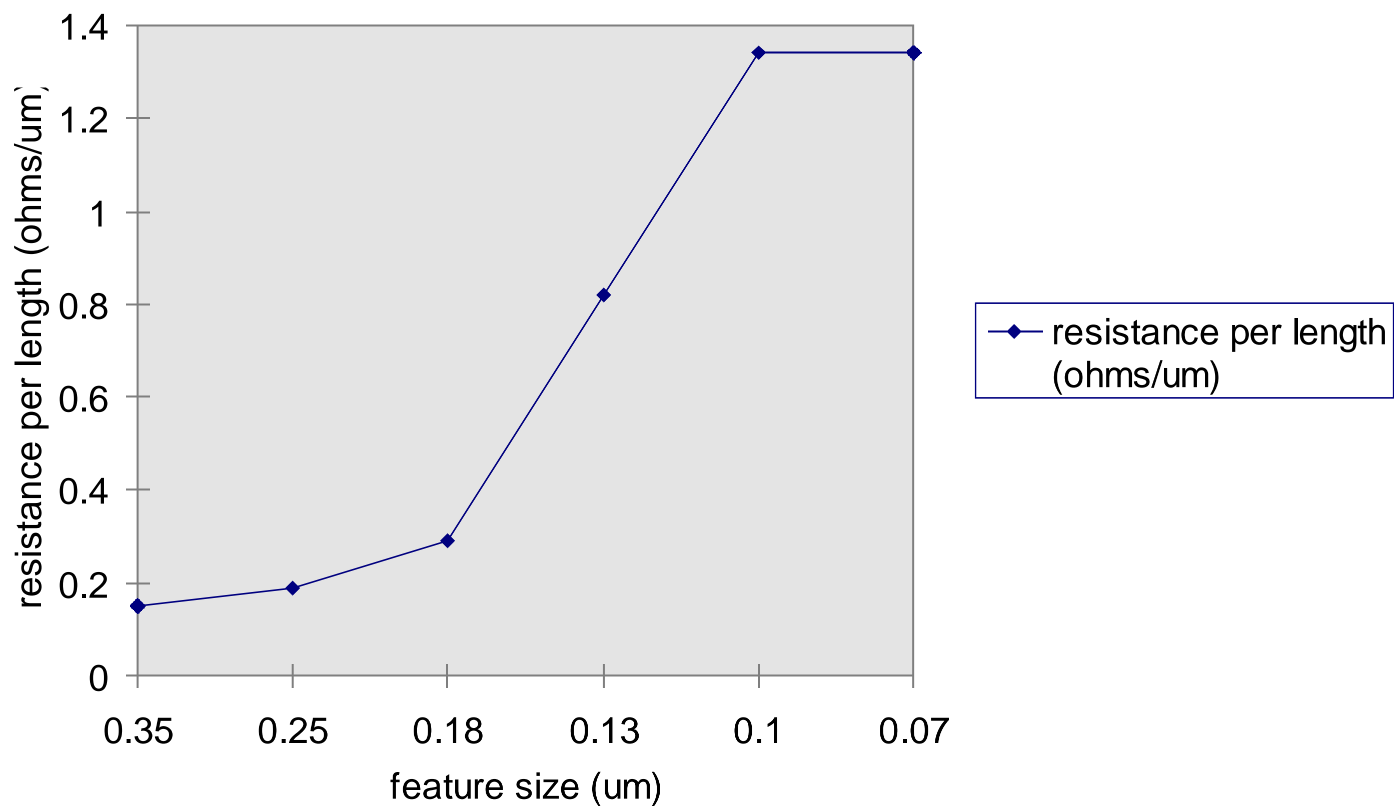


CD: critical dimension **ILD: interlayer dielectric**

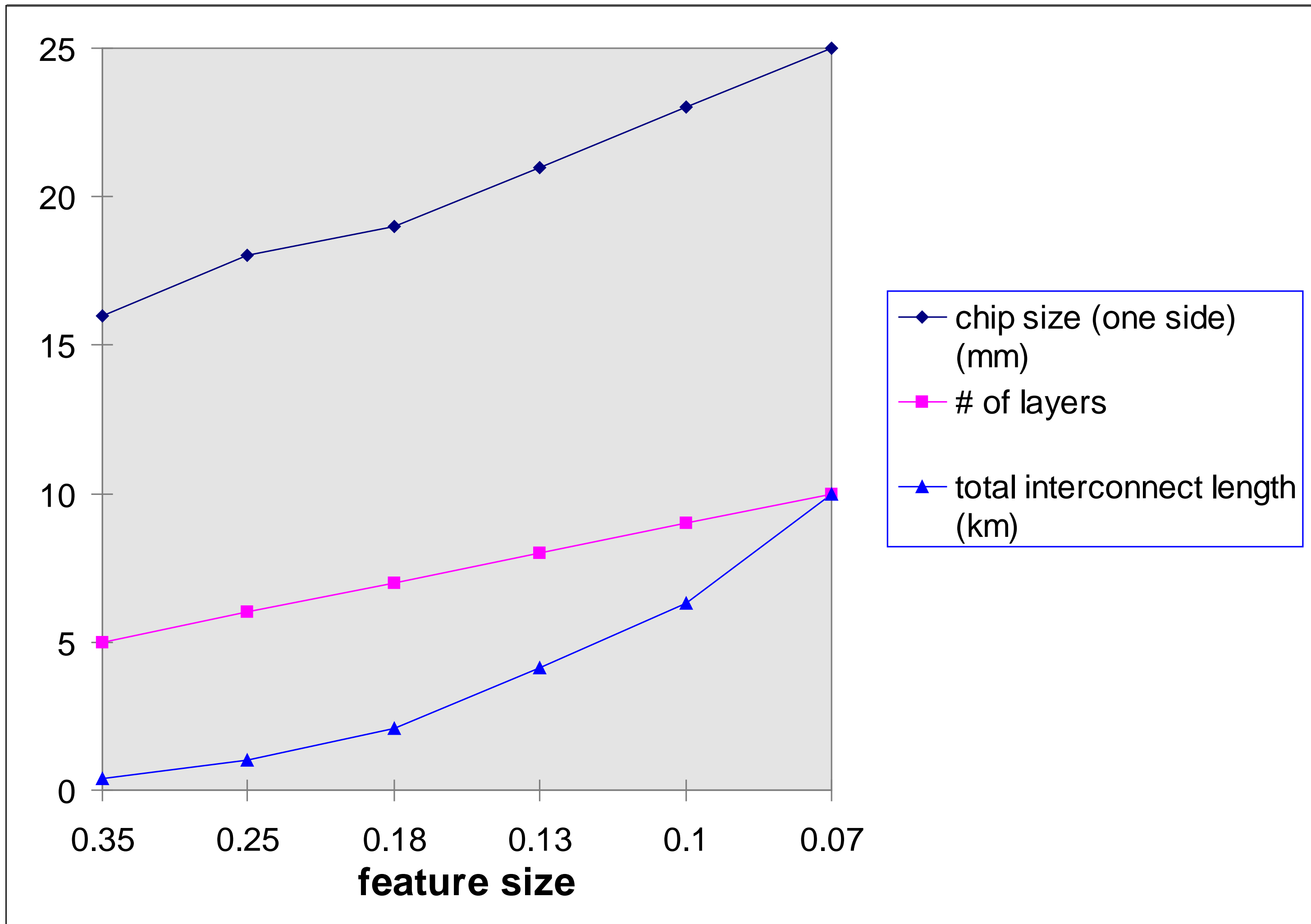
Capacitance scaling



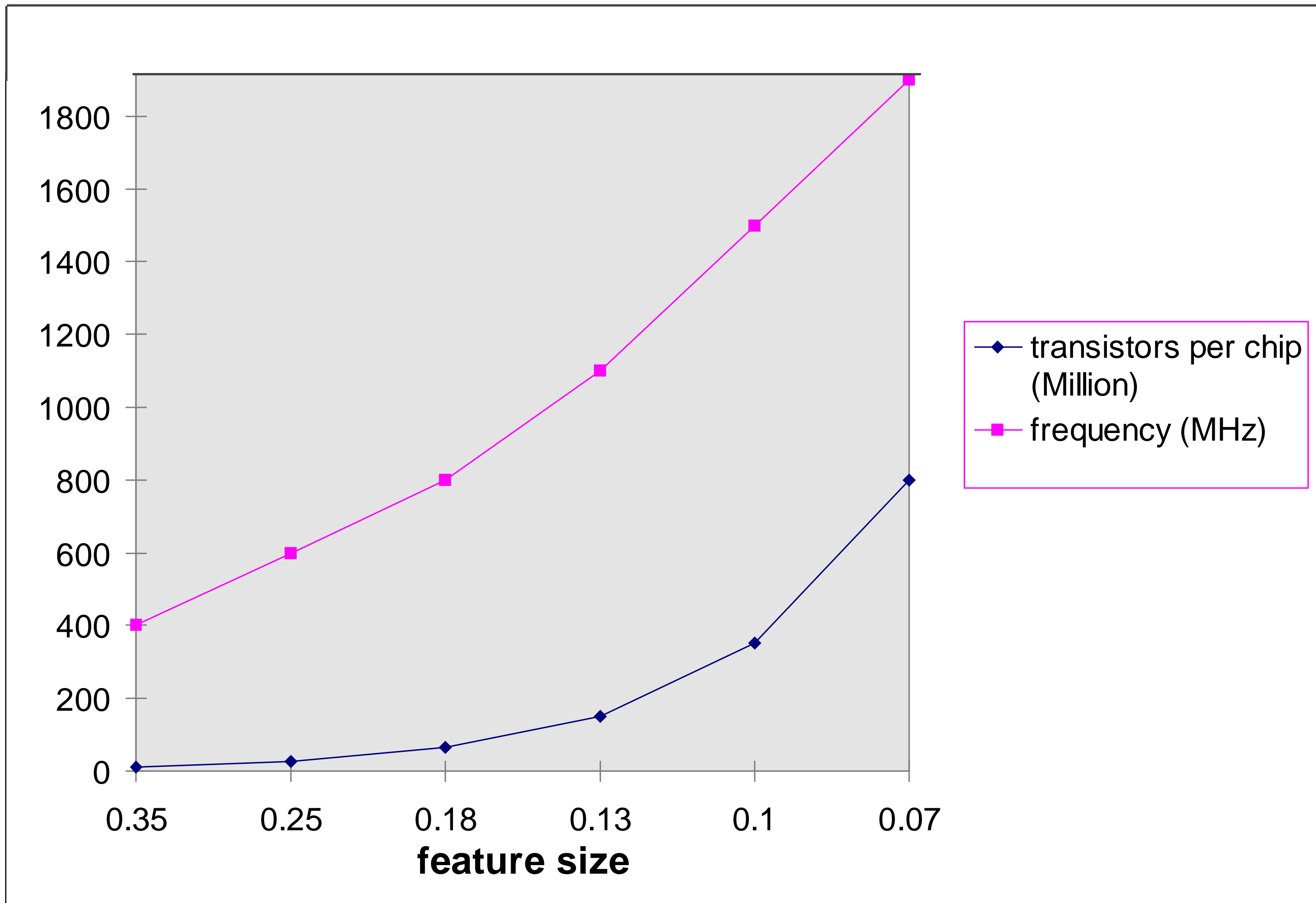
Resistance scaling



Chip evolution



Chip speed and complexity



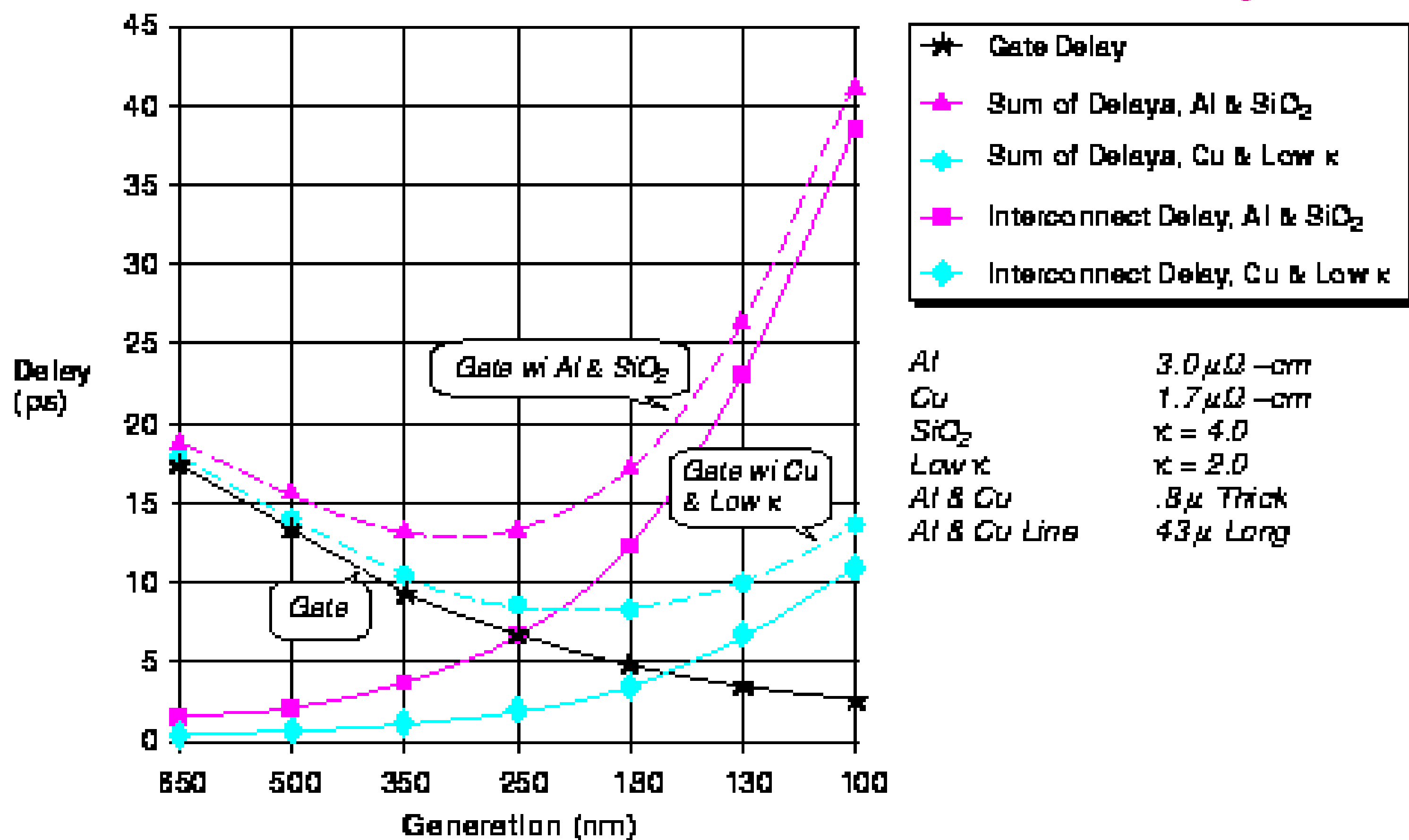
Technology Solutions

- **Process Technology Solutions**
  - — increase in # of layers => shorter interconnect
  - — Higher conductivity => lower resistance $R \propto \frac{1}{\sigma}$
    Copper
  - — Low dielectric constant => low capacitance $C \propto \varepsilon$
    Low-K materials (e.g., polyimide)
  - — planarization

Impact of interconnect on design

- Signal Delay
  - — Impact of wire capacitance, resistance, and length
  - — Impact of adjacent signals through cross-talk
- Signal Integrity
  - — False switching due to cross-talk
- Reliability
  - — Increasing current drive may cause electromigration
  - — Cross-talk may induce signal levels outside supply levels

Gate vs. interconnect delay



- **Despite everything interconnect effects dominate!**

Wirelength distribution