HPEMS / Xyce™

High Performance Electrical Modeling & Simulation at Sandia National Laboratories

http://csmr.ca.sandia.gov/workshops/nacdm2002/

3 April 2002

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Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000.

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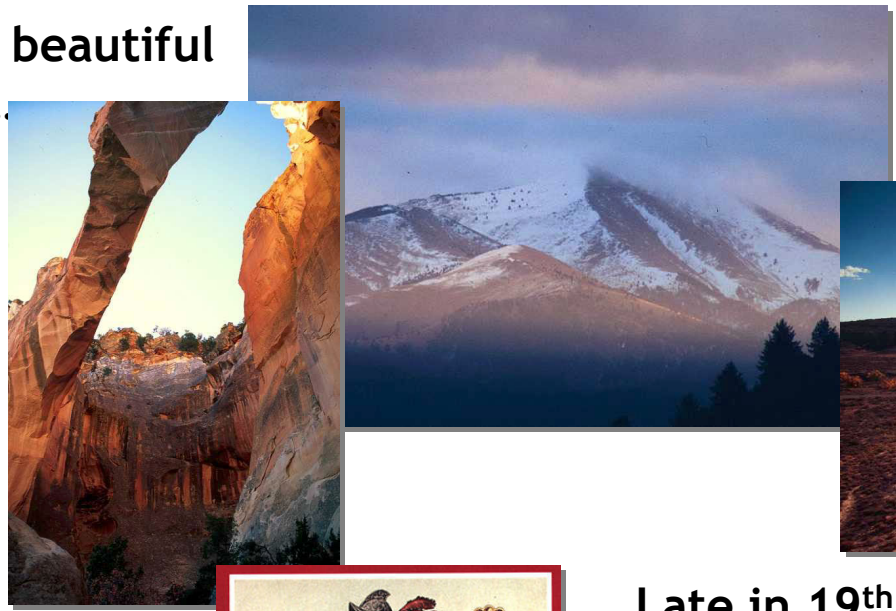
Talk Outline

- Workshop
  - Welcome
  - Goals
  - Background
- Sandia's HPEMS Program
  - High Performance Computing at Sandia
  - Design Process
  - HPEMS Integrated Road Map
  - Xyce Parallel Electronic Simulator
  - Preliminary Solver Results
  - Status
  - Challenges / Future Work
- Summary

Welcome to New Mexico - Hundreds of Years of Tradition

Initially, just beautiful landscapes..



Then the Anasazi - nearly 1000 years ago…

In 1598, first New Mexico colonial capital established by Don Juan de Onate…

Late in 19th century, the railroad and Anglos arrive…

Later, Other Art and Life Forms Arrived…

Photograph courtesy Philip Greenspun, http://photo.net/philg/

NACDM 2002, April 3-5, 2002, Santa Fe, NM

NACDM 2002 Workshop Goals

- ***Collaborations…***
  - Foster and strengthen collaborations between Sandia and leaders in circuit and device modeling and numerical analysis
- ***Information…***
  - Exchange information on the state-of-the-art methods for linear systems, nonlinear equations, ODE/DAEs and PDEs as applied to circuit and device simulation
- ***Challenges…***
  - Assess barriers and challenges to creating a scalable parallel circuit simulator and identify promising algorithmic and software approaches for overcoming these barriers

Background – Why a Workshop?

- Sandia has little or no history of developing circuit and device simulation codes
  - Few connections with academia or industry
- Sandia *does have* a long history of developing high-performance continuum mechanics codes
  - Leaders in large-scale parallel computing (algorithms, application codes, OS)
- Algorithms research, as applied to circuit simulation, doesn't appear very active, at least in academic circles
  - Is this an issue?

Discussion Topics

- ***How To Make Numerical Codes More Robust and Easier to Use***

  Wednesday – 12:30 PM

- ***The Utility of Iterative Linear Solvers and Other Numerical Methods for Circuit and Device Modeling***

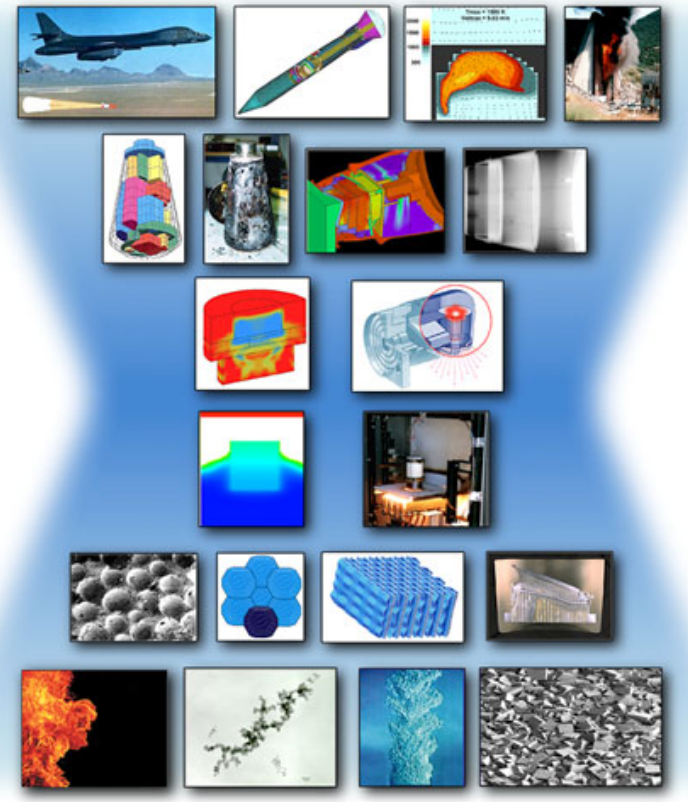
  Thursday – 4:00 PM

- ***The Next Generation of Transistor-Level Circuit Simulation***

  Friday – 11:30 AM

High Performance Computing at Sandia

- Full System
- Subassembly
- Components
- Continuum
- Sub-grid
- Separable effects



- Structural dynamics
- Thermal
- Solid mechanics
- Computational fluid dynamics
- *Electrical*
- Shock Physics
- Fire
- Geophysics

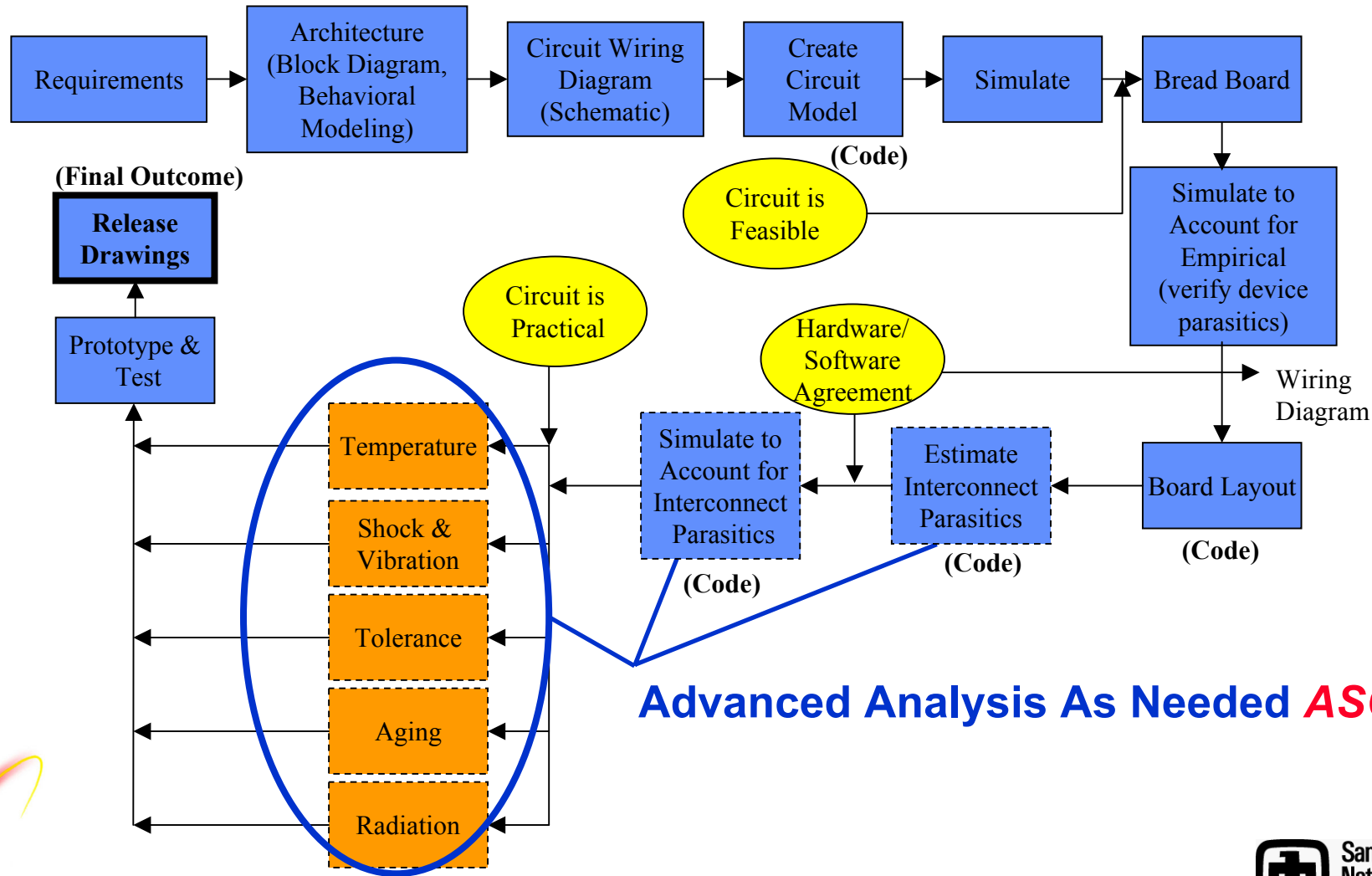
High Performance Algorithms at Sandia
(Partial List)

- **Solvers and Numerical Algorithms**
  - Trilinos (Epetra, AztecOO, TSF, NOX)
  - ML - Multi-level preconditioning
  - LOCA - Library of Continuation Algorithms
- **DAKOTA - Large-scale Engineering Optimization and Uncertainty Analysis**
- **Zoltan & Chaco - Partitioning and load-balancing toolkit**
- **CUBIT Mesh Generation Tool Suite**
  - Unstructured Hex, Tet, Quad, and Tri Meshing
  - Solid model geometry preparation

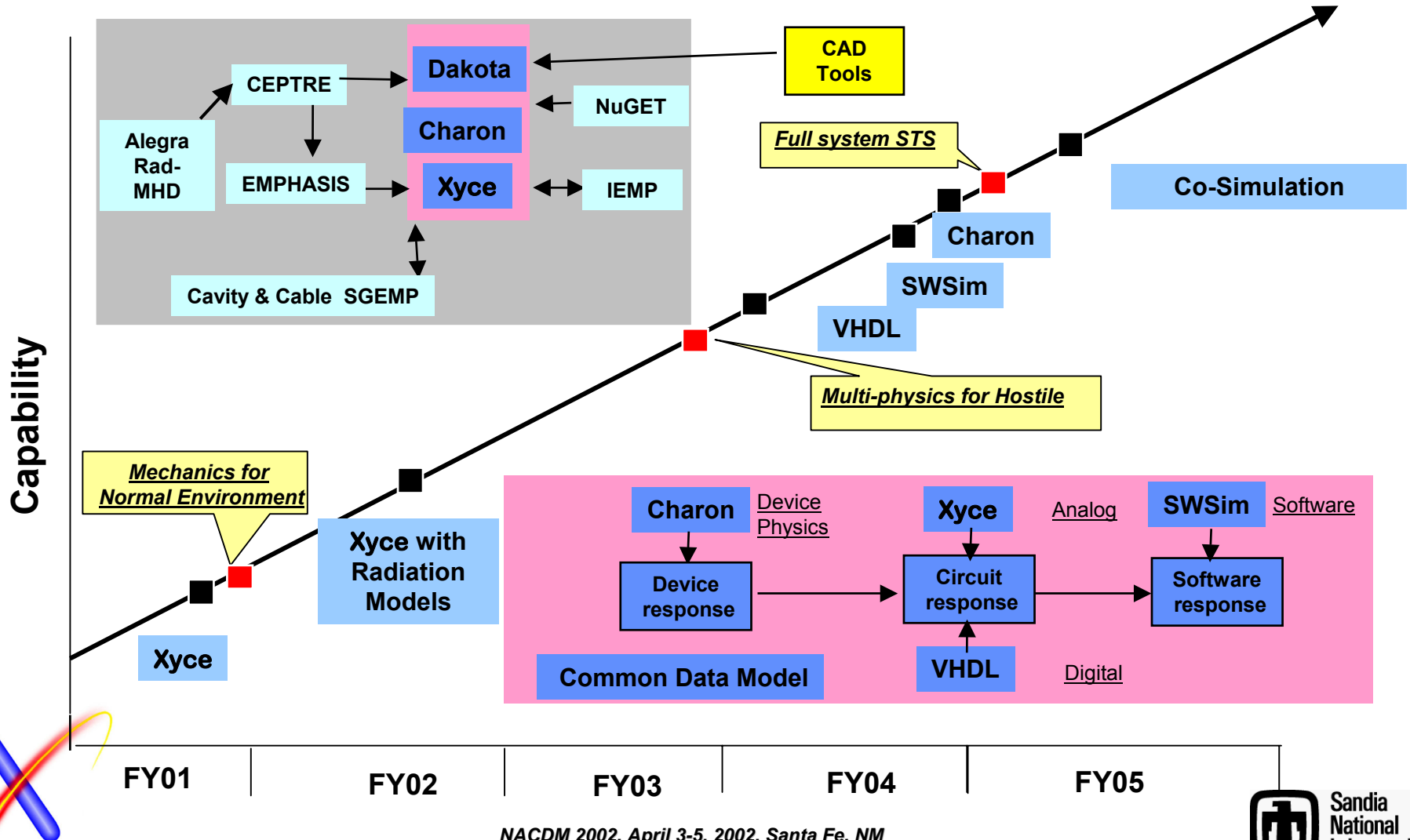
Sandia's High Performance Electrical Modeling and Simulation (HPEMS) Program

- Begun in 1996 under DOE ASCI program
- Focused initially on high-performance transient analog simulation
  - Parallel computing support
  - Radiation and age-aware device models
  - Two parallel codes:
    - Initial, short-term solution, shared-memory Berkeley SPICE-based *ChileSPICE*
    - Long-term solution - distributed-memory, object-oriented **Xyce**
- Enhanced Avant! DaVinci (dynamic memory support)
- Charon distributed-memory Device Modeling Code – under development
- Device/analog modeling, Mixed-signal Modeling
- Design optimization and sensitivity analysis (DAKOTA)

Sandia Electrical Circuit Design Process



HPEMS Integrated Roadmap



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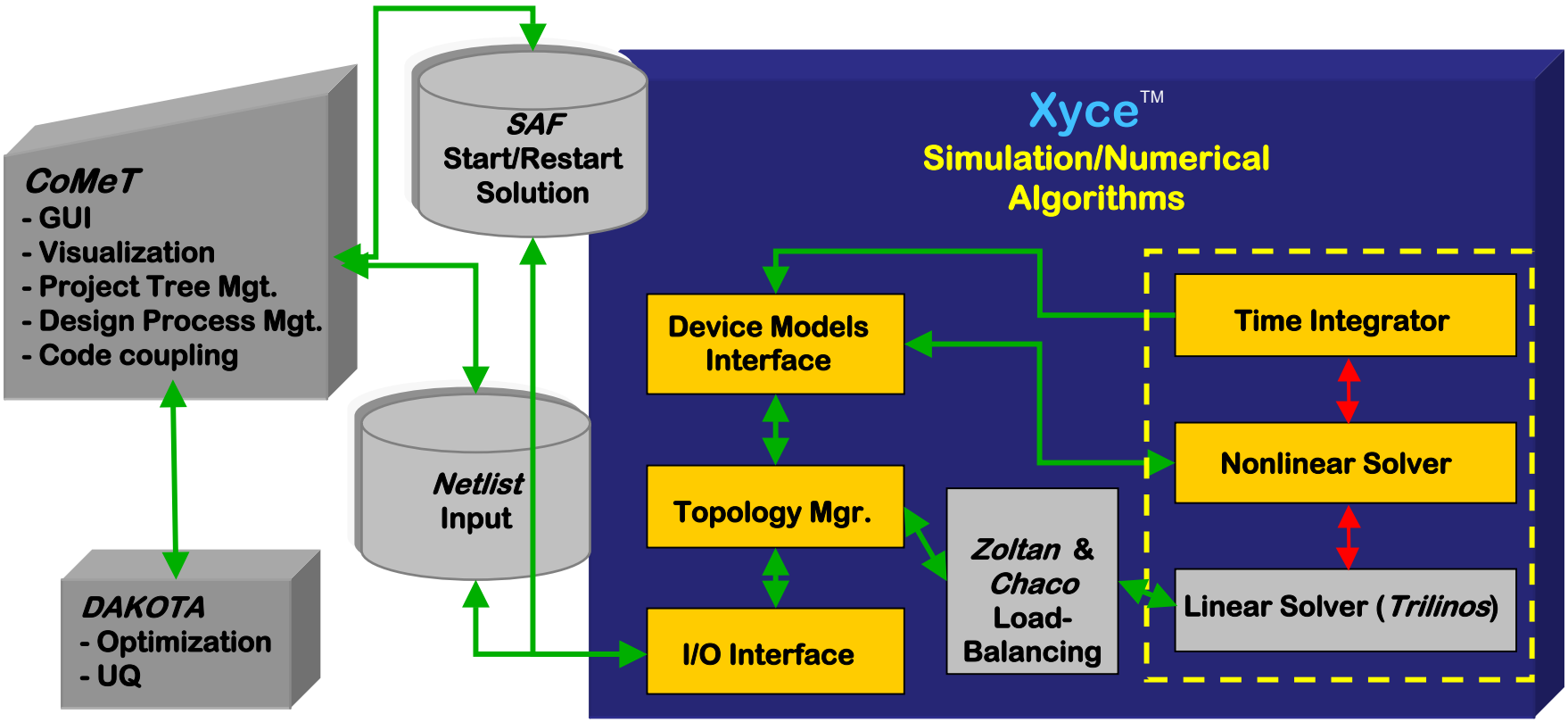
Xyce™ Kernel & Libraries



Xyce™ Novel Approaches (We think…)

- Object-oriented software design
- Distributed-memory parallel
  - Dynamic parallel partitioning and load balance of heterogeneous problems
  - Distributed sources
- "Standard" Newton solve – i.e., solve for update
  - More appropriate scaling for iterative solvers
- Experimented with a variety of nonlinear strategies:
  - Inexact-Newton methods, line-searches, modified Newton, gradient searches, etc.
- Focus on preconditioned Krylov iterative linear solvers
  - Primarily non-restarted GMRES
  - ILUT (dual threshold) preconditioners with overlapping
  - Diagonal shifting, adaptive strategies (Mike Heroux)
  - Reordering methods (RCM, Duff-Koster)

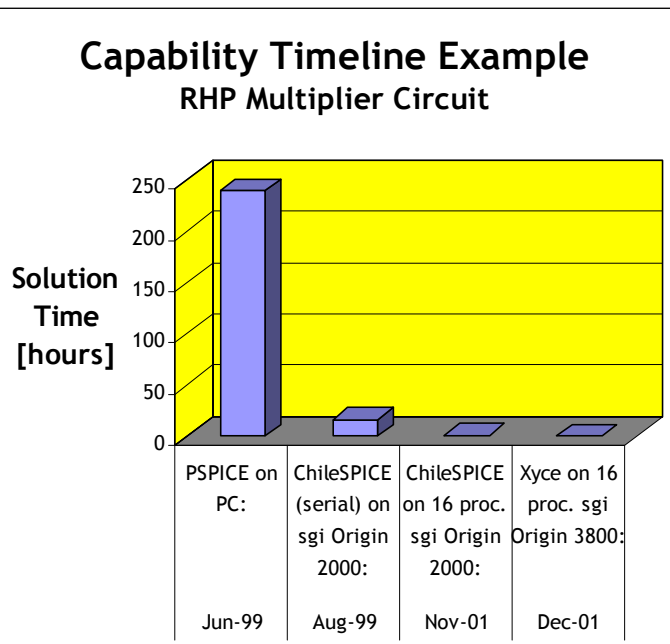
What We've Found (Preliminary)

- **Serial Example - Best case comparisons - Sparse direct vs. Krylov iterative:**

	Newton + SuperLU			Inexact-Newton + GMRES + ILUT		
	# Newton Steps	Linear Solver Time (s)	Total Time (s)	# Newton Steps	Linear Solver Time (s)	Total Time (s)
RHP Adder	61	3.00543	28.3939	55	0.510286	22.4649
CASC	58	0.023597	0.042887	22	0.016613	0.025845

  - Relatively small problems (RHP is ~1800 unknowns)
  - Line searches don't appear to help
  - Behavior isn't consistent as problem grows (e.g., Inexact-Newton method doesn't appear to work well on large problems)
  - Further studies underway…

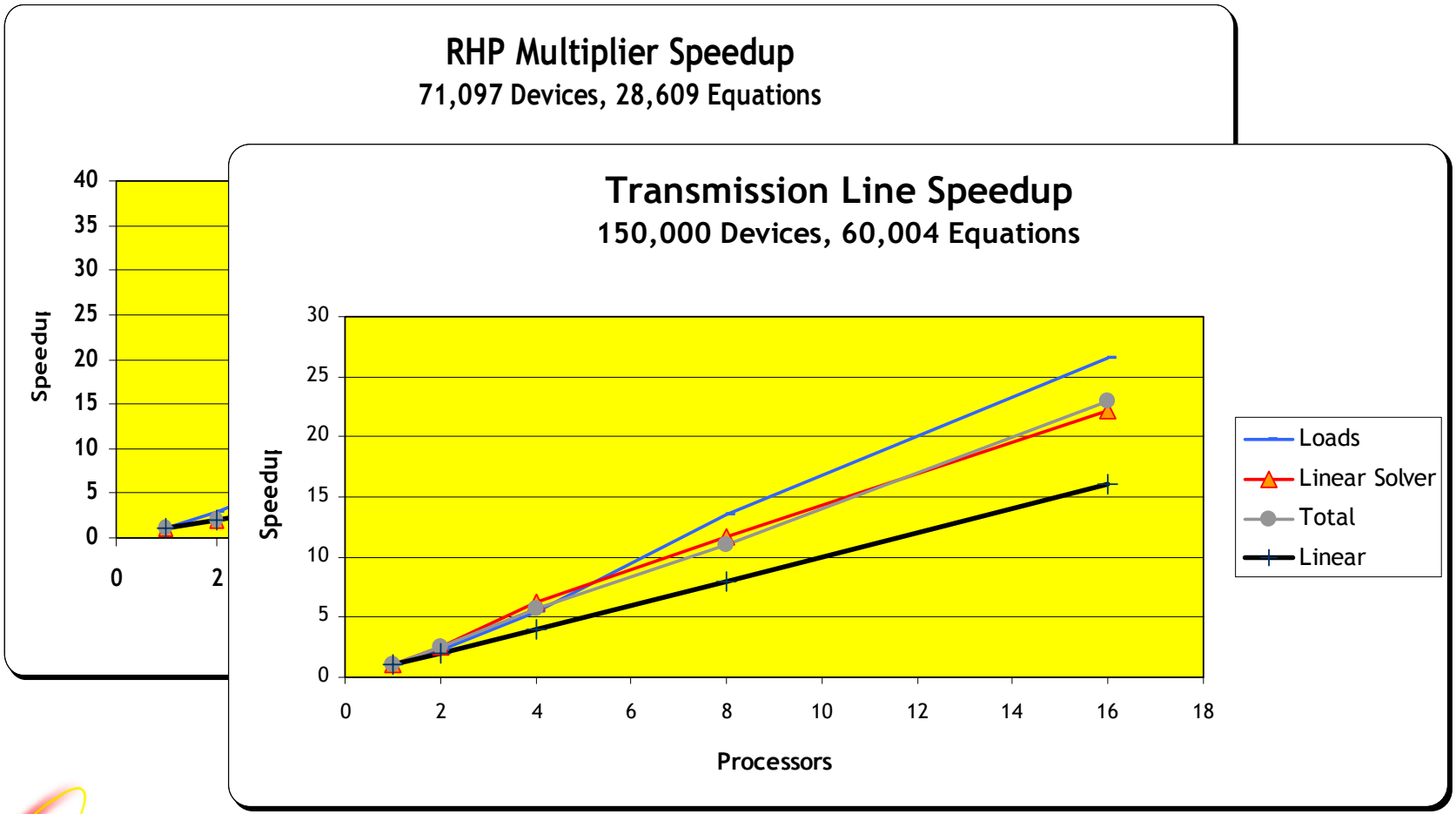
Xyce Performance



- RHP Adder Subcircuit on sgi Origin 3800, MIPS 400 MHz R12k Processors, 8 Mbyte cache
- *NOTE: Code in early development state; minimal optimization performed*

Program Phase	MFlops	Efficiency (800 MFlops max.)
Loads (Residual + Jacobian)	11.3	1.4 %
Linear Solve (Trilinos/Aztec)	96.6	12.1 %
Total Solution	32.9	4.1 %

Xyce Fixed Problem-Size Parallel Scaling

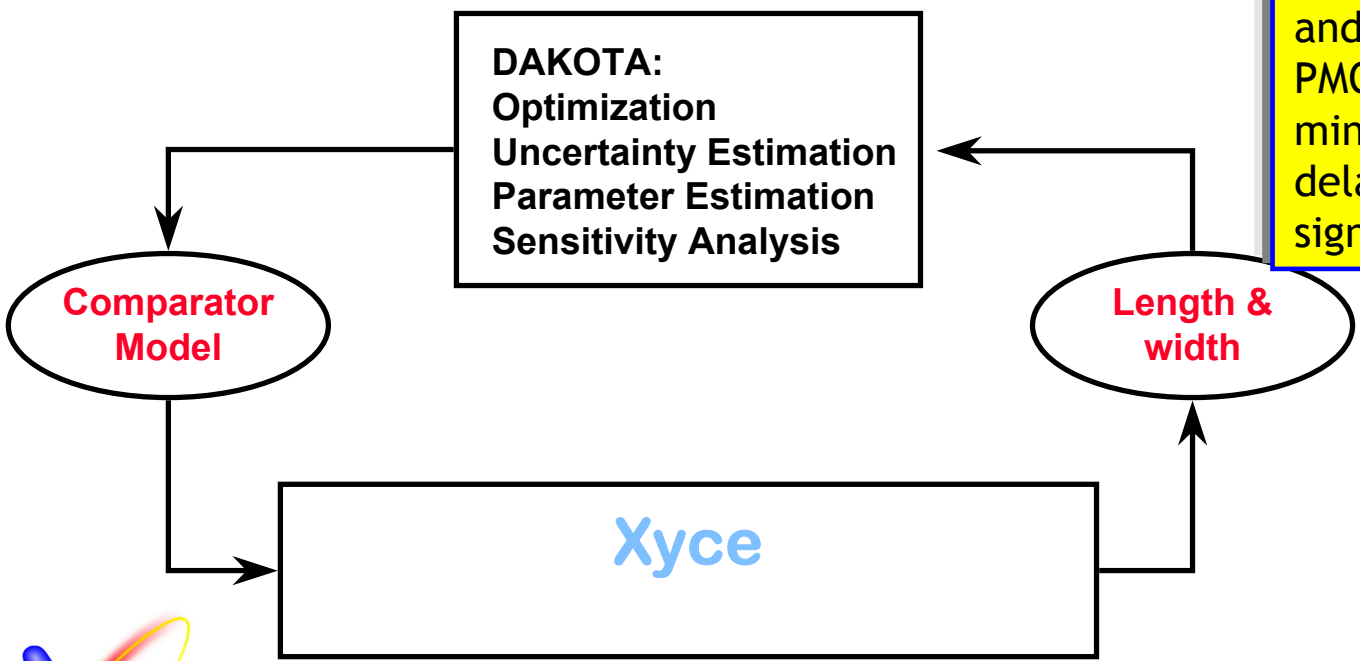


Xyce/DAKOTA: Overview

(work with Bart van Bloemen Waanders)

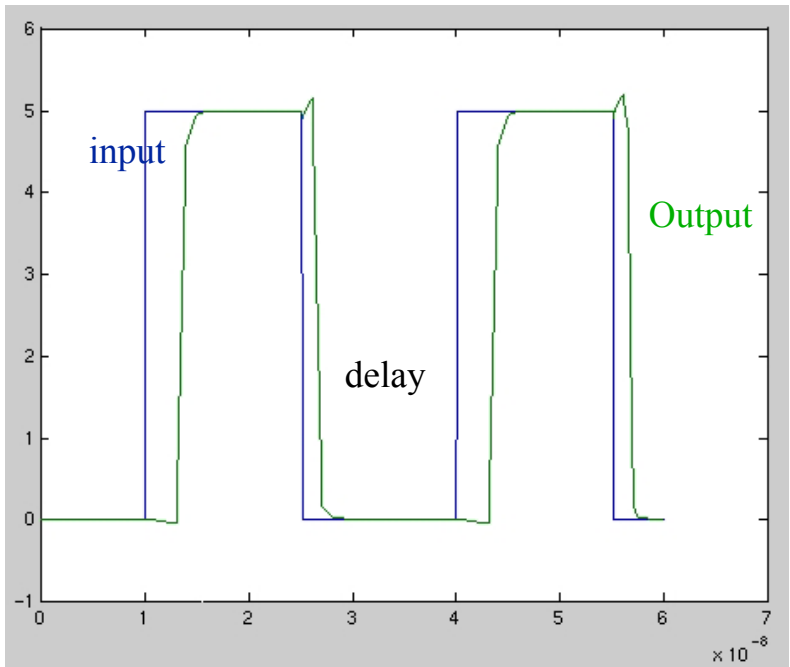
- DAKOTA is a framework of tools for optimization, uncertainty estimation, and sensitivity analysis, for use with massively parallel computers.

Design Goal:
find optimal width and lengths for NMOS & PMOS device features to minimize delay of input and output signal



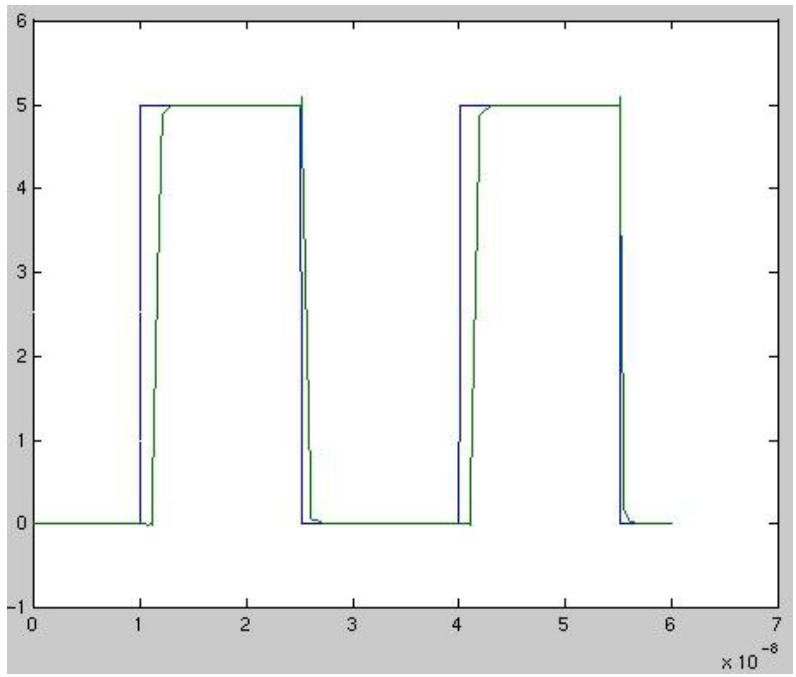
Xyce/Dakota Minimize Delay Results Comparator Circuit

Nominal Design



length = 2E-6, width = 2E-6

Final Design



length = 1E-6, width = 5E-6

* Found solution in 6 fcn evaluations using gradient based method vs 50 fcn evaluations using coordinate pattern search

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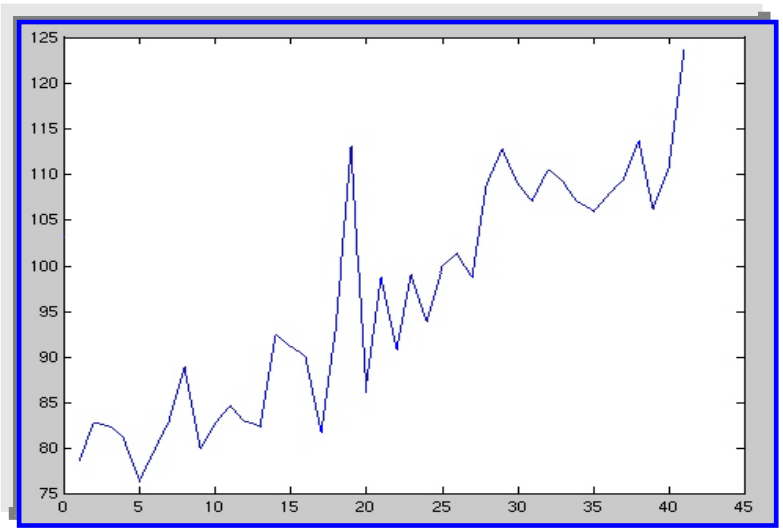
Xyce/DAKOTA FPGA Circuit Flipflop Device Optimization

- FPGA consists of XOR, AND, flipflop circuits
- flipflop circuit - 34 devices divided into 12 design variables -(6 x widths/lengths) chosen based on nominal width and length specifications
- Minimize delay between input and output signal
- Centered parameter study results:
  - random lower values
  - Xyce terminated in certain design space
- Gradient based method (npsol-sqp) failed,
- Vector parameter study from initial point to bounds (40 steps):
  - identified non-smooth behavior
  - multi-modal

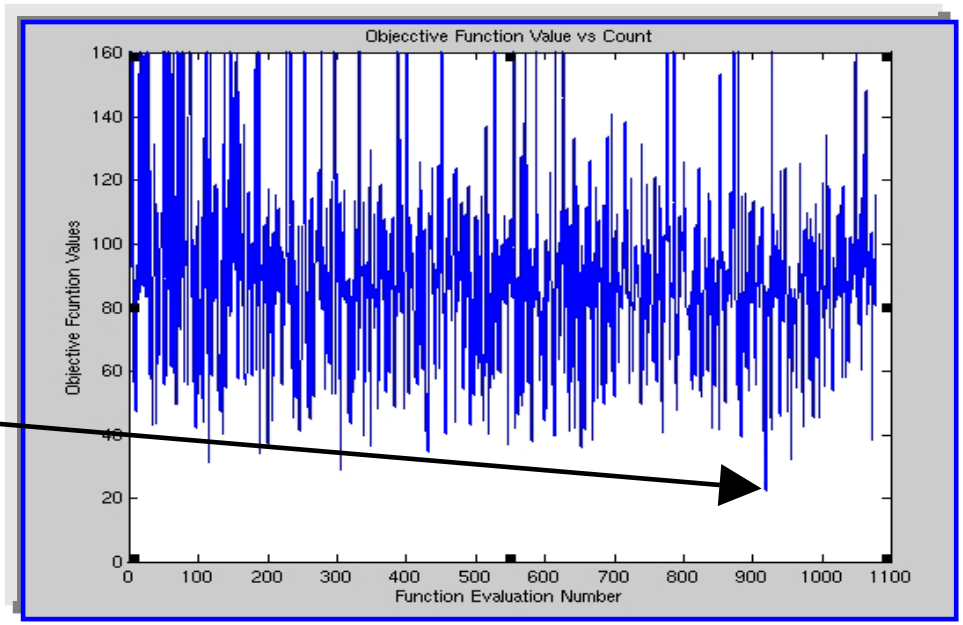
Vector Parameter Study - non-smooth behavior



- Genetic Algorithm study identified best design
  - 1000 function evaluations using population size of 160 (7 cycles)
  - SGOPT pga_real (W.Hart) / ran overnight on 8 proc linux cluster

Xyce/Dakota FPGA Circuit flipflop Device Optimization Results

Best Design



	L1	W1	L2	W2	L3	W3	L4	W4	L5	W5	L6	W6	Objective Fn
Nominal	0.6	2	0.6	4.8	0.6	5.1	0.36	3.8	0.6	2.8	0.6	6.6	112.1
Optimal	0.55	2.1	0.66	4	0.54	5.1	0.28	4.9	0.51	2.4	0.52	6	29.1

FPGA Transistor Groups Channel Length & Width Values [um]

Sandia HPEMS Status

- **Shared-memory ChileSPICE production computing:**
  - Several performance enhancements
  - Radiation models
- **Distributed-memory Xyce analog simulator in beta release:**
  - Large-scale transient analog simulation
  - Design optimization demonstrated with DAKOTA
  - Initial analog/device-scale coupling demonstrated
  - Radiation models implemented by end of FY
  - Mixed-signal simulation capability work underway

Outstanding Challenges (from our perspective) / Future Work

- Parallel preconditioned Newton-Krylov methods
  - Faster performance, Improved robustness
- Parallel sparse-direct solver library
- Stiff DAE integration
  - What's the status on waveform relaxation?
  - Fast Solvers?
- Homotopy methods for circuit simulation
- Constrained Newton methods - "continuous" voltage limiting
- Parallel partitioning / Ordering methods
- Robustness - *Too many solution parameters!*
- Adjoint sensitivities/optimization
- Schematic capture GUI for large problems (> 10^6 devices)
- Large-scale parasitic extraction

Thanks!

- **Sandia Computer Science Research Institute (CSRI):**
  - David Womble, Deanna Ceballos, Barbara Delap
  - CSRI Executive Board (David Womble, Bill Camp, Paul Yarrington, Neil Pundit, Juan Meza, Danny Sorenson, Deepak Kapur)
- **Workshop Colleagues:**
  - Tammy Kolda (Sandia), Bob Melville (Agere)