

# A FULLY DRY SELF-ASSEMBLY PROCESS WITH PROPER IN-PLANE ORIENTATION

*Sangjun Park and Karl F. Böhringer*

Department of Electrical Engineering, University of Washington, Seattle, Washington, USA

## ABSTRACT

A fully dry self-assembly method for chip-to-wafer stacking is developed in this paper. The assembly elements and substrate have complementary and interlocking features that place the assembly parts in the designated binding sites on the substrate. Proper in-plane orientation is achieved by deploying secondary features on the parts and substrate. These features are fabricated by a series of silicon deep RIE, sidewall passivation coating and isotropic etching. Experimental results show 100% assembly is accomplished on substrates with 2cm diameter, and 95% of assembly is done within 1 minute.

## 1. INTRODUCTION

Three-dimensional integrated circuits (3-D ICs) are emerging since they provide larger packing density and improved performance by eliminating horizontal wiring [1]. 3-D integration technology based on wafer-to-wafer bonding has been actively developed [2, 3]. However, this wafer-to-wafer bonding method is only applicable to devices with high process yield since the number of faults in 3-D circuits increases exponentially with the number of layers. In order to stack known good dice (KGD), a chip-to-wafer bonding method is preferable; also, it can integrate various elements with different chip sizes and chip thicknesses at much lower cost than system-on-a-chip (SoC). Conventional robotic pick-and-place assembly becomes less attractive for this application as it is a serial process; instead a parallel self-assembly method that yields high throughput is necessary [4].

The dry self-assembly method has a number of advantages over common fluid-based self-assembly such as shape-recognition [5] or capillary-driven methods [6, 7]; 1) it does not involve wet processing, so it does not affect parts with materials or coatings sensitive to water, and 2) the number of redundant parts required is much less than the fluid-based self-assembly that demands parts 5 to 100 times the number of binding sites [5, 7].

We previously reported a fully dry self-assembly method for chip stacking, but the in-plane orientation had not been achieved [8]. This paper presents a dry self-assembly method with proper in-plane orientation and high assembly rate.

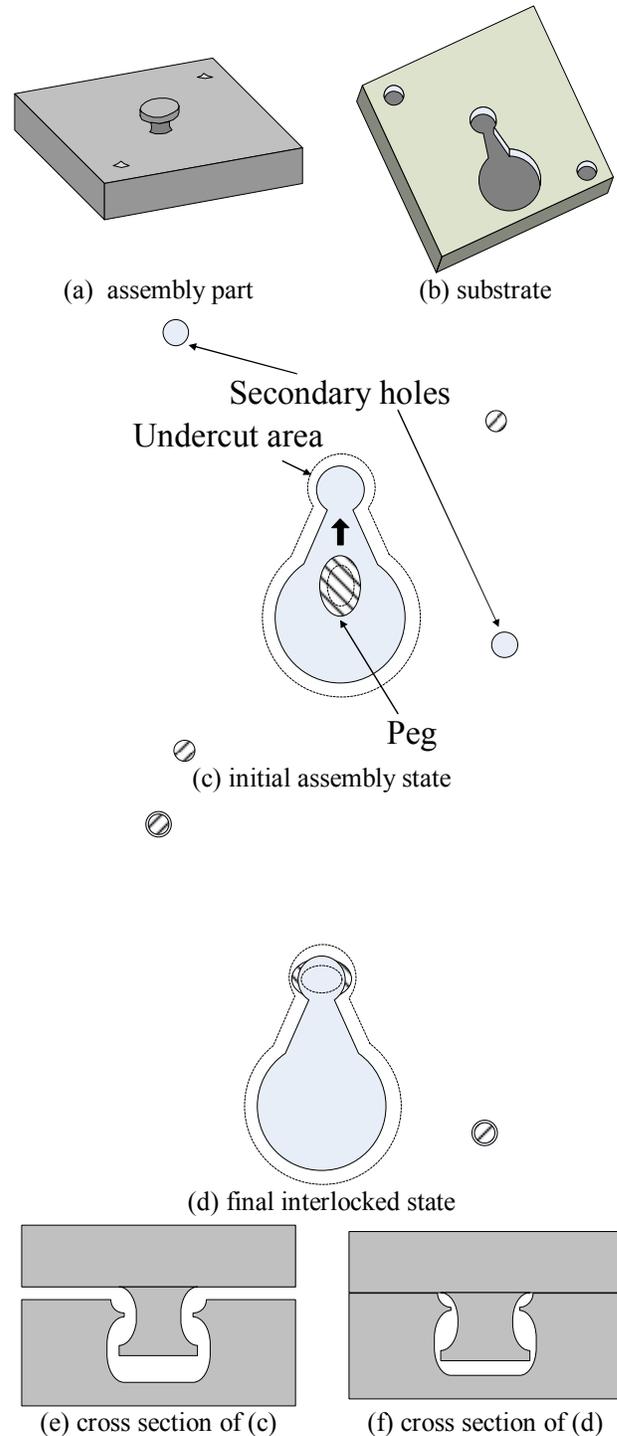


Figure 1: Schematic view of the assembly system and illustration of "lock-in" mechanism.

## 2. DESIGN OF ASSEMBLY SYSTEM

Figure 1 shows a schematic view of the assembly system. The assembly part has an interlock pin similar to a nail, and two small secondary pins as shown in Fig. 1(a). The “nailhead” part of the interlock pin has an elliptical shape. The corresponding substrate has a binding site consisting of a large circular hole (350 $\mu\text{m}$  in diameter), a small interlock hole (100 $\mu\text{m}$  in diameter), a pathway between them, and two secondary holes (70 $\mu\text{m}$  in diameter).

When vibration is applied to the substrate with the assembly parts on it, the interlock pin will fall into the large circular area initially, and then move to the small interlock hole, as shown in Fig. 1(c). When the “nailhead” part moves into the small pocket of the interlock hole, the assembly part rotates until the secondary pins meet secondary holes in the substrate (Fig. 1(d)). The secondary pins and holes properly orient the assembly parts. Note that once the interlock pin gets into the interlock hole, it is difficult to get out because of the elliptical shape of the nailhead.

## 3. FABRICATION

The fabrication process is shown in Fig. 2. It is mostly identical in both the fabrication of the assembly part and substrate, with a slight change in the etching depths. The process starts with deposition and patterning of an etch mask (PECVD oxide). A shallow isotropic RIE (150mTorr,  $\text{SF}_6=100\text{sccm}$ , 50W in Trion RIE) is done only on the substrate, so that the interlock pin of the assembly part can safely settle as shown in Fig. 1(f). Then the first deep silicon RIE is performed, and a PECVD oxide is deposited uniformly on all surfaces of the structure as shown in Fig. 2(d). The PECVD oxide is etched by anisotropic RIE, so that the oxide on the sidewalls still remains. The silicon is etched again by deep RIE, and an isotropic RIE etches the unprotected area exposed by the second deep RIE. At this step, the shank of the pin and the pocket in the binding site are formed. The secondary pin is made smaller at this step by losing its etch mask by the isotropic etch. Finally, all etch masks and passivation films are removed in hydrofluoric acid (HF).

SEM pictures of the fabricated system are shown in Fig. 3. The process is applied on both sides of the assembly parts, such that the parts can be mated on either side. The assembly part has 1.27mm width and 200 $\mu\text{m}$  thickness. The elliptical pin is 130 $\mu\text{m}$  in long axis and the undercut beneath the head is about 20 $\mu\text{m}$ . The substrate has 21 binding sites in 314mm<sup>2</sup> area. This corresponds to a fill factor of 18%. The interlock hole has 100 $\mu\text{m}$  diameter at the neck and 140 $\mu\text{m}$  at the pocket. The secondary pins are about 20  $\mu\text{m}$  in height.

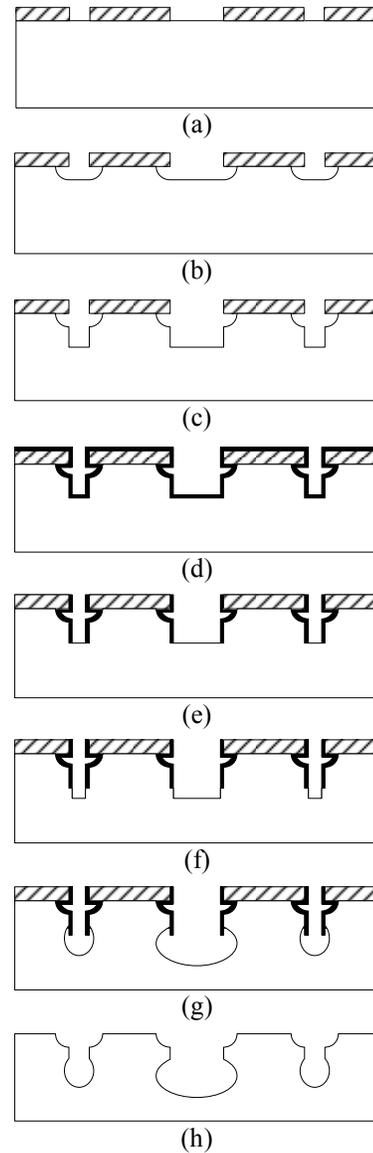


Figure 2: Fabrication process flow of interlock hole. (a) lithography, (b) isotropic RIE Si etch, (c) DRIE, (d) Si passivation, (e, f) anisotropic trench etches, (g) isotropic Si etch, (h) removal of mask and passivation.

## 4. EXPERIMENTAL RESULTS

The substrate is mounted on a loudspeaker, which is vibrated by an amplifier connected to a function generator. A glass tube is mounted on the substrate to avoid the assembly parts from flying away. Figure 4 shows the assembly result after 3 minutes of excitation with 127Hz sinusoidal wave. This frequency is selected since the loudspeaker applies a leveled excitation to the substrate at this frequency. Unleveled excitation causes the parts to move in one particular direction, which results in a substantially lower assembly yield. The amplitude of vibration is 7 $\mu\text{m}$ , and the maximum acceleration is 4.5m/s<sup>2</sup>. 31 assembly parts (50% redundancy) are used in this experiment. All of the 21 binding sites are

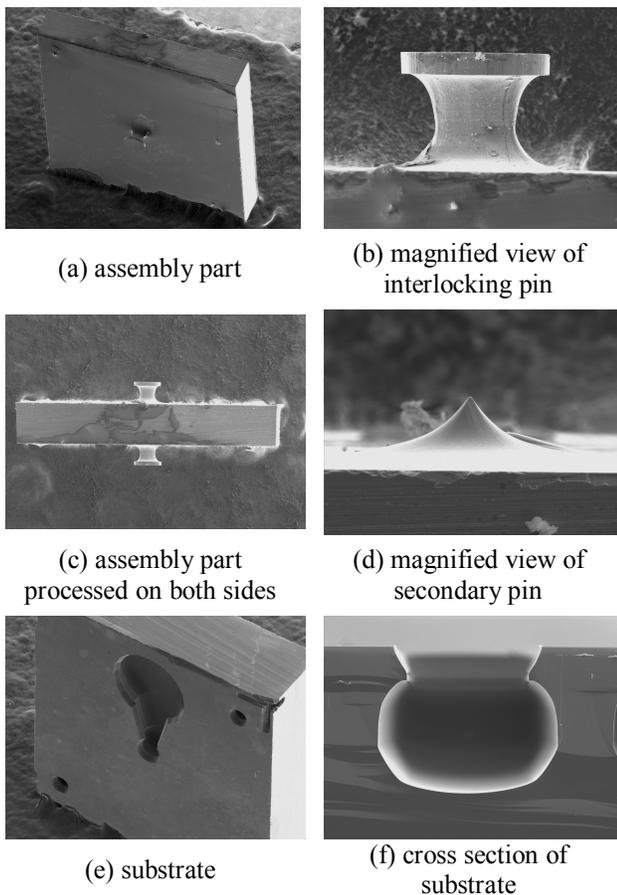


Figure 3: SEM photographs of fabricated self-assembly system.

occupied with the assembly parts, and also all of them are properly oriented. The excessive parts after the assembly are removed simply by flipping the substrate over. The maximum orientation error is 1.7 degrees, and the maximum translational error is  $\pm 5\mu\text{m}$ . This error derives from the safety margin in the design, which has been included as tolerance for process variations. The assembly rate versus time is shown in Fig. 5. The experiments are repeated 10 times and 100% assembly is ultimately accomplished for all cases. 95% of assembly is reached within 1 minute of vibration.

## 5. CONCLUSIONS

In this paper, a fully dry self-assembly method for chip-to-wafer stacking was developed. A high assembly yield and a high assembly rate were achieved as well as proper in-plane orientation of the parts.

The effects of higher fill factor and scaling of the part sizes should be further investigated. For the electrical interconnections between the assembly parts and substrate, the secondary pins can be made of solder bumps, and metal pads can be implemented in the secondary holes.

Work is underway to make stacks of multiple parts on a

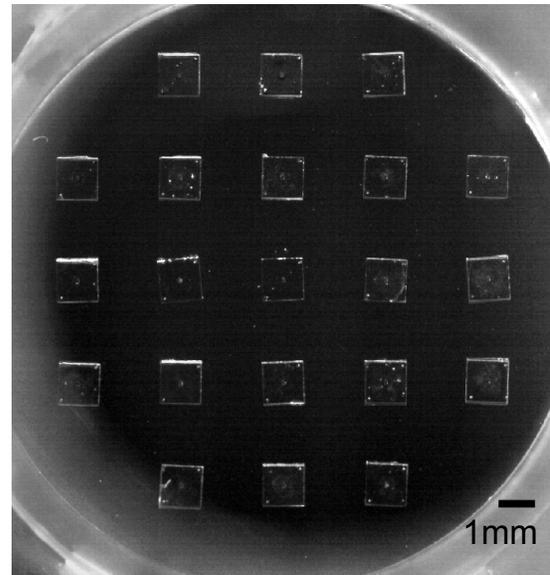


Figure 4: Self-assembled parts on substrate. The maximum alignment error is 1.7 degrees.

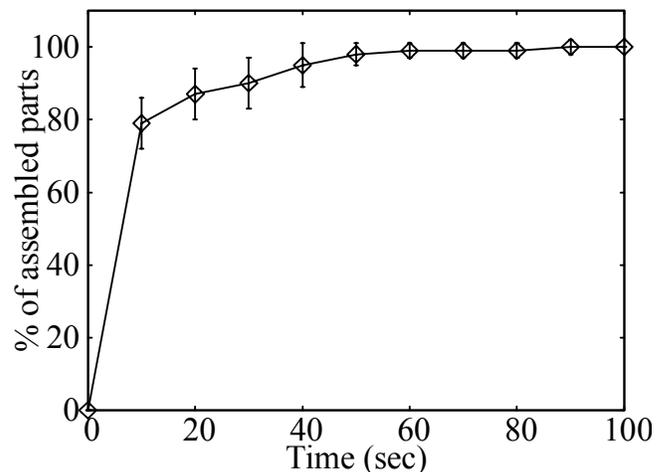


Figure 5: Plot of assembly rate. The error bars indicate the standard deviation. The data are averages of 10 experiments.

substrate. There can be different combinations of the complementary patterns on two sides of the assembly parts. In this way, multiple stacking of various elements in a designated order can be implemented.

## 6. ACKNOWLEDGMENTS

This work was conducted at the Washington Technology Center Microfabrication Laboratory and at the Center for Nanotechnology User Facility at the University of Washington, a member of the National Nanotechnology Infrastructure Network (NNIN) supported by NSF. This work was supported in part by NSF grant ECS-05-1628. S. P.

was supported in part by IT Scholarship Program from IITA (Institute for Information Technology Advancement) and MIC (Ministry of Information and Communication), Republic of Korea.

## 7. REFERENCES

- [1] A. Klumpp, R. Merkel, R. Wieland, and P. Ramm, "Chip-to-wafer stacking technology for 3D system integration," in *Proc. 2003 Electronic Components and Technology Conference*, pp. 1080-1083.
- [2] J.-Q. Lu, et al., "A wafer-scale 3D IC technology platform using dielectric bonding glues and copper damascene patterned inter-wafer interconnects," in *Proc. IEEE 2002 International Interconnect Technology Conference*, pp. 78-80.
- [3] A. W. Topol, et al., "Enabling SOI-based assembly technology for three-dimensional (3d) integrated circuits (ICs)," in *Tech. Digest IEEE Electron Devices Meeting (IEDM) 2005*, pp. 352-355.
- [4] T. Fukushima, Y. Yamada, H. Kikuchi, and M. Koyanagi, "New three-dimensional integration technology using self-assembly technique," in *Tech. Digest IEEE Electron Devices Meeting (IEDM) 2005*, pp. 348-351.
- [5] S. A. Stauth and B. A. Parviz, "Self-assembled single-crystal silicon circuits on plastic," *P. Natl. Acad. Sci. USA*, vol. 103, no. 38, pp. 13922-13927, 2006.
- [6] X. Xiong, Y. Hanein, J. Fang, Y. Wang, W. Wang, D. T. Schwartz, and K. F. Böhringer, "Controlled multibatch self-assembly of microdevices," *J. Microelectromech. S.*, vol. 12, no. 2, pp. 117-127, 2003.
- [7] W. Zhang, P. Buhlmann, and H. O. Jacobs, "Sequential shape-and-solder-directed self-assembly of functional microsystems," *P. Natl. Acad. Sci. USA*, vol. 101, no. 35, pp. 12814-12817, 2004.
- [8] S. Park and K. F. Böhringer, "Fully dry 2D and 3D self-assembly with interlocking pin fasteners," *Proc. Transducers '07*, pp. 2079-2082.