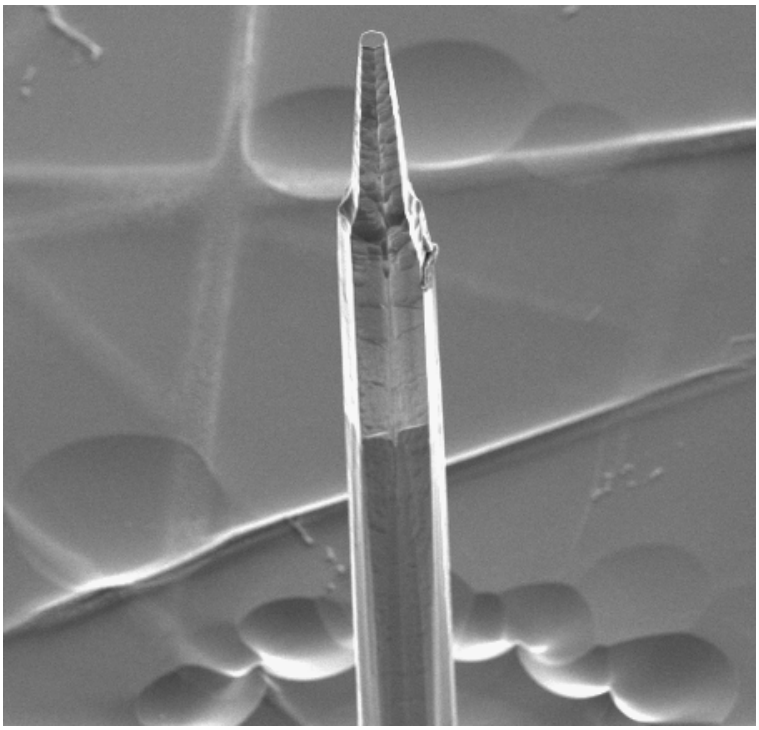
**Universität Karlsruhe (TH)**
**Institut für Mikrostrukturtechnik (IMT)**

**University of Washington**
**Department of Electrical Engineering**


# Master's Thesis

## Silicon micro-needles with flexible interconnects and tip metallization for intracellular applications



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December 13th, 2002

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**Author's Statement**

I certify that I have performed this work on my own, and that all sources that I have used or consulted are duly noted herein.

Seattle December 13th, 2002

## Acknowledgment

I want to thank

- my two supervisors, Prof. Saile and Prof. Böhringer for all their support and efforts, to give me the opportunity to come to the United States and to the University of Washington in Seattle,
- Christian Schabmueller for his patience while training me at the WTC clean room,
- Yael Hanein for explaining the needle project to me and discussing my thesis,
- Tai-Chang Chen, Keith Ritala, Eric Miller, Karen Nishimura, Kevin Kerkof, Yanbing Wang, Mark Mendez, Greg Golden and Anupama Govindarajan for their valuable help and useful comments,
- Corrie Smith, who became a very good friend during the last months, while we were driving to the university together, and for reviewing this thesis.

Finally, I want to thank my host family, Christine and Mike Ritchey, for everything they have done for me, especially for their outstanding hospitality and support during the last six months and making my stay in Seattle possible for me.

Peter Lücke

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# 1 INTRODUCTION

Intracellular sensing probes hold great promise for providing insight into the physiology and processes of single living cells. Current techniques for intracellular recording utilize glass capillaries and fine insulated conducting wires. However, these instruments have several drawbacks, including large dimension, limited integration with other components, and very limited ability to record in vivo.

In cooperation with the University of Washington Friday Harbor Marine Laboratories, many experiments have been performed on brain cells in the marine mollusk Tritonia diomedea. The brain structure of this sea slug is relatively simple and the function and location of individual brain cells (neurons) are well known. Brain cells up to 500µm in size make it possible to reidentify individual neurons and to perform identical experiments on different slugs.

At the University of Washington Micro-Electrical-Mechanical-Systems (MEMS) laboratory, processes have been developed to create silicon micro-needles, both singly and in arrays, suited for intracellular interfacing. To allow intracellular recording, neural probes with extremely sharp (<1µm) and long (>300µm) tips for effective bending and penetration are required. Also, coverage of the tip with metal and nitride is necessary to enhance the electrical properties of the metal-electrolyte interface (needle and intracellular fluid), and to insulate the base of the needle, allowing electrical signals to be obtained exclusively from the inside of the cell. The processes involve the creation of pillars through the use of deep reactive ion enhanced (DRIE) etching, and pillar sharpening via reactive ion enhanced (RIE) etching. The isolated needle-like microelectrodes are connected with an aluminium wire and encapsulated by a flexible polyimide-based interconnect. This design allows the integration of further components such as amplifiers, batteries, or memory, which is required for reaching the final goal: The fabrication of implantable micro-needle devices for intracellular recording from freely behaving animals.

The current processes using DRIE and RIE for fabricating silicon micro-needles with flexible interconnects are described in the third chapter. To document the process, a detailed step-by-step process listing was made, which can be found in the appendix A.2.

The main theme of this master's thesis is to improve the current process through which an ohmic contact is achieved between the silicon electrodes and the aluminium wire inside the flexible interconnect. To that end, a contact test has been devised and evaluated. The results, including the basics of metal-to-semiconductor junctions, will be discussed in Chapter 4.

The results of etch rate tests used to improve the sharpening step of the needles using RIE are described in the fifth chapter; process changes applied during this thesis will also be discussed.

As mentioned above, intracellular measurements require an electrode with a conducting tip and an insulated base. The final task of this thesis has been the development of a new method for insulating the base of the needle-electrode and the metallization of the needle tip. This new method is presented in the sixth chapter.

For a better understanding of the requirements of electrode devices suitable for intracellular measurements, this master's thesis first reviews the basics of extra- and intracellular recording.

# 2 PRINCIPLES OF INTRACELLULAR NEURONAL RECORDING

Understanding the neural basics of behavior is one of the most challenging research goals today. Brains consist of a complex, interactive network of neural cells (neurons). In small invertebrates such as leeches, several hundred neurons are connected, while in the human brain, there are several trillion neural connections. This network is responsible for motor functions, learning, memory, and decision-making. During the last decade, neuroscience has gained much knowledge about the structure, function, and organization of these neural networks through the use of extracellular probes. However, the information gathered by extracellular probes is not from a single cell, it is an average over several cells located near the probe. These extracellular probes do not provide the critical information about the DC state of a cell, nor can they be used to identify the behavior of a single cell. Many questions are still unsolved related to brain activity and neural network processes. It is believed that some questions could be answered if scientists were able to measure the activity of single neurons from animals in their natural habitat. This would help to understand the correlation between neuronal activity and external stimulation, communication patterns inside neural networks, as well as neuronal activity and behavior.

This shows the potential for intracellular probes. In order to obtain signals just from the inside of one cell, the tip of such a probe needs to be extremely sharp (<1µm) and long (>300µm). This is required for effective bending and penetration of the flexible cell membrane.

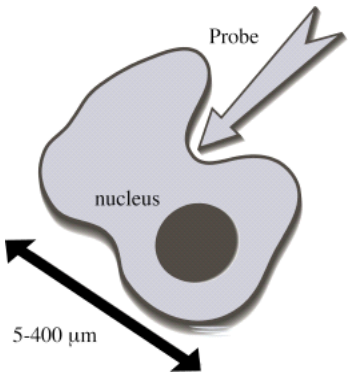
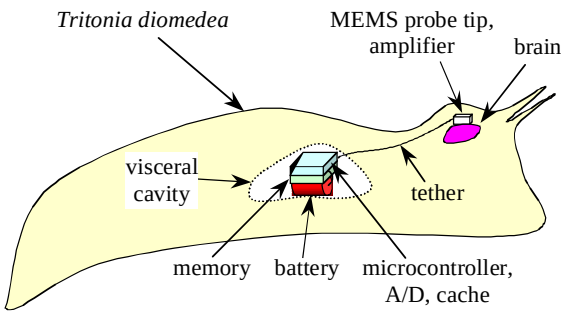



Figure 2.1: Schematic drawing of the bending of the cell membrane [HaLa02]

Existing probes for intracellular sensing are using fine insulated conducting wires or sharp glass capillaries. The capillaries are transformed into neural probes by filling them with an electrolyte and placing a silver/silver chloride electrode in the electrolyte. After penetrating the cell membrane the glass provides an ionic insulation and ensures low leakage current, thus only signals from the inside of the cell are recorded.

However, these methods have a number of drawbacks, including too large dimensions and limited ability to be integrated them with other components such as amplifiers, memory, and batteries. Therefore, they are not implantable into freely behaving animals.

The UW MEMS lab has presented an approach for fabricating silicon micro-needles, both singly or in arrays, with flexible interconnects for intracellular applications. These devices are very promising to overcome the problems mentioned above. They offer small dimensions and built-in integrated circuit capabilities. The tip geometry is very similar to the geometry of the glass capillaries. To obtain only signals from the inside of cells, a sealing between the recording electrode and the cell membrane is required. The glass capillaries provide a good sealing after penetrating the cell membrane, as the glass provides an ionic insulation and ensures low leakage current. The solid silicon micro-needles are fabricated with highly conducting silicon, therefore, they need to be insulated with a dielectric layer, except for the very tip.




To demonstrate the performance of the silicon micro-needles as neural probes for intracellular recording, a partnership between the UW MEMS lab and the UW Friday Harbor Marine Laboratories has been initiated. This laboratory is focused on extra- and intracellular measurements on the brain cells of the marine mollusk Tritonia diomedea. The brain structure of these sea slugs is relatively simple and the functions and locations of individual and reidentifiable neurons are well known. The large dimensions of these neurons (~400µm) make it possible to identify specific cells, and to perform reproducible experiments on different slugs.

Furthermore, the sea slug has a large visceral cavity in which an autonomous implant system can be buried.


Figure 2.2: Brain of the marine mollusk Tritonia diomedea

Figure 2.3 shows the results of first measurements with silicon needles from the inside of one cell.

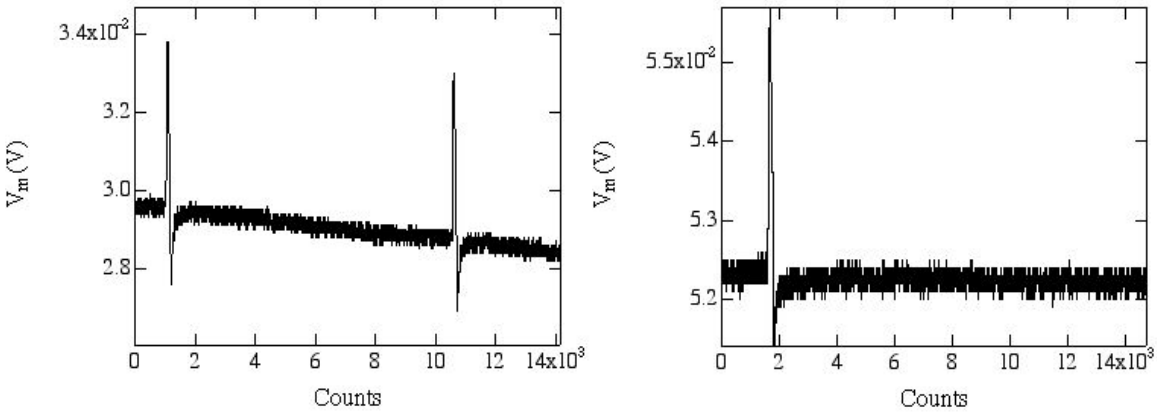



Figure 2.3: Spontaneous intracellular potentials in a sea slug brain

# 3 FABRICATION

This chapter reviews the complete fabrication process of the needle devices. The current processes are using Deep Reactive Ion Enhanced (DRIE) and Reactive Ion Enhanced etching (RIE) for etching and sharpening of the high aspect pillars. For better understanding of the fabrication process, the following section gives an overview of the involved plasma etching machines, as well as the photolithography tools, used for needle fabrication at the Washington Technology Center (WTC) clean room.

## 3.1 Photolithography and Plasma Basics

### Photolithography

Photolithography is essential in MEMS fabrication processes for masking. During the fabrication processes of the silicon micro-needles the positive photoresists AZ1512 and AZ4620 from Clariant and the polyimide PI2721 (negative resist) from HD MicroSystems are used. The polyimide functions as flexible structural material and, due to its good insulation attributes, as an insulation material for the metallic contact lines. The resists are spun on the wafers using a fully programmable multistep CEE Photoresist Spin Coater. Like many MEMS devices the needle process requires doublesided alignment, which was done with an ABM Contact Aligner. The photomasks were precisely positioned into correct registration with photoresist-coated wafers by infrared light.

### Plasma Etching

Plasma etching techniques are dry etching processes. Inside a plasma, nonreactive molecules are turned into reactive species by introducing energy, such as an electrical charge. The reactivity and the etching effect, i.e. whether the etching is anisotropic or isotropic depends on the chamber geometry, the reaction gas, the vacuum, the applied radio frequency, and the DC bias that is accelerating the ions towards a target.

A standard plasma etching system that can be found in almost every clean room is a Barrel Asher, which uses an oxygen-plasma. Due to the barrel geometry, the etch is isotropic and utilized for removing organic films and contamination from wafers, as well as stripping photoresist.

The Trion Reactive Ion Enhanced (RIE) etcher uses a different chamber geometry. The reaction gases ($SF_6$, $CHF_3$, and $O_2$) are contained between two parallel plates. Depending on the applied DC bias, anisotropic etches can be performed, as reactive radicals are accelerated towards the wafer. For the needle process the RIE is used with $SF_6$ to etch the alignment structures and for the needle sharpening.

The high aspect ratio needles were etched in an Oxford Instruments DRIE (System 100) using the “Bosch Process”, a technique for deep silicon etching developed and patented by the Robert Bosch GmbH.

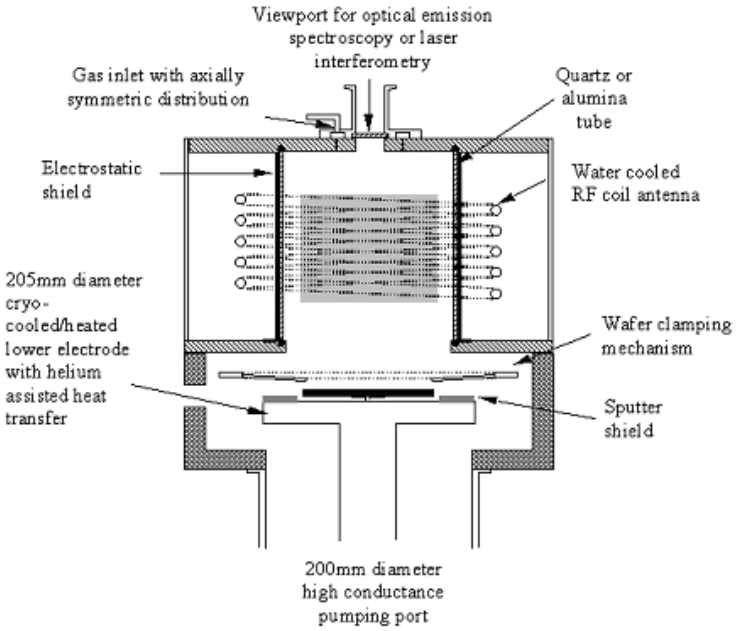



Figure 3.1: Schematic diagram of ICP system used for Bosch processing [MaWa01]

The “Bosch Process” consists of a two step cycle, the silicon is etched using a fluorine plasma chemistry ($SF_6$), followed by fluorocarbon plasma ($C_4F_8$) that provides sidewall passivation and improves the selectivity.

More information about DRIE plasma etching can be found in “Comparison of Bosch and cryogenic processes for patterning high aspect ratio features in silicon” by Martin J. Walker [MaWa01].

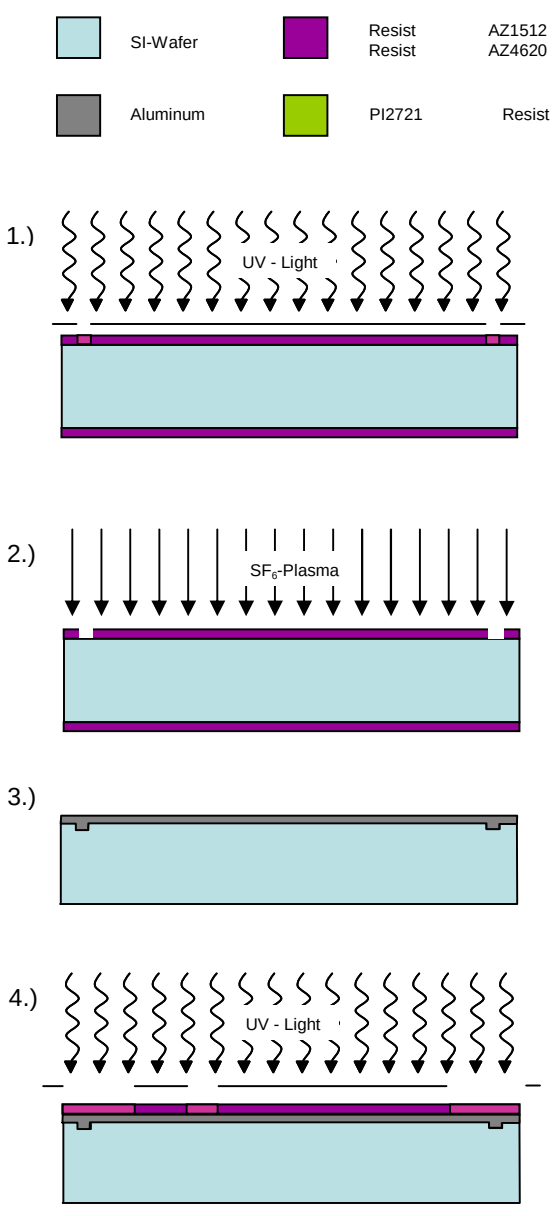
## 3.2 Fabrication of Flexible Silicon Micro-Needle-Devices

This process description follows the procedure presented by [HoHa01] and [ChSc02]. However, small changes have been applied, which will be discussed in detail in Chapter 5. A current step-by-step process listing can be found in section A.2 and a listing of the masks used in section A.6.2.

To fabricate the needle devices, highly conducting 4'' and 500µm thick <100> oriented p-type wafers are used.

The complete needle device consists of four different layers (silicon, polyimide 1, aluminum, polyimide 2), which all need to be carefully aligned with each other. For this reason, alignment structures are created as a first step. Photoresist AZ4620 is spun on the front side and exposed with mask PL-ND-AG. The backside is protected with a blanket cover of AZ1512 (Step 1). The alignment structures are etched with an $SF_6$ plasma in the RIE etcher (Step 2).

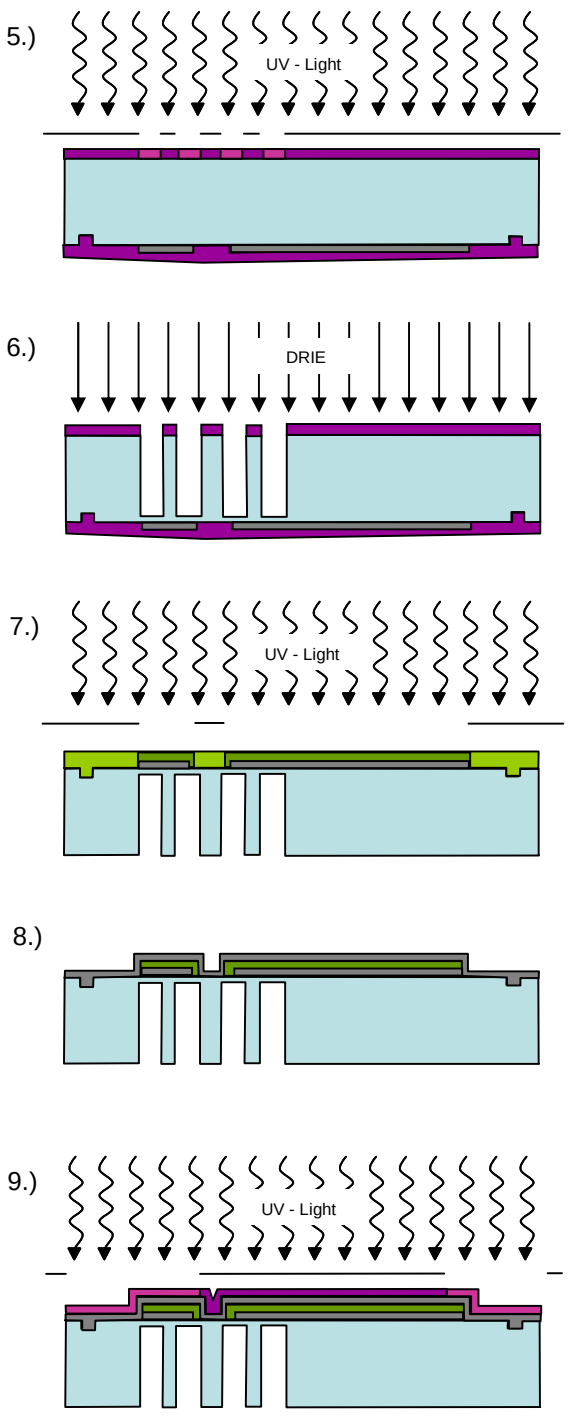
For stripping the photoresist, the wafers are first placed in an $O_2$ plasma in the barrel asher for 10min and then merged into EKC followed by AZ300T for 10min each (this is the standard resist stripping procedure).



To protect the polyimide layer afterwards during the sharpening step, an etch stop layer is either applied by evaporating a 300Å thick aluminum layer or by growing a 2µm thick oxide layer in the furnace on the front side (Step 3). To pattern the etch stop layer, AZ1512 is used and exposed with the mask PL-ND-ETCHSTOP followed by an aluminum etch (for aluminum) or patterned with PL-ND-OXIDE followed by a BOE etch (for oxide) and a final resist strip (Step 4).

To define the needles and the release trench a 12µm thick AZ4620 layer is applied on the backside for masking (mask PL-ND-DRIE) and developed. The frontside is covered with AZ1512 for protection (Step 5). Then the wafer is placed in an Oxford Instruments DRIE and ~450µm tall pillars are etched (etch rate ~2.1µm·min$^{-1}$) (Step 6) (see Figure 3.3 and Figure 3.4). After stripping the resist the wafer surface is activated and dehydrated with an $O_2$ plasma for 10min inside the barrel asher prior to spinning a polyimide layer on the front side. The polyimide PI2721 is exposed using mask PL-ND-PI1 and then cured inside a furnace at 350°C (Step 7).

The polyimide layer is ~10µm thick after curing.



To contact the needles a 7000Å thick aluminum layer is evaporated (Step 8) and patterned with AZ4620 and mask PL-ND-AL (Step 9) followed by an aluminum etch (Step 10). To promote better adhesion and to activate and dehydrate the surface, the wafer is placed for 30sec in an $O_2$ plasma inside the barrel asher, prior to spinning on the second polyimide PI2721 layer.

The polyimide is exposed using PL-ND-PI2 (Step 11) and developed (Step 12). The curing step for the second polyimide layer is also an annealing step for the aluminum contacts. For this purpose, the furnace is first heated to 350°C for 20min for curing and then ramped up to 400°C for 10min to perform the aluminum annealing.

To sharpen the needle pillars and to release the completed device the wafer was placed in an RIE etcher with an $SF_6$ plasma (Step 13). During the sharpening, the protection pillars that surround the needle are first totally etched away (see Figure 3.5 and Figure 3.6), and then for the release the remaining silicon at the bottom of the trench is etched away (Step 14) (see Figure 3.7).

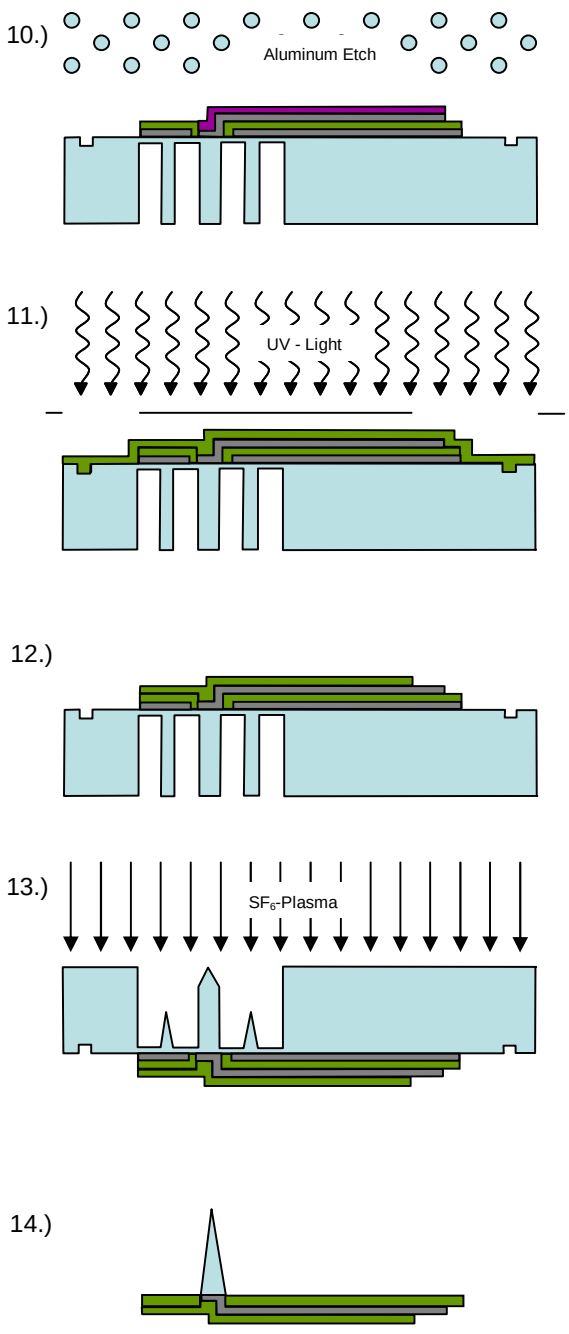



Figure 3.2: Needle Process

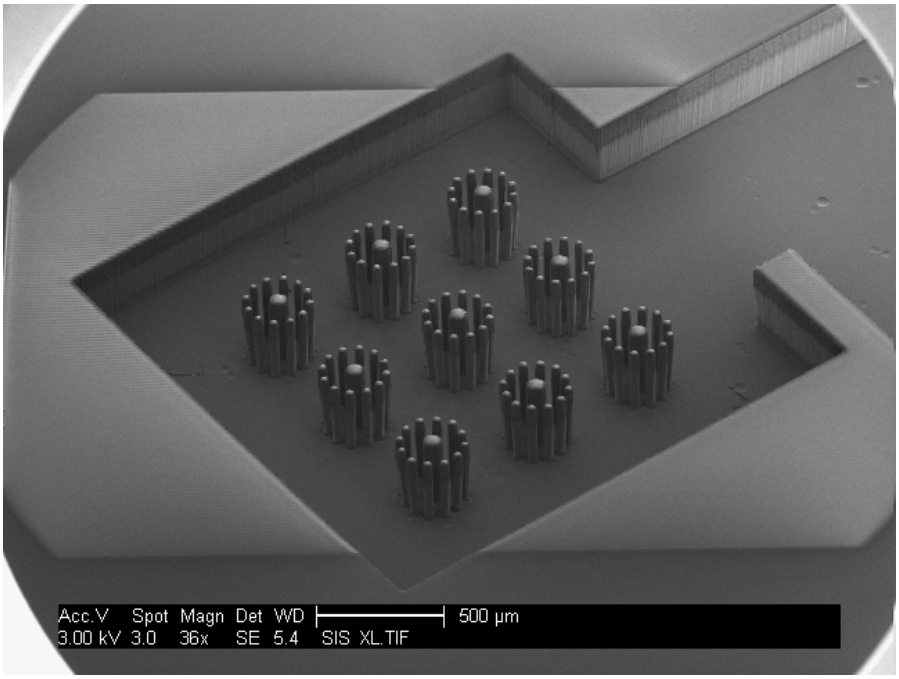



Figure 3.3: Needle array after DRIE

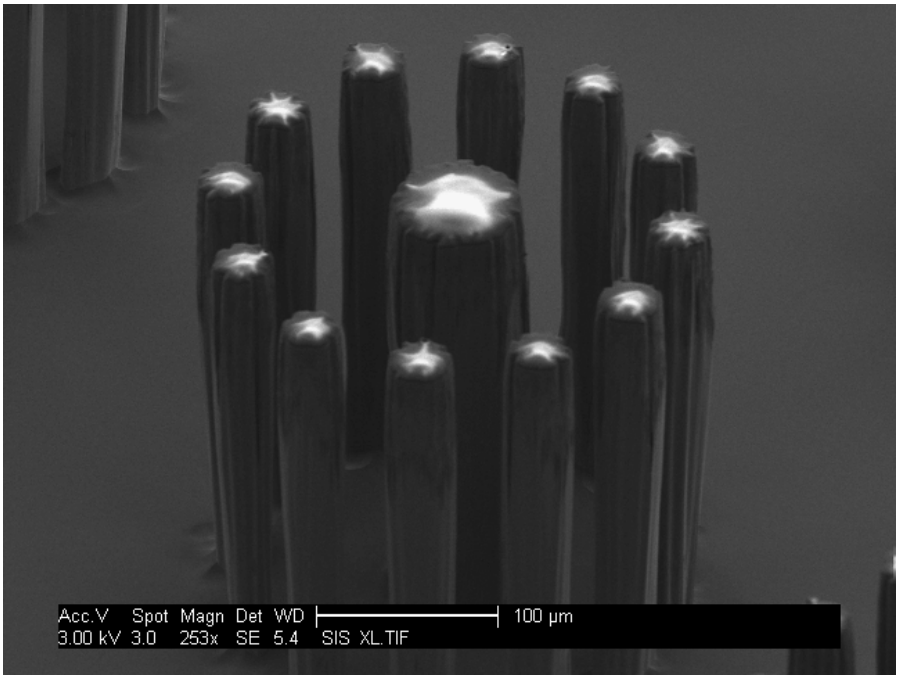



Figure 3.4: Needle pillar with surrounding protection pillars after DRIE

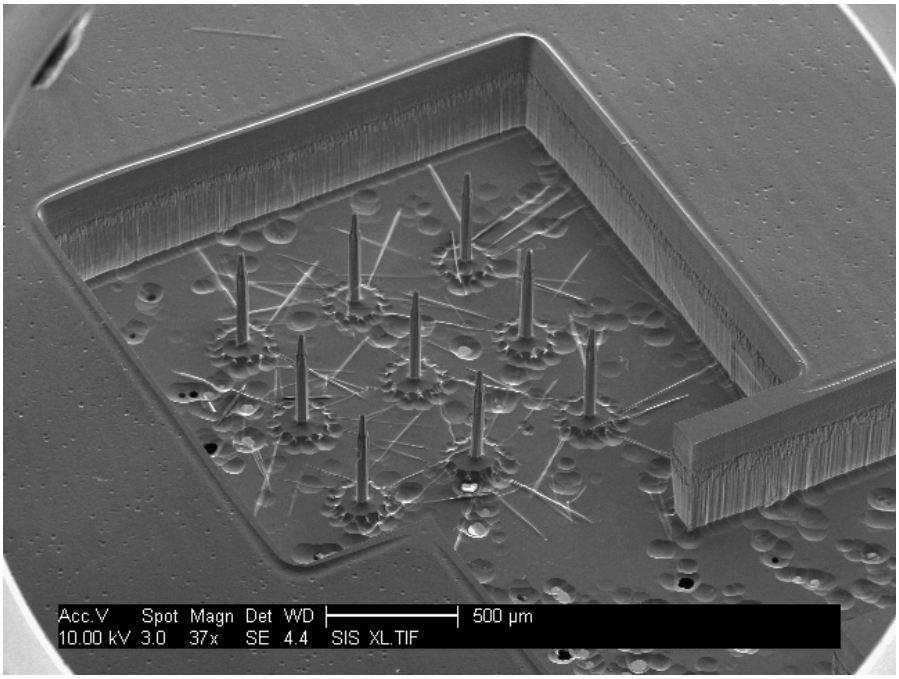



Figure 3.5: Needle array during RIE sharpening

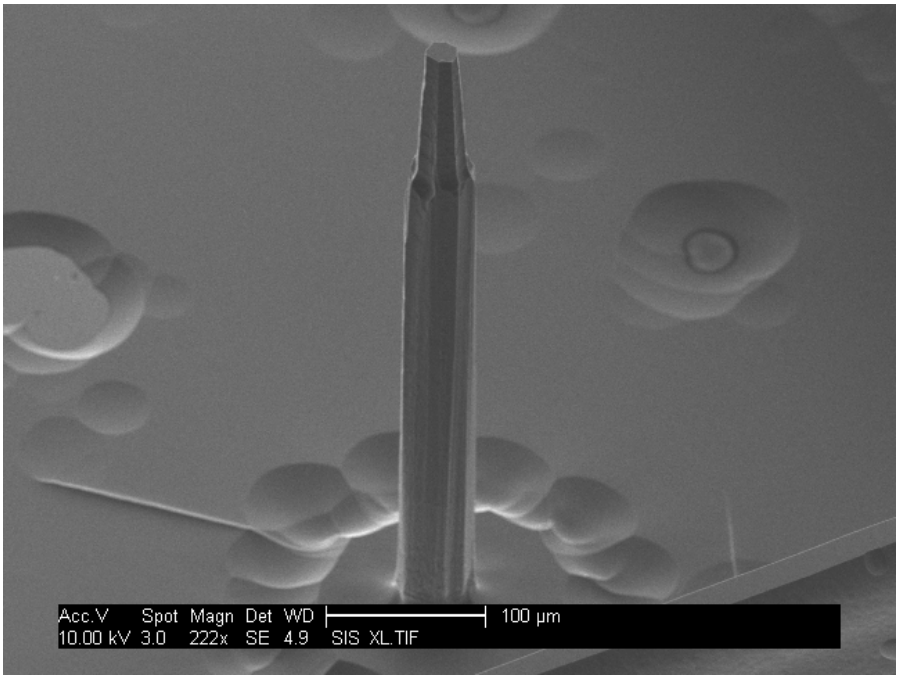



Figure 3.6: Single needle during RIE sharpening

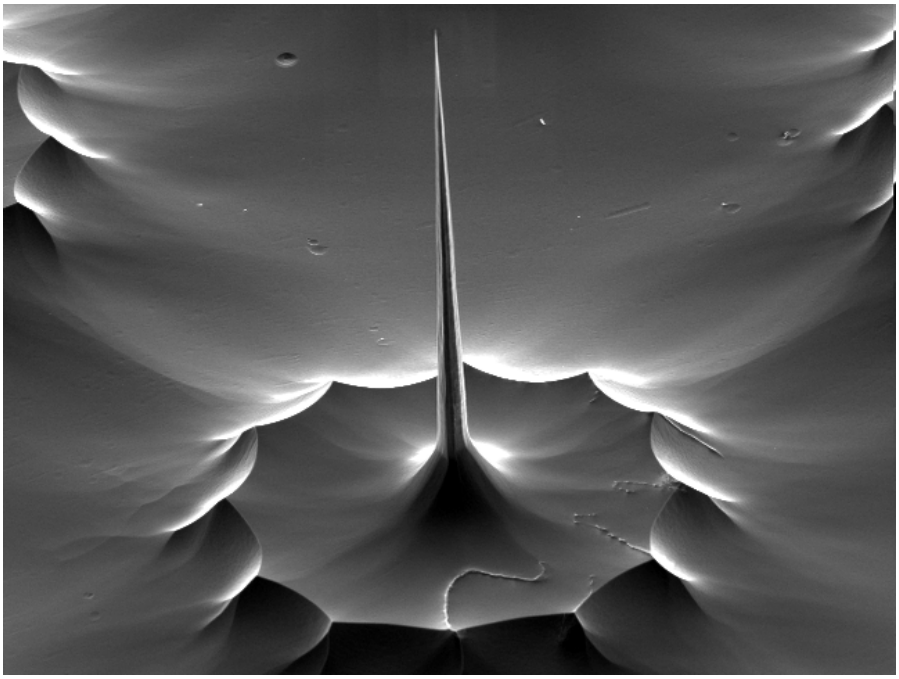


Figure 3.7: Sharp Needle. Picture by C. Schabmüller

## 3.3 Design of Flexible Silicon Micro-Needle-Devices

Figure 3.8 shows the scheme of the current flexible polyimide based interconnection, which is implantable and produced in the integrated process described above. It was presented by [HoHa01] and [ChSc02]. The main components are a larger silicon base, either a single silicon needle or an array of nine needles, and a connecting wire encased by two polyimide layers. This design allows the integration of further elements on the base needed for recording, such as amplifiers, battery, or memory.

The silicon needles are contacted through the aluminum wire, while the two polyimide layers provide a flexible insulation. The 135° bend reduces stress on the silicon base during the implantation and the long arms allow positioning of the base outside the brain area (see Figure 3.9).


Figure 3.8: Schematic of the flexible neural implant device

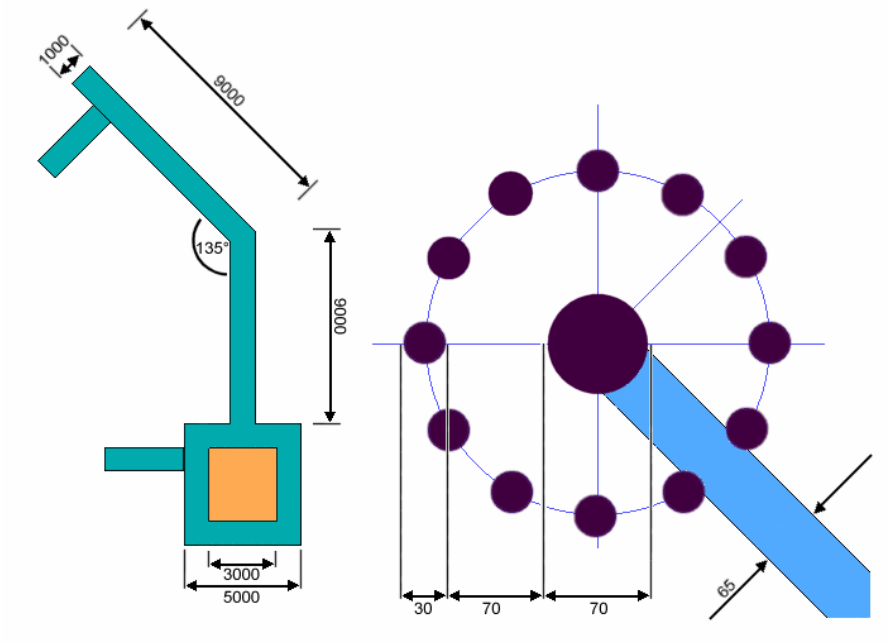



Figure 3.9: Layout of release trench with base (left) and contacted needle with protection pillars (right) (all units in µm).

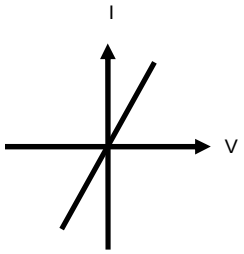
# 4 METAL TO SILICON MICRO-NEEDLE CONTACT

As discussed in section 3.2 the silicon needles are connected with an aluminum layer encapsulated by flexible polyimide films.

In this chapter this metal-to-semiconductor interface will be characterized by performing a general contact test with varying contact sizes. The main focus is to achieve an ohmic behavior of the contact. Therefore, the theory of doping, energy bands, and metal-to-semiconductor contacts will be discussed first.

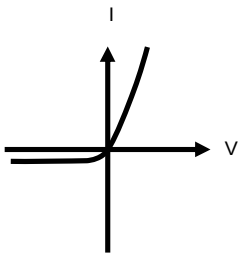
## 4.1 Metal-to-Semiconductor Junctions

In general, contacts should provide a low resistance connection between interconnected conducting materials. Metal-to-semiconductor junctions can form either rectifying (Schottky) or ohmic contacts. Contacts are referred as ohmic when their current-voltage characteristic exhibits a near-linear function in both directions of current flow. Non-ohmic, rectifying contacts are referred to as Schottky-contacts or barriers and find applications in IC devices, e.g. as diodes.



Ideal ohmic contact

Most metal-to-semiconductor junctions show non-ohmic characteristics, because the metal work function ($\Phi_M$) is greater than the semiconductor work function ($\Phi_S$). When metal and semiconductor materials are in contact at equilibrium (no current flow) the Fermi level must be constant through this system. If the work functions of the metal and the semiconductor are different, a potential-energy barrier exists between the connected materials at equilibrium. Assuming $\Phi_M > \Phi_S$ this height $\Phi_B$ is given by equation [4-1].



Rectifying contact (Schottky)

$$q\Phi_B = q(\Phi_M - \chi_S) \qquad [4\text{-}1]$$

Where q is the electronic charge, $\chi_S$ the electron affinity (4.05V for Si), and the work function for aluminum is $\Phi_M$=4.25V.

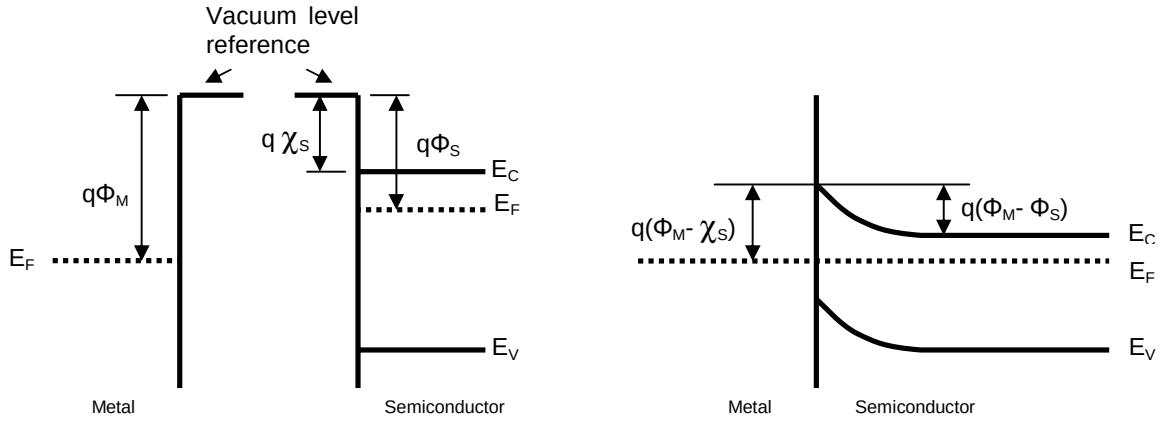



Figure 4.1: Energy band diagram of a metal-semiconductor contact with $\Phi_M > \Phi_S$ [WoTa86]

In order to create an ohmic contact between the metal and semiconductor, the impact of this barrier has to be negligible. Since there is no metal available showing a small barrier height when in contact with silicon, a simple ohmic metal-silicon-contact is not realizable.

To achieve ohmic behavior requires heavy doping of the semiconductor, thus carriers have energies greater than the barrier height and can get past the barrier by quantum-mechanical tunneling through it. To allow this process, the doping concentration $N_D$ has to exceed $10^{19}$ $cm^{-3}$.

Doping can be accomplished by different processes, e.g. gas phase diffusion or ion implantation. There are two different types of atoms suitable for doping:

- n-type or donor dopants contribute in general an extra electron to the crystal (e.g. phosphorus or arsenic (column V)).
- p-type or acceptors containing one fewer electron in their outermost shell compared to host semiconductor, causing a “hole” (e.g. boron or gallium (column III)).

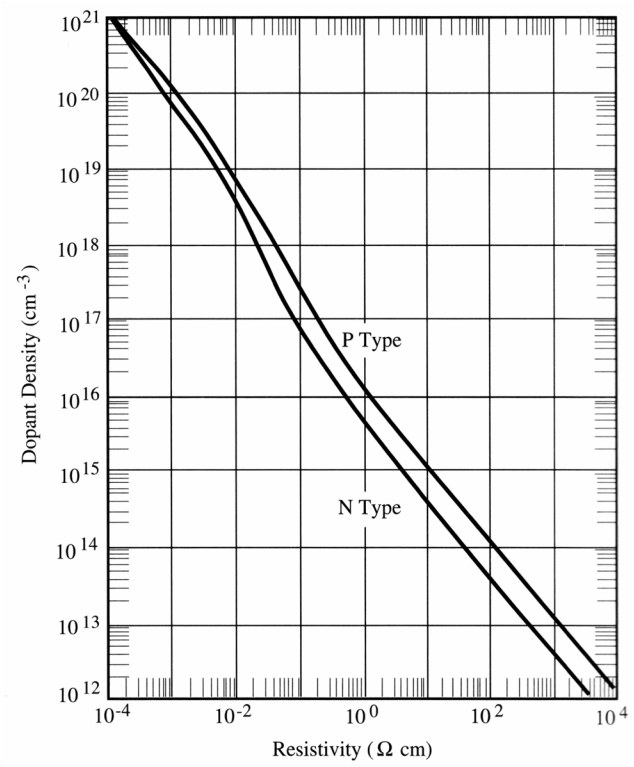



Figure 4.2: Resistivity versus doping for n- and p-type silicon [BeTs85]

Doping also has the big advantage that charge transport across the metal-to-semiconductor contact can be controlled by the doping concentration in the silicon.

The quality of a metal-to-semiconductor contact can be characterized by the specific contact resistivity, describing an incremental resistance of an infinitely small area, which is defined as:

$$\rho_c \equiv \left[\frac{\partial V_{MS}}{\partial J}\right]_{V_{MS}\,=\,0} \qquad [4\text{-}2]$$

Where J is the current density across the metal/semiconductor interface and $V_{MS}$ is the voltage across it. For tunneling contacts, the current density is given by:

$$J_S \propto \exp[-2x_d \sqrt{8\pi^2 m^* (q\phi_B - qV)/h^2}\,] \qquad [4\text{-}3]$$

Where h is Planck's constant and m* is effective mass of the tunneling carrier. The depletion layer $x_d$ through which the tunneling occurs is given by:

$$x_d = \sqrt{\frac{2\varepsilon_s \phi_B}{qN_D}} \qquad [4\text{-}4]$$

Where $\varepsilon_s$ is the permittivity and $N_d$ is the doping concentration of the semiconductor. Combining equations [4-3] and [4-4] into [4-2] leads to the contact resistivity for tunneling contacts:

$$\rho_c = \rho_{co} \exp\left(\frac{4\pi\phi_B\sqrt{m^* \varepsilon_s}}{h\sqrt{N_D}}\right) \qquad [4\text{-}5]$$

$\rho_{co}$ is a constant depending on the metal and the semiconductor. Equation [4-5] shows that the contact resistivity $\rho_c$ primarily corresponds to the reciprocal $\sqrt{N_D}$.

Aluminum, which belongs to group III of the periodic table, is the most common and important metal used for ohmic contacts for silicon [WoTa86]. To form low resistance contacts with silicon, it is necessary to remove any possible surface contaminations, especially the native oxide on the surface. This is usually done by a brief HF or BOE dip, followed by rinsing and drying immediately prior to the metal evaporation.

Depositing aluminum directly onto less heavily doped silicon ($N_D$ between $10^{19}cm^{-3}$ and $10^{16}cm^{-3}$), followed by a subsequent annealing step, low contact resistivities can still be observed as aluminum acts as a p-type dopant. This effect is created during the cooling phase of the annealing step, as the solid solubility of silicon in aluminum decreases with decreasing temperature and the aluminum becomes supersaturated with silicon. This causes the formation of silicon precipitates occurring at the Al:Si interface, consisting of p-type silicon, doped with aluminum to a concentration of $\sim 5 \cdot 10^{17} cm^{-3}$.

An annealing or sinter step is typically done at the end of the process in a diffusion furnace. Standard process temperatures are usually between 400-500°C for 10 to 30 minutes in presence of $H_2$ or in a forming gas ambient (5-10% $H_2$ and 90-95% $N_2$). The forming gas is needed because aluminum is, like many metals, sensitive to oxygen at higher temperatures. $H_2$ will passivate and deactivate interface traps.

In addition, the aluminum reacts with $SiO_2$ during the annealing, forming a thin layer of $Al_2O_3$ by reducing the native oxide and promoting a better adhesion between the silicon and the aluminum. As the aluminum reacts with the thin $SiO_2$ layer, the native oxide layer is eventually completely consumed. Thereafter, aluminum is still diffusing through the $Al_2O_3$ layer reaching the silicon surface and forming an intimate metal-to-semiconductor contact. This also means that if the native oxide layer is too thick, eventually not all of the $SiO_2$ will be consumed and a poor ohmic contact will result [WoTa86].

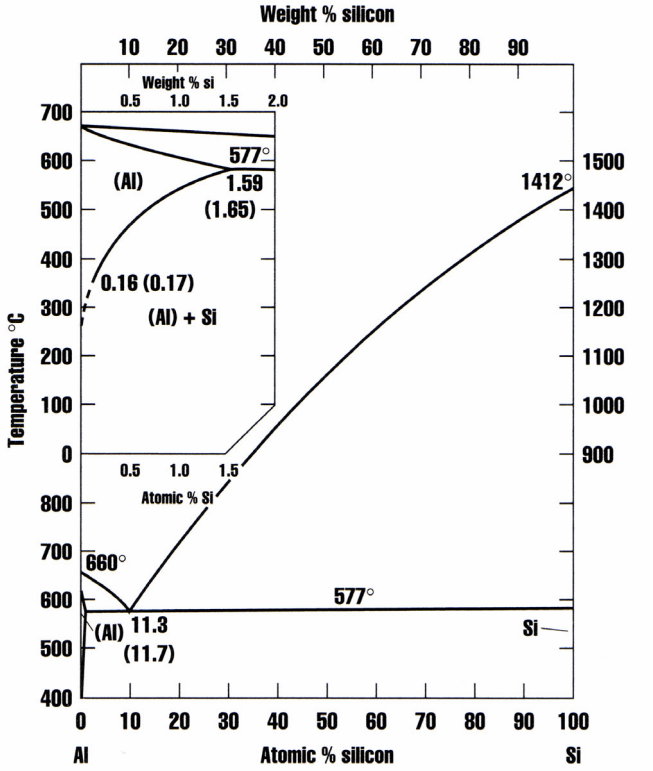



Figure 4.3: Phase diagram of Al/Si. Inset shows the low concentration region. [SACa96]

When using an annealing step for fabricating low resistance contacts, a counterproductive side effect has to be considered. As the inset of Figure 4.3 shows, the solubility of silicon in aluminum rises as the temperature increases. The silicon wafer will act as source and depending on the temperature, silicon will diffuse into the aluminum layer until the saturation concentration has been reached. Once the silicon is dissolved in the aluminum, it will be removed from the contact, evoking small long holes that will be filled up with aluminum. This

effect is referred to as junction spiking; spikes can penetrate into the wafer as deep as 1µm causing large leakage currents or even short circuits.

To prevent spiking liability at semiconductor contacts, an aluminum/silicon alloy is used. As the maximum process temperature is normally less than 500°C, adding 1% silicon is sufficient to exceed the silicon solubility and diffusion will no longer occur.

## 4.2 Contact Test

As discussed in the section above the quality of the ohmic contact between a metal and a semiconductor depends on a number of process parameters like doping concentration of the silicon wafer, native oxide layer, the deposited metal, a subsequent sintering or annealing step, as well as the contact geometry.

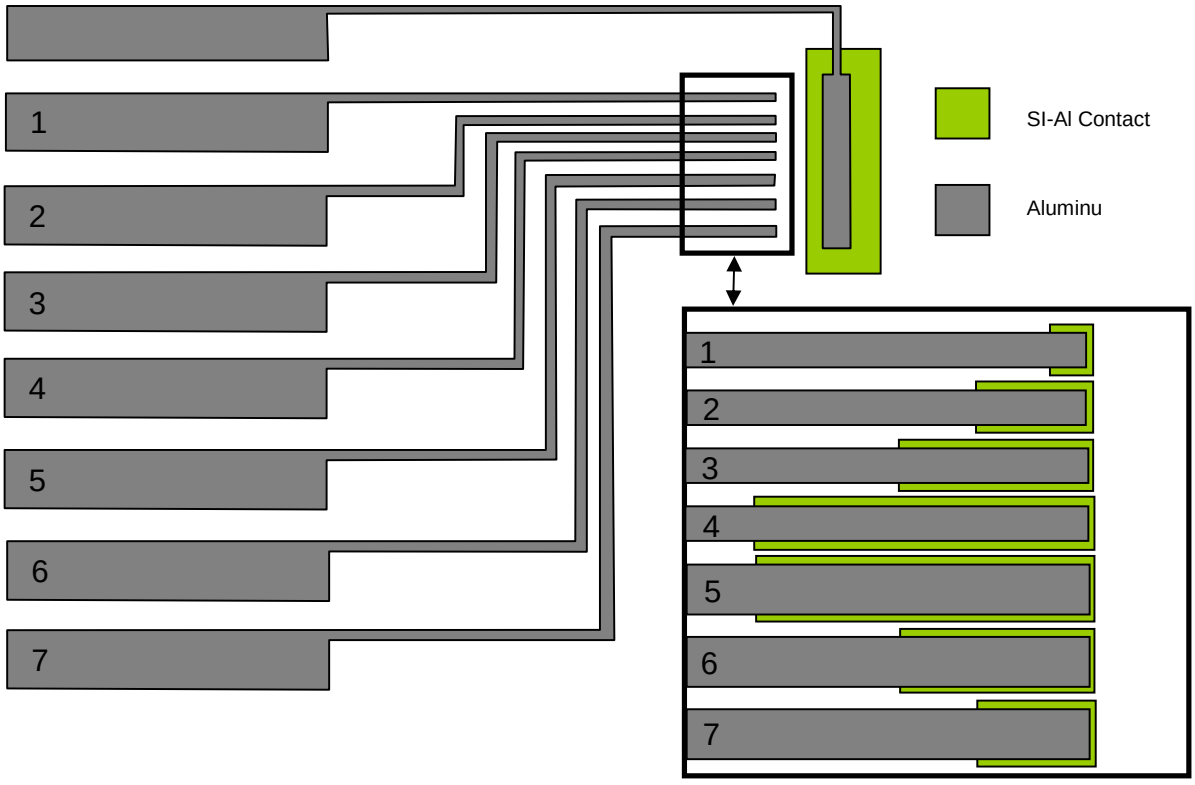



Figure 4.4: Design of the contact test

As it is very difficult to characterize just the contact between the aluminum wire and a silicon needle using a complete silicon micro-needle device, test devices were designed. The focus of the test was to determine how the resistance of the metal-to-semiconductor contact scales with the contact area, depending on the doping concentration of the silicon wafer.

For this reason tests were performed with wafers of different resistivities:

a) $\rho_{Si}$ =1-10 Ω·cm ~ $N_D \approx 10^{15}$ $cm^{-3}$

b) $\rho_{Si}$ =0.06 Ω·cm ~ $N_D \approx 10^{18}$ $cm^{-3}$

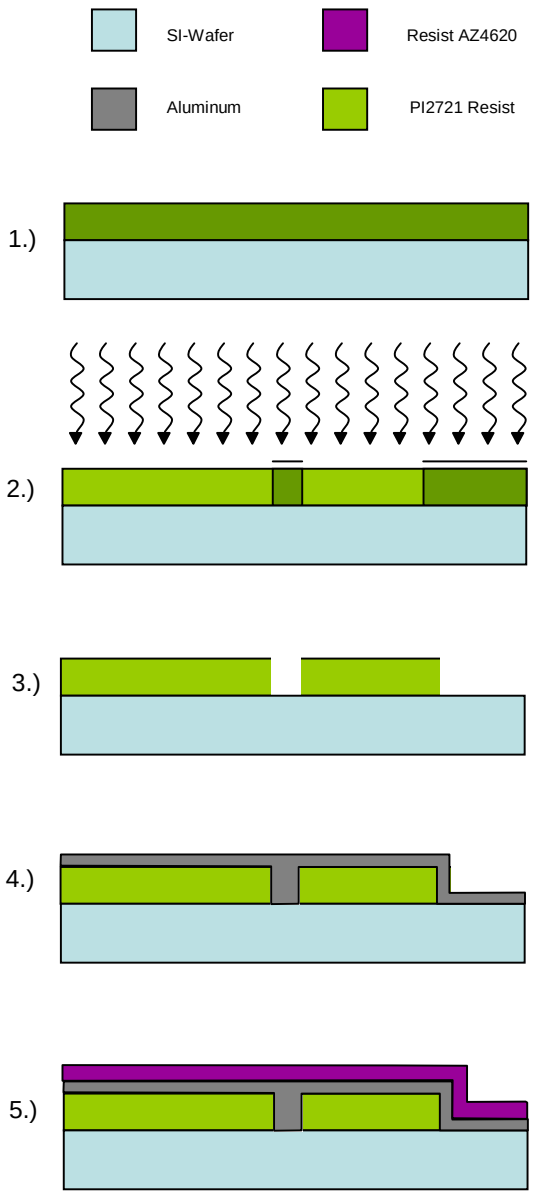
c) $\rho_{Si}$ =0.0007 Ω·cm ~ $N_D \approx 10^{20}$ $cm^{-3}$

Figure 4.4 shows the design of the contact test devices.

The fabrication process of the contact test devices is similar to the process described in section A.3, in order to transfer results easily. A complete step-by-step process listing can be found in section A.3.

First an 8µm thick polyimide layer was spun onto the wafer and patterned (Mask: PL-CT-POLY) for insulation and to define contact areas of varying sizes (steps 1-3).

A 7000Å thick aluminum layer was evaporated on top of the polyimide layer (step 4). To pattern the metal layer, photoresist AZ4620 was spun on and exposed using mask PL-CT-AL. Following a short hardbake the wafers were



immersed into an aluminum etch (step 5-8).

After stripping the photoresist, an annealing step using a furnace was performed (step 9). Times and temperatures of the curing step of the second polyimide layer of the original needle devices recipe have been used, in order to make the process of the contact test similar to fabrication of the needle devices.

For the testing, single devices had to be separated by using a dicing saw. To protect the devices during the dicing process a layer of resist AZ4620 was spun on the front side. The backside was covered with blue wafer tape (Step 10).

Striping the photoresist with acetone was the final step before the measurements (Step 11).

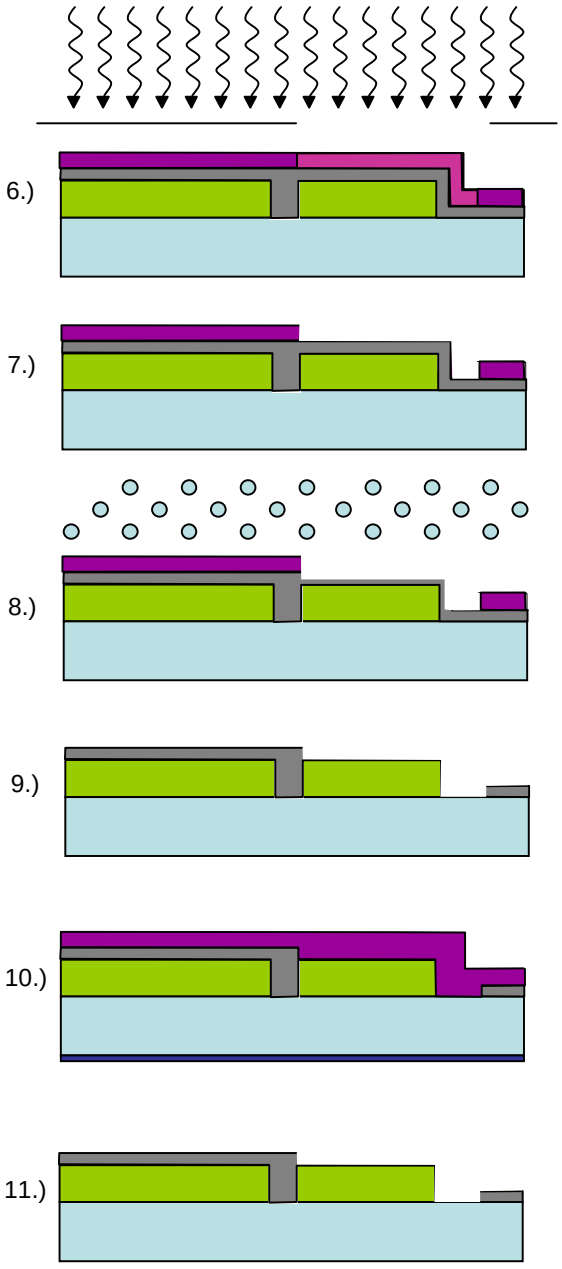



Figure 4.5: Contact Test Process

## 4.3 Contact Test Calculation

To estimate the seven different resistances $R_{tot}$, which depend on the varying metal to semiconductor contact sizes (see 4.2), the following model (Figure 4.6) has been used.

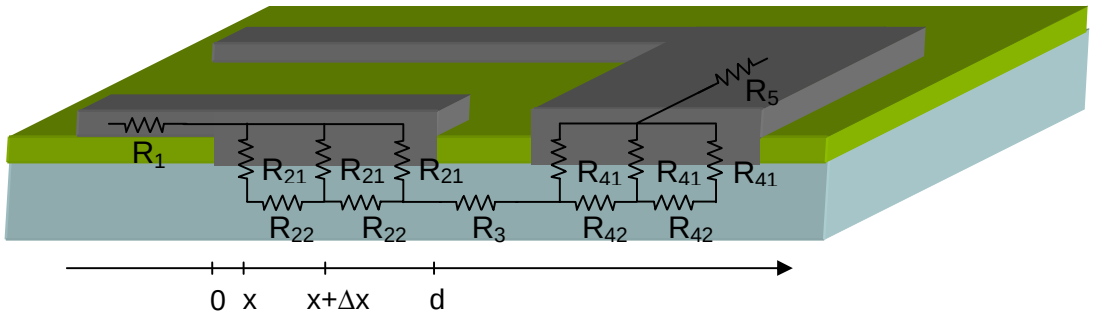



Figure 4.6: Resistance model for contact test

The resistances $R_1$ and $R_5$ of the circuit paths are uniform slabs of conducting material and can be expressed as:

$$R_1 = \frac{\rho L}{tW} \qquad [4\text{-}6]$$

Where ρ is the specific resistivity of the conducting material. For this contact test aluminum ($\rho_{Al}=2.65\cdot10^{-6}$ Ωcm) has been used. L is the conductor length, W is the conductor width and t is the thickness. $R_5$ can be calculated accordingly.

The contact resistance $R_2$ between the metal and semiconductor can be described by the resistive network of $R_{21}$ and $R_{22}$, slicing the contact areas into small sections with length $\Delta x$ (Figure 4.6). Accordingly, $R_4$ can be calculated using $R_{41}$ and $R_{42}$.

$R_{21}$ and $R_{22}$ are given by:

$$R_{21} = \frac{\rho_c}{W\Delta x} \qquad [4\text{-}7]$$

$$R_{22} = R_s \frac{\Delta x}{W} \qquad [4\text{-}8]$$

$R_s$ is the sheet resistance of the semiconductor layer and $\rho_c$ is the contact resistivity between the metal and semiconductor, which is defined under [4-2].

Applying Kirchoff's law, the relationships between voltages and currents at x and x+$\Delta$x can be found.

$$I(x+\Delta x) - I(x) = \frac{V(x)}{R_{21}} = \frac{V(x)W}{\rho_c}\Delta x \qquad [4\text{-}9]$$

$$V(x+\Delta x) - V(x) = I(x)R_{22} = \frac{I(x)R_s}{W}\Delta x \qquad [4\text{-}10]$$

By letting $\Delta$x approach zero, two differential equations for the current, I(x) and voltage, V(x) can be obtained:

$$\frac{dI}{dx} = \frac{V(x)W}{\rho_c} \qquad [4\text{-}11]$$

$$\frac{dV}{dx} = \frac{I(x)R_s}{W} \qquad [4\text{-}12]$$

Differentiating [4-11] and combining with [4-12] leads to:

$$\frac{d^2I(x)}{dx^2} = I(x)\frac{R_s}{\rho_c} = \frac{I(x)}{\lambda^2} \quad \text{with } \lambda = \sqrt{\frac{\rho_c}{R_s}} \qquad [4\text{-}13]$$

The parameter $\lambda$ describes the penetration length, i.e. the characteristic distance over which the current occurs under the metal contact.

Solving [4-13] with the initial values $I(0)=I_0$ and $I(d)=0$ the general solutions for I(x) is:

$$I(x) = I_0 \frac{\sinh\frac{d-x}{\lambda}}{\sinh\frac{d}{\lambda}} \qquad [4\text{-}14]$$

The general solution for V(x) can be found by integrating [4-12] and using [4-14]:

$$V(x) = I_0 \frac{\lambda R_s}{W} \frac{\cosh \frac{d-x}{\lambda}}{\sinh \frac{d}{\lambda}} \qquad [4\text{-}15]$$

The total resistance of the contact is then given by:

$$R_2 = R_4 = \frac{V(0)}{I(0)} = \frac{\lambda R_s}{W} \coth \frac{d}{\lambda} = \frac{\sqrt{\rho_c R_s}}{W} \coth \frac{d}{\lambda} \qquad [4\text{-}16]$$

As [4-16] shows, the contact resistance depends on the specific contact resistivity, the semiconductor sheet resistance and the contact geometry. For contacts with $d>>\lambda$ the coth becomes 1 and the contact resistance simply scales with the reciprocal contact width.

To determine the contact resistance, equation [4-5] can be written in the form:

$$\rho_c = \rho_{co} \exp\left(\frac{\phi_B C_1}{\sqrt{N_d}}\right) \qquad [4\text{-}17]$$

Where $C_1$ is $7.0 \cdot 10^{10}$ $cm^{-3/2}$ $eV^{-1}$ for silicon, $\Phi_{B,Al}$=0.6eV and $\rho_{co} = 1 \cdot 10^{-7}$ Ω cm² for a silicon–aluminum contact. As this equation can be only applied for tunneling contacts ($N_D > 10^{19} cm^{-3}$), the contact resistance for the wafers with $N_D \approx 10^{18} cm^{-3}$ was estimated based on the measurement results ($\rho_{c,18} = 7.6 \cdot 10^{-4}$ Ω cm² and $\rho_{c,20} = 6.7 \cdot 10^{-6}$ Ω cm²) [PDG00].

More information about contact resistance to a semiconductor can be found under [BVZe02].

Because of its nonrectangular shape, determining the resistance of $R_3$ requires a more elaborate calculation. Approximations for commonly used nonrectangular shapes can be found under [HeHo76]. In this case, Figure 4.7 has been used to estimate the resistance through the silicon:

$$R_3 \approx R_S \cdot k \qquad [4\text{-}18]$$

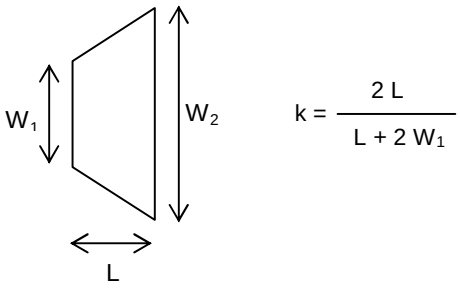



Figure 4.7: Resistance of nonrectangular shapes [HoDu83]

Where $W_1$ and $W_2$ are the widths of the two contact areas and L is the distance between the contacts.

After determining the single resistances, $R_{tot}$ is described by a serial connection network:

$$R_{tot} = R_1 + R_2 + R_3 + R_4 + R_5 \qquad [4\text{-}19]$$

## 4.4 Contact Test Measurement Results

The contact test measurements were accomplished using a Hewlett Packard Semiconductor Parameter Analyzer (HP 4145A). The voltage was increased from -0.5V to 0.5V in 0.01V steps with a compliant DC current of 40mA.

Information about the silicon wafers used for this contact test can be found at A.1.

A first test run was performed with wafers with $N_D \approx 10^{15}$ $cm^{-3}$ (resistivity 1-10 Ωcm) (Wafer 1). The results show a Schottky barrier, as expected.

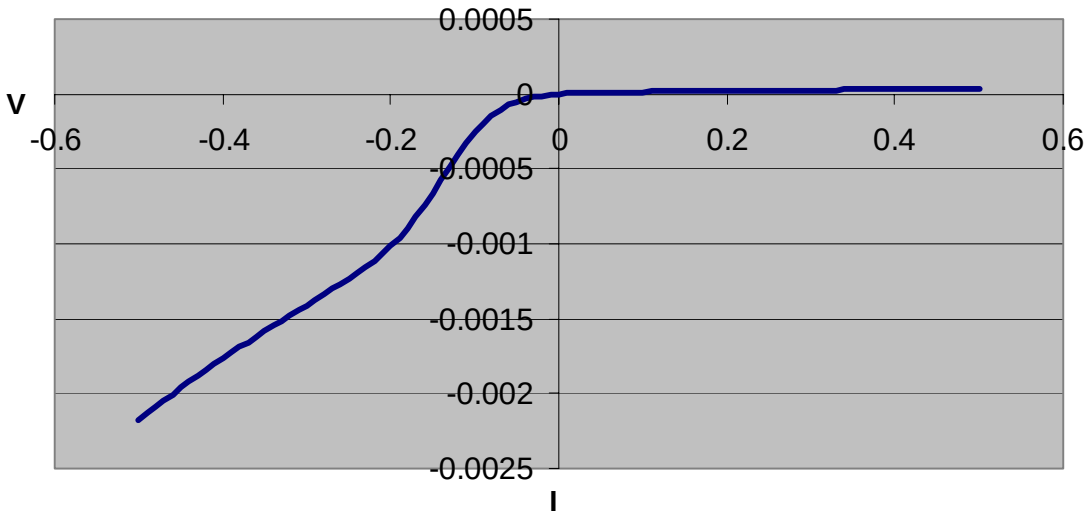



Figure 4.8: Contact test measurements of one contact for $N_D \approx 10^{15}$ $cm^{-3}$

Table 4-1 shows the anticipated ($R_{tot,C}$) and measured ($R_{tot,M}$) results of the contact tests using silicon wafers with two different doping concentrations ($N_D \approx 10^{18}$ $cm^{-3}$ (Wafer 2) and $N_D \approx 10^{20}$ $cm^{-3}$ (Wafer 3)). For the higher doped ones, wafers with $N_D \approx 10^{15}$ $cm^{-3}$ were doped with boron inside the furnace, therefore only a thin surface layer was highly doped. For these two tests, a linear ohmic behavior was observed.

$R_1$ and $R_5$ are added together because they vary only by the length of the circuit path.

| Contact size [µm²] | | 1<br>70·70 | 2<br>70·300 | 3<br>70·600 | 4<br>70·1200 | 5<br>140·1200 | 6<br>140·600 | 7<br>140·300 |
|---|---|---|---|---|---|---|---|---|
| Al contact on $N_D \approx 10^{18}$ cm$^{-3}$ | $R_{1\&5,C}$[Ω] | 6.07 | 6.43 | 6.81 | 7.19 | 7.23 | 11.13 | 11.47 |
| | $R_{2,C}$ [Ω] | 16.12 | 3.76 | 1.88 | 0.94 | 0.51 | 1.03 | 2.05 |
| | $R_{3,C}$ [Ω] | 1.97 | 1.97 | 1.97 | 1.97 | 1.46 | 1.46 | 1.46 |
| | $R_{4,C}$ [Ω] | 0.14 | 0.14 | 0.14 | 0.14 | 0.14 | 0.14 | 0.14 |
| | $R_{tot,C}$ [Ω] | **24.30** | **12.30** | **10.80** | **10.24** | **9.35** | **13.76** | **15.13** |
| | $R_{tot,M}$ [Ω] | **23.77** | **18.70** | **16.73** | **15.13** | **16.03** | **17.62** | **19.57** |
| Al contact on $N_D \approx 10^{20}$ cm$^{-3}$ | $R_{1\&5,C}$ [Ω] | 6.07 | 6.43 | 6.81 | 7.19 | 7.23 | 11.13 | 11.47 |
| | $R_{2,C}$ [Ω] | 1.87 | 0.44 | 0.22 | 0.11 | 0.09 | 0.18 | 0.36 |
| | $R_{3,C}$ [Ω] | 2.14 | 2.14 | 2.14 | 2.14 | 1.59 | 1.59 | 1.59 |
| | $R_{4,C}$ [Ω] | 0.04 | 0.04 | 0.04 | 0.04 | 0.04 | 0.04 | 0.04 |
| | $R_{tot,C}$ [Ω] | **10.11** | **9.05** | **9.20** | **9.48** | **8.96** | **12.94** | **13.46** |
| | $R_{tot,M}$ [Ω] | **11.18** | **11.08** | **11.27** | **11.46** | **11.15** | **13.42** | **13.58** |

Table 4-1: Anticipated and measured results for accomplished contact test with Wafer 2 & 3

As the graphical visualization illustrates (Figure 4.9 and Figure 4.10), the calculated values are close to the actual measurements. According to [PDG00] contact resistances are often found to be higher than expected. The difference between the results can be explained by the internal resistance of the measurement setup, the resistance of the native aluminum oxide layer, the initial condition of the silicon surface, segregation of dopants into the aluminum, and the inaccurate calculation and estimation of the contact resistivity.

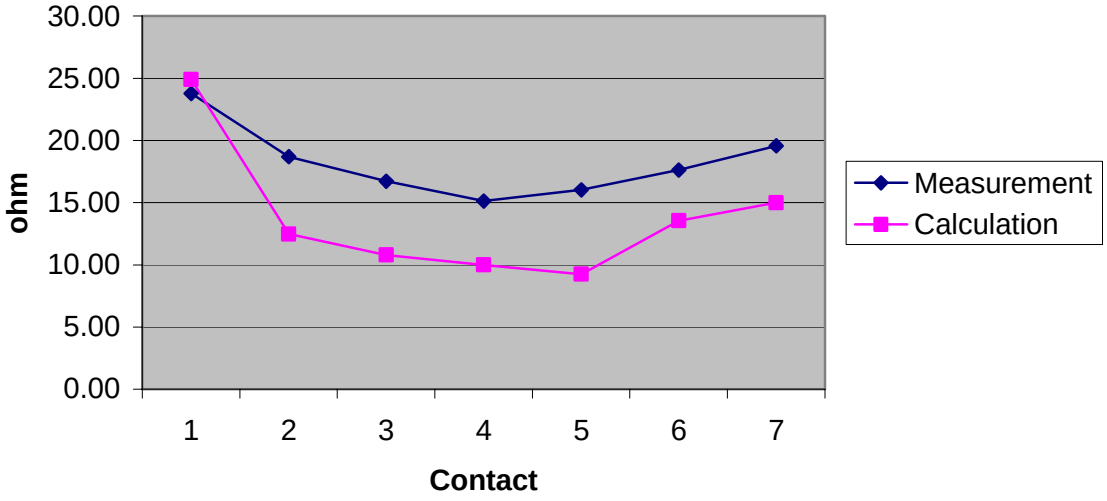



Figure 4.9: Contact test measurements and calculation for $N_D \approx 10^{18}$ $cm^{-3}$ (Wafer 2)

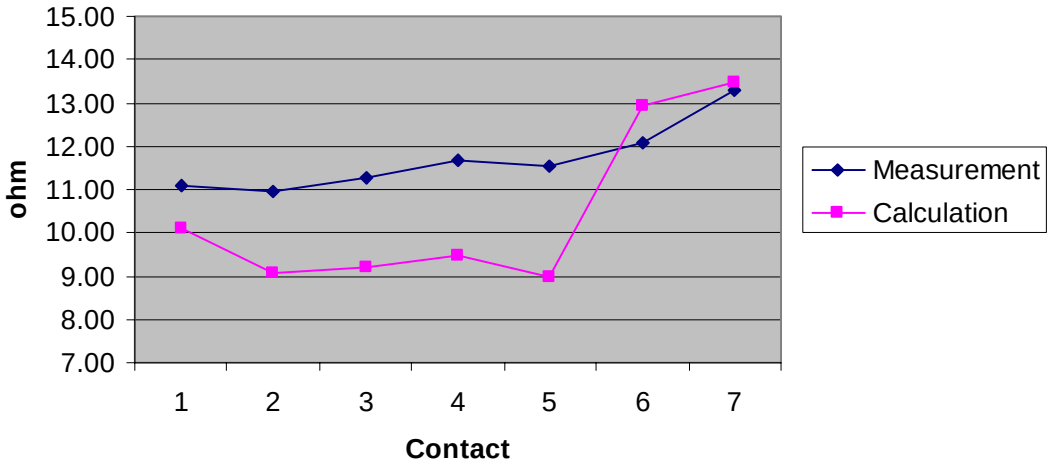



Figure 4.10: Contact test measurements and calculation for $N_D \approx 10^{20}$ $cm^{-3}$ (Wafer 3)

## 4.5 Transfer and Conclusions for Needle Devices

As discussed in this chapter, the quality of the aluminum to silicon contact depends on the doping concentration of the silicon wafer, removing the native silicon oxide prior to the deposition, a subsequent sintering or annealing step, and the contact geometry. Considering this, ohmic contacts were fabricated and characterized using highly doped p-type silicon wafers.

Table 4-2 summarized the properties of the wafers used in these contact tests.

| | Wafer 1 | Wafer 2 | Wafer 3 |
|---|---|---|---|
| Resistivity | 1 – 10Ωcm | 0.01 – 0.06Ωcm | ~0.0007Ωcm |
| Sheet resistance | ~180Ω/□ | 1.5Ω/□ | 1.63Ω/□ |
| Doping concentration | $N_D \approx 10^{15}\ cm^{-3}$ | $N_D \approx 10^{18}\ cm^{-3}$ | $N_D \approx 10^{20}\ cm^{-3}$ |
| Contact resistivity | - | $0.76 \cdot 10^{-3}\ \Omega cm^2$ | $0.67 \cdot 10^{-8}\ \Omega cm^2$ |
| $\lambda \left(\sqrt{\frac{\rho_c}{R_s}}\right)$ | - | 226µm | 64µm |

Table 4-2: Properties of the silicon wafers used for the contact test

Whether the resistance of the contact depends on the length and width of the contact area or only scales with the reciprocal contact width depends on the ratio of λ to the contact length (equation [4-16]). As the contacts for the needles are very small (65µm·65µm), the contact length has a big impact (factor 3.6) on the resistance for wafers like “wafer 2”. For wafers as heavily doped as “wafer 3”, the resistance scales primarily reciprocal to the contact width (factor 1.1).

Applying equation [4-16] the resistance of the needle contact (65µm·65µm) will be approximately 2.58 Ω (for wafers with $N_D \approx 10^{20}\ cm^{-3}$) and approximately 18.62Ω (for wafers with $N_D \approx 10^{18}\ cm^{-3}$).

The aluminum to silicon contact at the backside of the needles is only the first metal-silicon contact in the needle devices. As described in Chapter 6, for intracellular applications the very tip of the needle needs to be metallized with silver/silver chloride. As silver only forms an ohmic contact on wafers with a doping concentration exceeding $>N_D \approx 10^{19}$ $cm^{-3}$, on less heavily doped wafers ($N_D \approx 10^{16}$ $cm^{-3}$ to $N_D \approx 10^{19}$ $cm^{-3}$) an aluminum layer for the ohmic semiconductor-metal-contact needs to be evaporated first with silver on top. The characterization of this contact is, in principle, analogous to the approach described above; however, due to the geometry of the very tip, a more elaborate procedure will be required.

# 5 MODIFICATIONS AND PROCESS CHARACTERIZATION

In this chapter, modifications that have been made on the former needle device design and the former process presented by [HoHa01] and [ChSc02] are discussed, as well as process characterizations.

To understand and improve the fabrication process and the design of the needle devices, etch rates of each etch step must be known. Etch rates of many etchants for standard processes are commonly known and can be found in the literature. However, the used recipes for DRIE and RIE are specially developed for the needle process and are not standard recipes. Therefore, these etch steps have to be characterized.

## 5.1 Mask Layout Change

The former mask layout consisted of nine single needle devices on one 4'' wafer. They were arranged on a grid such that all devices could be diced out of the wafer, in order to sharpen one device at a time. As these pieces had different sizes, and they often did not remained at their position in the RIE chamber during the pumping, the time for the sharpening varied for every device. In addition, the required time varied depending on the previous position of the device on the wafer, due to the non-uniform etch rate of the DRIE, which decreases from the middle of the wafer towards the edge.

As the sharpening of single devices requires more handling and is very time-consuming, a more efficient way would be beneficial. The former grid layout was based on a process that required dicing for the release step. In the current process the devices are released during the sharpening step, therefore the layout does not need to be diceable anymore. To be able to sharpen more needles in a single step, the devices have been arranged on the wafer such that the needles of all devices are on one concentric circle, assuming that the etch rate is constant on the circle.

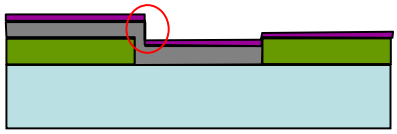
It has been observed that all needles on the circle have been etched uniformly by DRIE (uniformity on the circle 1.2%), as well as after the final RIE sharpening step no differences between the needles were observed under the SEM.

This change makes it also possible to process entire wafers after the sharpening for a future tip insulation process. The new mask layouts can be found at A.6.2.

## 5.2 Process Modifications

It has been found that due to the mask layout change described in the section above, no modifications to the fabrication process were required. However, the following changes have been applied to avoid problems, which had occurred during the previous fabrication process:

- During the fabrication of the contact test devices, the aluminum contact was disconnected at the polyimide to silicon step. The thin photoresist AZ1512 was not able to cover and protect the step during the aluminum etch. This was solved by changing from AZ1512 to the much thicker photoresist AZ4620 and a 5min hardbake at 120°C prior to the etch.



- After the DRIE etching the wafer is turned upside down for the polyimide and metallization processes. The polyimide and aluminum masks need to be carefully aligned to the needles. In the former process this was done by backside alignment with structures on the DRIE mask. As the DRIE structures are etched deep and the alignment structures are very small, the sidewalls of the alignment structures are not etched vertical, causing an insufficient resolution for alignment. For this reason, a special alignment mask has been added for backside alignment of the DRIE mask and for frontside alignment of the polyimide and aluminum masks. The alignment structures are etched 5µm deep by an $SF_6$ plasma in the RIE. By this, the alignment steps themselves were much easier and a higher quality of the alignment was achieved.
- By submerging the wafers into distilled water to wet them prior to the aluminum etch, a faster and more uniform etch of both aluminum and silver was observed.

- A hardbake of the DRIE mask (masking material photoresist AZ4620) for 30min at 120°C on the hotplate was added, as photoresist on wafers without post-develop bake tend to stick to the clamp ring in the DRIE and subsequently cannot be unloaded (compare WTC DRIE Operations).
- To avoid little gas bubbles inside the polyimide layer the polyimide has to be at room temperature when it is used. When it is cold, the viscosity is higher and bubble entrapment is more likely to occur. Therefore, the polyimide has to be taken out of the refrigerator, where it is normally stored, at least eight hours prior to use to warm it up.

  Small bubbles in the aluminum layer were observed after the second polyimide-curing step. They only occurred in areas where the metal layer was on top of the polyimide layer. In areas where the aluminum was evaporated directly onto silicon no bubbles were observed. As the former recipe used 350°C as final cure temperature for the first layer and 450°C as final cure temperature for the second layer, a possible explanation for these bubbles is that the first polyimide layer continued outgassing because of the higher temperature during the second curing step. Therefore, the gas was trapped by the aluminum layer and formed bubbles.

  According to [PI2720] 350°C is a sufficient final cure temperature. The second final cure temperature has to be higher than the first to promote better adhesion between the two polyimide films [HoHa01]. As the aluminum annealing step requires at least 400°C for 10min, the recipe was changed as shown in Figure 5.1. Therefore, the second final cure temperature is higher than the first to ensure good adhesion, and it is sufficient for annealing. Applying the new curing recipe, no more bubbles as well as no adhesion problems were observed.

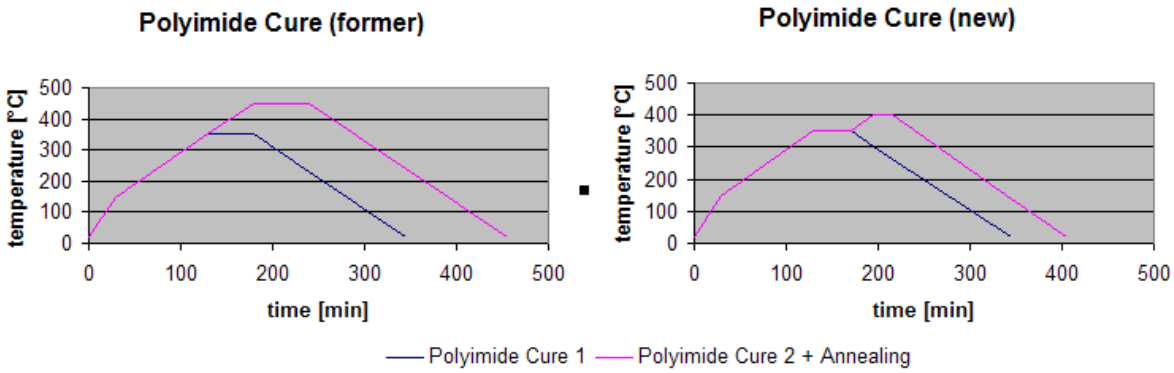



Figure 5.1: Polyimide Curing Recipes

## 5.3 Deep Reactive Ion Enhanced (DRIE) Etching

Together with an engineer from Oxford Instruments the following recipe for high aspect ratio etching using an Oxford Instruments DRIE (System 100) was developed to etch the pillars (Bosch Process):

| Deposition Step | | | | Etch Step | | | |
|---|---|---|---|---|---|---|---|
| Step Time: | 4 | Gas 1 ($SF_6$): | 1 | Step Time: | 7 | Gas 1 ($SF_6$): | 100 |
| Log Interval: | 1 | Gas 2: | 0 | Log Interval: | 1 | Gas 2: | 0 |
| | | Gas 3 ($C_4F_8$): | 100 | | | Gas 3 ($C_4F_8$): | 1 |
| | | Gas 4: | 0 | | | Gas 4: | 0 |
| Set pressure: | 15 | Set position: | 37 | Set pressure: | 20 | Set position: | 41 |
| RF Fwd Power: | 10 | ICP Fwd Power | 1250 | RF Fwd Power: | 25 | ICP Fwd Power | 1100 |
| Strike Pressure=DC Bias=Ramp Rate: | | | 0 | Strike Pressure=DC Bias=Ramp Rate: | | | 0 |
| Table Temp.: | 0 | Helium Backing | 7.00 | Table Temp.: | 0 | Helium Backing | 7.00 |

Table 5-1: DRIE recipe for high aspect ratio needles

The average etch rate of this recipe is about 2.1µm·min$^{-1}$ and good results of ~450µm tall pillars were achieved. The uniformity of the etch rate varied from the center of the wafer towards the edge, i.e. the difference between the trench depth measured at the top of the needle device compared to the depth at the bottom of the device was around 12%.

## 5.4 Needle Sharpening with Reactive Ion Enhanced (RIE) Etching

To form the needles out of the pillars, the devices were placed in an RIE (Trion) plasma etcher. An optimized recipe for this process, using $SF_6$ as a reaction gas, required ~25min for the sharpening of single devices on a diced silicon piece. With the new mask layout, entire wafers were placed inside the RIE chamber, increasing the process time to ~75min. This is due to the so-called loading effect, i.e. the etch rate depends on the area of exposed surface. It is caused by a significant depletion of the etchant species in the plasma phase due to consumption during the etching process. This effect makes it difficult to predict etch rates of a given process when the size and the number of samples varies from run to run.

To release the needle devices, the remaining silicon inside the trench has to be etched away during the same period as the needles are sharpened. To adjust the remaining thickness during the DRIE etching, the etch rate of silicon during the RIE has to be known.

As during the sharpening step the entire wafer is exposed and the loading effect has to be considered, the etch rate test has been accomplished with a blank, unpatterned silicon wafer.

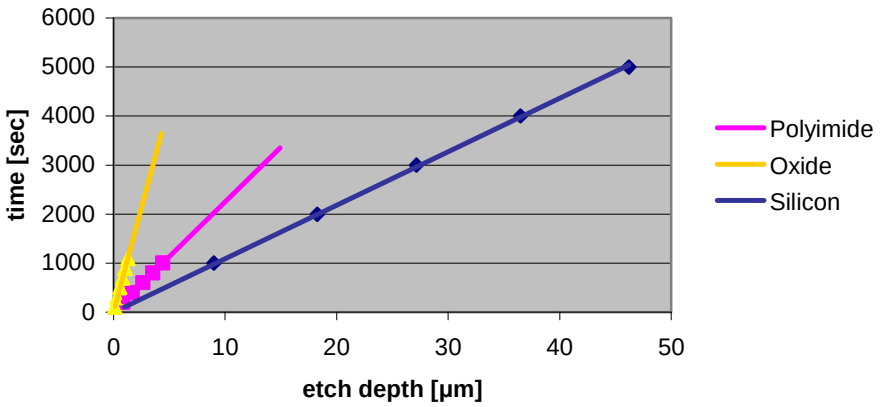



Figure 5.2: RIE etch rates of polyimide, oxide and silicon with SF6

Figure 5.2 shows the result: the determined etch rate of silicon is 0.6µm·min$^{-1}$, therefore the remaining thickness has to be 45µm assuming 75min for the sharpening process.

As mentioned in section 5.3, the DRIE etch rate is not uniform, i.e., the remaining thickness of the release trench becomes higher towards the edge of the wafer. Therefore, during the RIE sharpening, the device is already released around the needle while there is still silicon left at the base of the device. While the remaining silicon is etched away, polyimide is exposed to $SF_6$ in areas that are already released. As the etch rate test for polyimide shows, $SF_6$ attacks polyimide with an etch rate of 0.25µm·min$^{-1}$, therefore the selectivity between silicon and polyimide is ~2.4. (for polyimide no loading effect was observed). Therefore, to protect the polyimide an etch stop layer is required.

Etch rate tests with aluminum masks have shown that aluminum is not attacked by $SF_6$ and therefore is a suitable material for an etch stop layer. As aluminum is also used for contacting the needles, a direct contact between the aluminum etch stop layer and the aluminum contact has to be avoided. Therefore, a gap between the contact area and the etch stop layer is required, but in this gap polyimide will be exposed to $SF_6$.

To avoid this gap, oxide was tested as an etch stop layer material. The etch rate of oxide with $SF_6$ has been determined as 0.07µm·min$^{-1}$, therefore the selectivity between silicon and oxide is ~9. Whether oxide is suitable as an etch stop layer or not depends on the uniformity of the DRIE etch rate, the silicon etch rate and the thickness of the oxide layer. The maximum thickness of an oxide layer is about 2µm, therefore the oxide layer lasts for about 30min when attacked by $SF_6$. If the uniformity of the DRIE etch rate is not greater than 4%, an oxide layer would be suitable as an etch stop layer. For non-uniformities exceeding 4%, oxide is not a sufficient etch stop layer. This can be expressed by the following equation:

$$y = \frac{\text{oxide thickness}}{\text{etchrate oxide}} - \frac{\text{DRIE etch depth} \cdot \text{uniformity}}{\text{etch rate silicon}} \qquad [5\text{-}1]$$

For y<0 the oxide layer is not a sufficient etch stop layer, for y>0 the layer is sufficient.

As equation [5-1] shows, the release step would be also improved by increasing the silicon etch rate. As this etch rate shows a strong loading effect in the RIE, it could be increased by using a mask. An etch rate test, using an aluminum mask showed an etch rate of 2.7µm·min$^{-1}$. In the current recipe, the oxide etch stop layer grown in the oxidation furnaces

on both sides of the wafer is only used on the front side and completely etched away on the backside. Instead of completely removing the oxide layer on the backside, this layer could be patterned and used as a mask.

# 6 TIP METALLIZATION

The overall goal of the current study is the fabrication of sharp silicon needles suited for intracellular recording from brain cells of freely behaving animals, e.g. Tritonia diomedea – a sea slug. For this reason, the intracellular probes need to be long (>300µm) with extremely sharp tips (<1µm) for effective bending and penetration of the flexible cell membrane. In order to observe the electrical activity of one single neuron, only the very tip (5-10µm) of the needle, which is inside the cell, should be conducting. The rest of the needle must be insulated from the electrolyte outside the cell with a dielectric layer. With sputtered silicon nitride high quality passivation layers were produced [HaBö02].

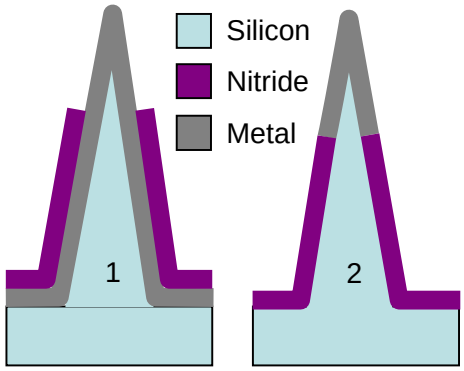
In addition, possible instabilities, noise sources, and bio-fouling have to be considered. The stability of the tip can be improved by covering it with a metal. To date most stable results have been achieved with silver-silver chloride electrodes [LAGe72]. Silver can be evaporated and chlorided in a post process.

More information about intracellular recording can be found in “Towards MEMS Probes for Intracellular Recording” by Y. Hanein et al. [HaBö02].

## 6.1 Concept and Fabrication Process

There are two major possible methods of insulating the needle:

1. to evaporate the metal layer first and then sputter the nitride on top
2. to sputter the nitride first, remove it at the tip and then evaporate the metal




As the picture shows, the first method has the disadvantage that the metal layer will not be completely covered at the bottom of the needle and signals from the outside of the cell will also be recorded.

For this reason, a process was developed using the second method, sputtering silicon nitride on the needle first. As the needle is positioned inside the release trench, the basic idea is to fill up the trench with photoresist, expose and develop it, so that only the tip is not covered with resist. Then the nitride is etched away and the metal evaporated.

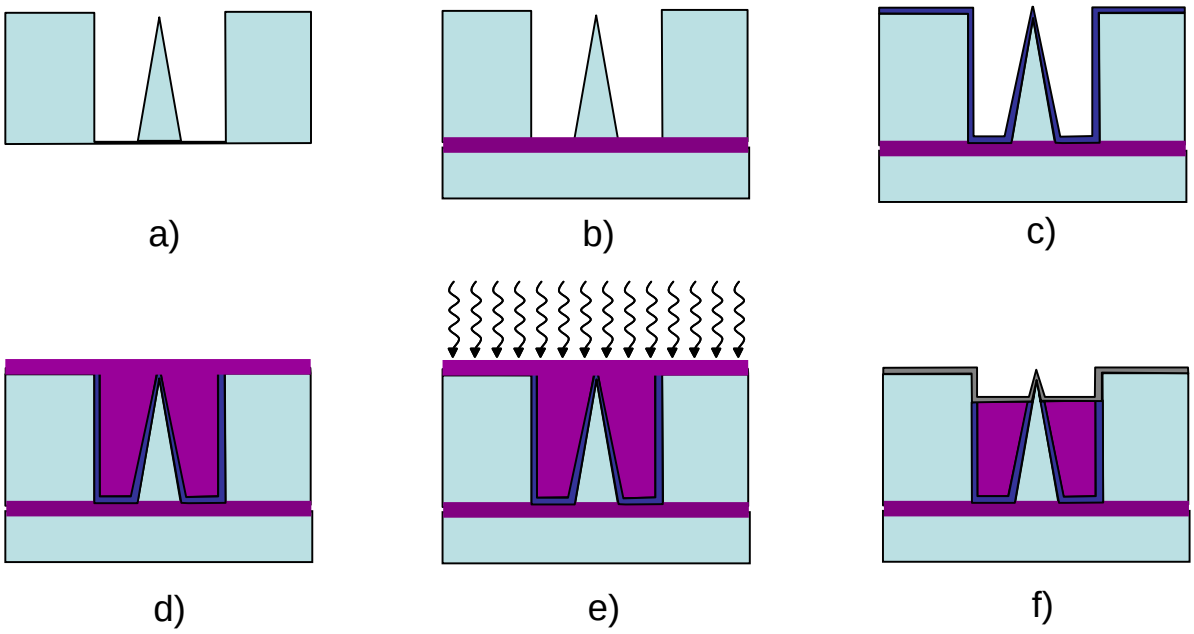



Figure 6.1: Tip Metallization Concept

To prove this concept, only the metallization of the tip was done without the insulating silicon nitride layer. For this, the device needs to remain inside the trench after the RIE sharpening and release step. To accomplish this, the device wafer was coated with photoresist AZ4620 and a sacrificial wafer was attached on the device side. To ensure good adhesion and complete out-gassing, the wafers were hardbaked inside a vacuum oven for 60min at 100°C.

For filling up the trenches, different tests were done with AZ1512 and AZ4620. The resist was spun on using the CEE Photoresist Spin Coater only with an eight second spread step at 800rpm / 650 $r \cdot s^{-1}$, followed by a softbake at 70°C for 7min and a hardbake at 95°C for 7min. Due to the small dimensions of the trench, surface tension causes a non-uniform fill. For this

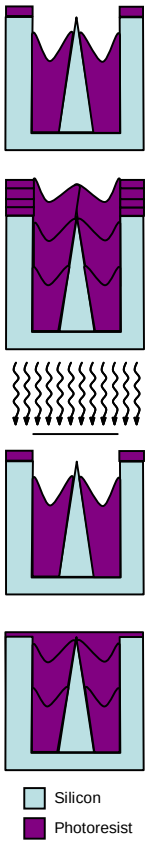
reason, the trench needs to be completely filled up with photoresist to overcome the surface tension.

Since the photoresist shrinks during the baking, the trench must be refilled 4-5 times, to ensure that is completely filled with photoresist. It has been observed that trenches can be filled with the thicker AZ4620 in significantly less steps compared to the AZ1512.

As the resist layer on top of the wafer gets thicker with every fill up step as well, the handling of the wafer becomes more and more difficult. Therefore, mask PL-ND-TIP has been used to expose and develop away the photoresist on top of the wafer. After the exposure of 80sec the resist is developed for ~20min.

When the trench was completely filled, the wafer was briefly exposed to UV-light (4sec) and the upper resist layer was developed away, leaving only the very tip uncovered. In order to control this parameter of tip insulation, further research is required of exposure and development times.

After a brief HF dip for 30sec to clean residues and to remove the native oxide layer, the metal layer (~1000Å of aluminum) can be evaporated. The final lift-off was done with acetone.




## 6.2 Results

The following SEM pictures illustrate the results of the first test run. As described above, only the fill up and metal evaporation steps were performed. For test purposes the tips were not completely sharpened. The shiny areas at the tip of the needles are where the aluminum was deposited by thermal evaporation. This shows that this method can be used for tip metallization.

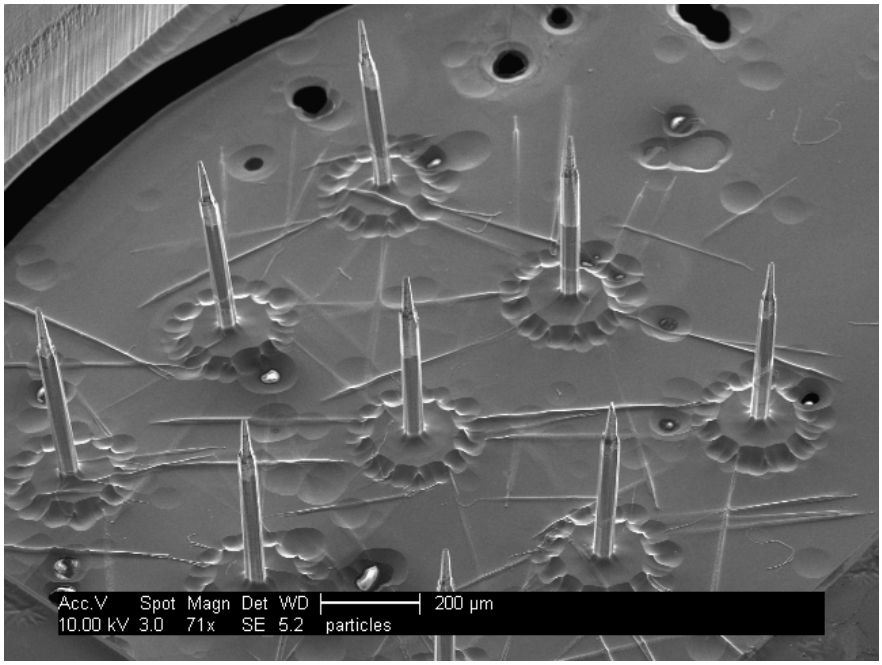



Figure 6.2: Tip Metallization

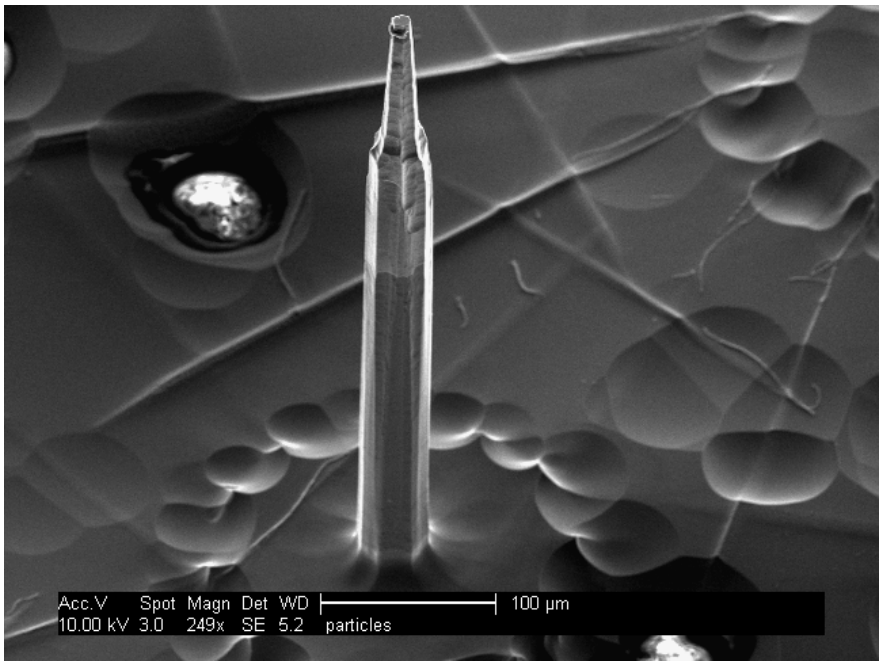



Figure 6.3: Tip Metallization

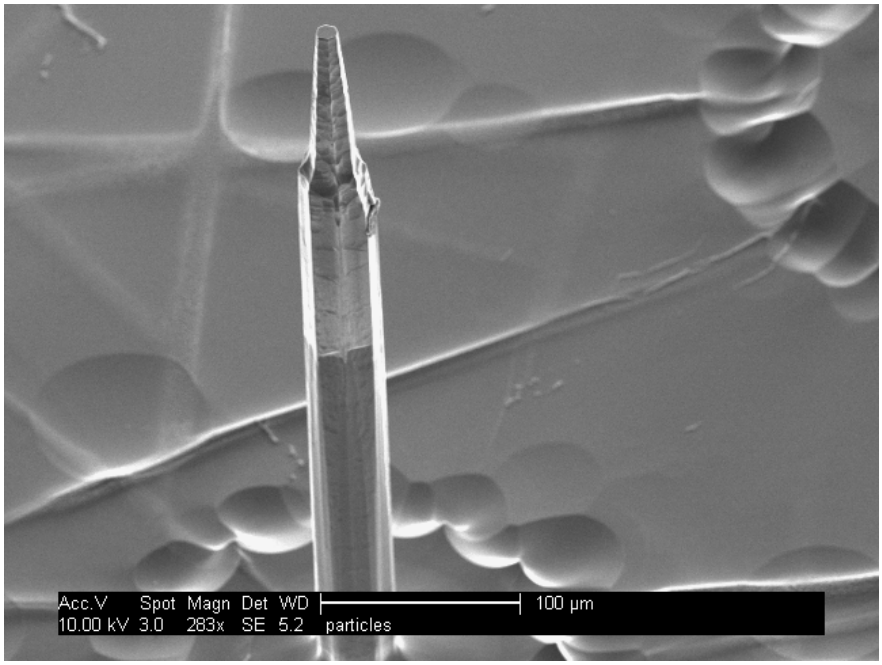



Figure 6.4: Tip Metallization

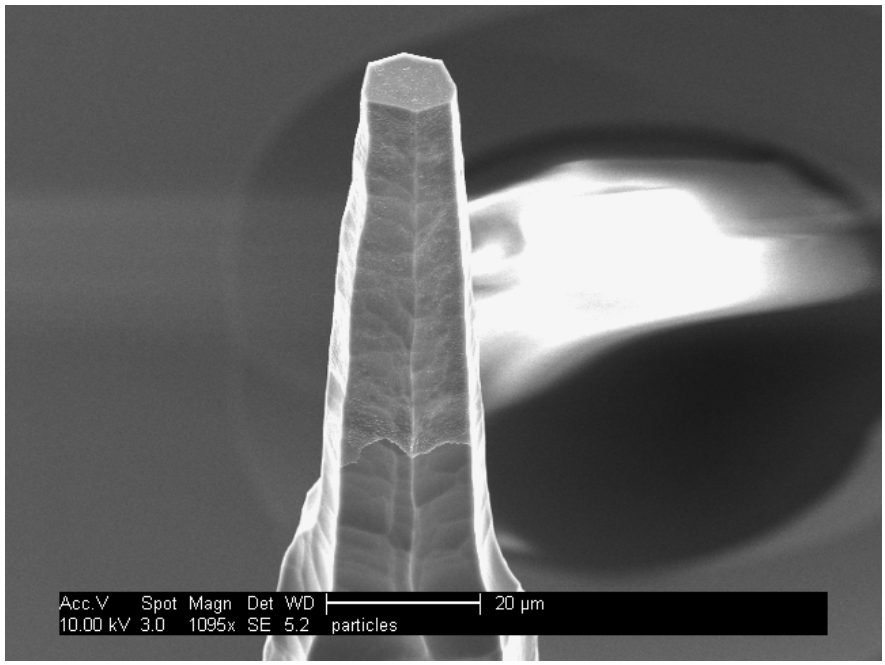



Figure 6.5: Tip Metallization

# 7 SUMMARY

In summary, a new improved fabrication process of the silicon micro-needle devices with flexible polyimide interconnects of the UW MEMS lab was presented and documented.

It was shown that by choosing highly doped silicon wafers good ohmic contacts between the needle electrode and the connecting aluminum wire can be achieved.

A new mask layout, arranging the needles of all devices on a circle concentric with the wafer was developed and successfully tested. This new layout will help to reduce the handling and fabrication times of the devices. Further changes to improve the process were successfully applied. The RIE sharpening of the needles was characterized by performing a number of etch rate tests.

Finally, a new method was presented for insulating the needle base and metallizing the very tip. This was a milestone of the long term goal of this research project, to build stand-alone, implantable sensing units, suitable for intracellular recording from freely behaving animals.

Further research is required for characterizing this new method in order to control the length of the tip metallization in a 5-10µm range. In addition, stabilizing the DRIE process in order to obtain pillars with positive profile is the goal for the near future.

# A APPENDIX

## A.1 Silicon Wafer for Contact Test

| | | | | |
|---|---|---|---|---|
| Wafer 1: | Supplier: | International Wafer Service (http://www.siwafer.com) | | |
| | Diameter: | 100.0mm, 4inch | Orientation: | <100> |
| | Type/Dopant: | P/B | Resistivity: | 1 – 10 ohm–cm |
| | | Double Side Polished | Thickness: | 500 – 550µm |
| | | Semi STD Flats | Growth Method: | CZ |
| | | Slice Alignment | | |

| | | | | |
|---|---|---|---|---|
| Wafer 2: | Supplier: | Virginia Semiconductor, Inc. (http://www.virginiasemi.com) | | |
| | Diameter: | 100.0mm, 4inch | Orientation: | <100> |
| | Type/Dopant: | P/B | Resistivity: | 0.01 - 0.06 ohm–cm |
| | | Double Side Polished | Thickness: | 375µm |
| | | Semi STD Flats | Growth Method: | CZ |
| | | Slice Alignment | | |

Wafer 3: Wafer 1 wafers doped with boron solid source wafers (BN-975 and BN-HT from Carborundum Inc.) inside an atmospheric furnace.

| | | | |
|---|---|---|---|
| Type/Dopant: | P/B | Resistivity: | ~0.0007Ωcm |

## A.2 Needle Process Listing

### Wafer Preparation / Cleaning

1. Labeling wafers
    - ☐ Scribe code and numbers on wafer: PL-ND-1…
2. Wafer Cleaning (Piranha 4:1 – $H_2SO_4$:$H_2O_2$)
    - ☐ Label: date, time, name, phone number, chemicals/mixture
    - ☐ Wear protective equipment: face shield, heavy latex gloves, heavy acid apron
    - ☐ Use dedicated labeled glass beaker inside labeled white container
    - ☐ Measure 800ml $H_2SO_4$
    - ☐ Slowly pour 200ml $H_2O_2$ from graduate cylinder (CAUTION: exothermic reaction)
    - ☐ Immersion wafers into piranha solution using Teflon boat for 15min
    - ☐ Transfer to dunk tank and allow 3-cycle rinse
    - ☐ Place Teflon boat with wafers into Spine Rinse Drier
    - ☐ Allow piranha solution to cool down
    - ☐ Use the aspirator tube located in the Microvision wet bench to aspirate the solution

### Lithography for Alignment

- ☐ Transfer wafers to dedicated metal cassette and load into wafer priming oven (HMDS vapor) at 150°C for 30min

1. blanket cover for back side
    - ☐ Spread: 500 rpm, 125 r/sec, 5 sec; Dry: 3000 rpm, 500 r/s, 30 sec
    - ☐ Dispense AZ1512 resist onto wafer
    - ☐ Prebake wafer directly on hotplate for 5min at 110°C
2. front side for Alignment
    - ☐ Spread: 500 rpm, 125 r/sec, 8 sec; Dry: 1500 rpm, 750 r/s, 40 sec
    - ☐ Dispense P-10 Wafer
    - ☐ Dispense AZ4620 resist onto wafer

- ☐ Prebake wafer directly on hotplate for 5min at 70°C and for 5min at 95°C

3. ABM IR aligner (reservation required)
   - ☐ Fill out log sheet
   - ☐ Load mask PL1-AG and wafer
   - ☐ Expose two steps 10.0sec and 9.0sec
4. Development
   - ☐ Add 100ml AZ400K developer to 400ml H2O in dedicated glass beaker (4:1 – H2O:AZ400K)
   - ☐ Load wafer into Teflon boat and immerse under agitation for 2-3min
   - ☐ Transfer to dunk tank and allow 3-cycle rinse
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier
   - ☐ Used AZ developer can go down the sink drain

**Reactive Ion Etching for Alignment**

1. TRION RIE (reservation required)
   - ☐ Run “Clean”
   - ☐ Etch wafer 5µm deep
     - Parameter:

| | | | | |
|---|---|---|---|---|
| Pressure Set: | 200 | Oxygen Set: | 0 |
| RF Power Set: | 125 | CHF3 Set: | 0 |
| Endpoint Set: | 100 | SF6 Set: | 100 |
| Process Time Set: | 90 sec | | 0 |
| Temperature: | 300 | | 0 |
| Base Pressure Set: | 150 | | 0 |

2. Resist strip
   - ☐ Fill out log file for barrel asher
   - ☐ Load wafers in dedicated quartz boat for asher
   - ☐ Barrel asher with $O_2$-plasma for 10min
   - ☐ EKC for 10min at ~60°C
   - ☐ AZ300T for 10min at ~75°C
   - ☐ transfer to dunk tank using Teflon boat and allow 3-cycle rinse

- ☐ Place Teflon boat with wafers into Spine Rinse Drier

**Batch split: Oxide or Aluminum as Etch-Stop-Layer**

**Etch-Stop-Layer Aluminum**

1. Al evaporation
   - ☐ Fill out log file
   - ☐ Density Aluminum: 2.69
   - ☐ Evaporate Al (99%Al, 1%Si) 30nm thick (~300Å)
2. Lithography for front side
   - ☐ Spread: 500 rpm, 125 r/sec, 5 sec; Dry: 3000 rpm, 500 r/s, 30 sec
   - ☐ Dispense AZ1512 resist onto wafer
   - ☐ Prebake wafer directly on hotplate for 3min at 90°C
3. ABM IR aligner (reservation required)
   - ☐ Fill out log sheet
   - ☐ Load mask PL1-Etchstop and wafer
   - ☐ Expose 3.0sec
4. Development
   - ☐ Add 100ml AZ351 developer to 400ml H2O in dedicated glass beaker (4:1 – H2O:AZ351)
   - ☐ Load wafer into Teflon boat and immerse under agitation for 50~60sec
   - ☐ Transfer to dunk tank and allow 3-cycle rinse
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier
   - ☐ Used AZ developer can go down the sink drain
5. Al Etch
   - ☐ Hardbake wafers on hotplate for 5min at 120°C
   - ☐ Heat Al-etch to 40°C
   - ☐ Wet wafers with DI-water and immerse under agitation

- ☐ Transfer to dunk tank and allow 3-cycle rinse
- ☐ Place Teflon boat with wafers into Spine Rinse Drier
- ☐ Use the aspirator tube located in the Microvision wet bench to aspirate the used Al Etch solution

6. Strip resist
   - ☐ Fill out log file for barrel asher
   - ☐ Barrel asher with $O_2$-plasma for 10min
   - ☐ EKC for 10min at ~60°C
   - ☐ AZ300T for 10min at ~75°C
   - ☐ transfer to dunk tank using Teflon boat and allow 3-cycle rinse
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier

**Etch-Stop-Layer Oxide**

1. Oxidation (reservation required, process time 12h)
   - ☐ Fill out log sheet
   - ☐ Place wafers surrounded by dummy wafers into dedicated boat
   - ☐ Check water-level
   - ☐ Parameter Tube #2 for ~1.6µm Oxide:

| Seg Type | Time | Target | N2 Sol | N2 SP | O2 Sol | O2 SP | N2/H2 Sol | N2/H2 SP | N2BP Sol |
|---|---|---|---|---|---|---|---|---|---|
| Time Target | 2.0 | 25 | open | 60.0 | closed | 0.0 | closed | 0.0 | closed |
| Ramp Rate | 10.0 | 1150 | open | 60.0 | closed | 0.0 | closed | 0.0 | closed |
| Dwell | 360.0 | 0 | open | 30.0 | open | 10.0 | closed | 0.0 | closed |
| Dwell | 10.0 | 0 | open | 60.0 | closed | 0.0 | closed | 0.0 | closed |
| Dwell | 360.0 | 0 | open | 30.0 | open | 10.0 | closed | 0.0 | closed |
| Ramp Rate | 3.0 | 25 | open | 60.0 | closed | 0.0 | closed | 0.0 | closed |
| End | XXX | 0 | closed | 0.0 | closed | 0.0 | closed | 0.0 | open |

   - ☐ Refill water after 3600min
2. Lithography for front side
   - ☐ Spread: 500 rpm, 125 r/sec, 5 sec; Dry: 3000 rpm, 500 r/s, 30 sec

- ☐ Dispense AZ1512 resist onto wafer
- ☐ Prebake wafer directly on hotplate for 3min at 90°C

3. ABM IR aligner (reservation required)
   - ☐ Fill out log sheet
   - ☐ Load mask PL1-Etchstop and wafer
   - ☐ Expose 3.0sec
4. Development
   - ☐ Add 100ml AZ351 developer to 400ml H2O in dedicated glass beaker (4:1 – H2O:AZ351)
   - ☐ Load wafer into Teflon boat and immerse under agitation for 50~60sec
   - ☐ Transfer to dunk tank and allow 3-cycle rinse
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier
   - ☐ Used AZ developer can go down the sink drain
5. Oxide Etch with BOE
   - ☐ Hardbake wafers on hotplate for 3min at 120°C
   - ☐ Wear protective equipment: face shield, heavy latex gloves, heavy acid apron
   - ☐ Load wafer into Teflon boat and immerse under into BOE (10:1) for 40min
   - ☐ Transfer to dunk tank and allow 3-cycle rinse
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier
6. Strip resist
   - ☐ Fill out log file for barrel asher
   - ☐ Load wafers in dedicated quartz boat for asher
   - ☐ Barrel asher with O2-plasma for 10min
   - ☐ Load wafer into Teflon boat and immerse into Acetone for 5min
   - ☐ transfer to dunk tank using Teflon boat and allow 3-cycle rinse
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier

**Lithography for DRIE**

1. blanket cover for front side

- ☐ Spread: 500 rpm, 125 r/sec, 5 sec; Dry: 3000 rpm, 500 r/s, 30 sec
- ☐ Dispense AZ1512 resist onto wafer
- ☐ Prebake wafer directly on hotplate for 5min at 110°C

2. back side for DRIE
   - ☐ Spread: 500 rpm, 125 r/sec, 8 sec; Dry: 1500 rpm, 750 r/s, 40 sec
   - ☐ Dispense P10 Wafer Primer
   - ☐ Dispense AZ4620 resist onto wafer
   - ☐ Prebake wafer directly on hotplate for 5min at 70°C and for 5min at 95°C
3. ABM IR aligner (reservation required)
   - ☐ Fill out log sheet
   - ☐ Load mask PL1-DRIE and wafer
   - ☐ Expose two steps 10.0sec and 9.0sec
4. Development
   - ☐ Add 100ml AZ400K developer to 400ml H2O in dedicated glass beaker (4:1 – H2O:AZ400K)
   - ☐ Load wafer into Teflon boat and immerse under agitation for 2-3min
   - ☐ Transfer to dunk tank and allow 3-cycle rinse
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier
   - ☐ Used AZ developer can go down the sink drain
5. Hard Bake
   - ☐ Post bake wafers on hotplate for 30min at 120°C

**DRIE Process**

1. Oxford DRIE (reservation required)
   - ☐ Fill out log file
   - ☐ Run “Needle Process” with patterned dummy wafer for 30min
   - ☐ Run wafers: adjust time accordingly
   - ☐ Measure membrane thickness
   - ☐ Run “clean”

2. Strip resist
   - ☐ Fill out log file for barrel asher
   - ☐ Load wafers in dedicated quartz boat for asher
   - ☐ Barrel asher with O2-plasma for 10min
   - ☐ EKC for 10min at ~60°C
   - ☐ AZ300T for 10min at ~75°C
   - ☐ transfer to dunk tank using Teflon boat and allow 3-cycle rinse
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier

**Polyimide Process I**

- ☐ Take PI out of refrigerator min 8 hours prior to use to allow PI to get up to room temperature

1. Activating surface and dehydrate with barrel asher
   - ☐ Fill out log file
   - ☐ Load wafers in dedicated quartz boat for asher
   - ☐ Barrel asher with O2-plasma for 10min
2. Spinning PI
   - ☐ Use white plastic cover for PI spinning
   - ☐ Spread: 300 rpm, 100 r/sec, 7 sec; Dry: 2750 rpm, 20000 r/s, 40 sec
   - ☐ Dispense PI2721 onto wafer
   - ☐ Prebake wafer using metal template on hotplate for 3min at 60°C and for 3min at 105°C
3. ABM IR aligner (reservation required)
   - ☐ Fill out log sheet
   - ☐ Load mask PL1-PI1 and wafer
   - ☐ Expose 45.0sec
4. PI Development (NO WATER TO BE IN CONTACT WITH POLYIMIDE)
   - ☐ 100% Developer DE6180 for 3min (2min without and 1min with agitation)
   - ☐ 1:1 - Developer DE6180 : Rinse RI9180 for 1min
   - ☐ 100% Rinse RI9180 for 30sec

- ☐ new 100% Rinse RI9180 for 30sec
- ☐ dry with $N_2$ gun and load wafers into Teflon boat
- ☐ Place Teflon boat with wafers into Spine Rinse Drier: Press DRY ONLY button Dry Spine Rinse Drier with air gun if wet inside
- ☐ Pour wasted developer and rinse into appropriate labeled waste bottles

5. Polyimide curing (reservation required, process time ~8h)
   - ☐ make sure tube is cooled down, check for prior users
   - ☐ Load “PI curing” with parameter:

| Seg Type | Time | Target | N2 Sol | N2 SP | H2 Sol | H2 SP | N2BP Sol |
|---|---|---|---|---|---|---|---|
| Time Target | 30.0 | 150 | open | 60.0 | closed | 0.0 | closed |
| Ramp Rate | 2.0 | 350 | open | 60.0 | closed | 0.0 | closed |
| Time Target | 60.0 | 350 | open | 60.0 | closed | 0.0 | closed |
| Ramp Rate | 2.0 | 20 | open | 60.0 | closed | 0.0 | closed |
| End | XXX | 0 | closed | 0.0 | closed | 0.0 | open |

**Aluminum Process**

1. Activation with barrel asher
   - ☐ Fill out log sheet
   - ☐ Load wafers in dedicated quartz boat for asher
   - ☐ Barrel asher with $O_2$-plasma for 30sec
2. BHF dip immediately prior to evaporation or BOE
   - ☐ Wear protective equipment: face shield, heavy latex gloves, heavy acid apron
   - ☐ Load wafer into Teflon boat and immerse for 20sec
   - ☐ Transfer to dunk tank and allow 3-cycle rinse
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier
3. Al evaporation (reservation required)
   - ☐ Fill out log sheet
   - ☐ Density Aluminum: 2.69
   - ☐ Evaporate Al (99%Al, 1%Si) 700nm thick (~7000Å)

## Aluminum Lithography

1. Spinning Photoresist AZ4620
   - ☐ Spread: 500 rpm, 125 r/sec, 8 sec; Dry: 1500 rpm, 750 r/s, 40 sec
   - ☐ Dispense AZ4620 resist onto wafer
   - ☐ Prebake wafer directly on hotplate for 5min at 70°C and for 5min at 95°C
6. ABM IR aligner (reservation required)
   - ☐ Fill out log sheet
   - ☐ Load mask PL1-Aluminum and wafer
   - ☐ Expose two steps 10.0sec and 9.0sec
7. Development
   - ☐ Add 100ml AZ400K developer to 400ml H2O in dedicated glass beaker (4:1 – H2O:AZ400K)
   - ☐ Load wafer into Teflon boat and immerse under agitation for 2-3min
   - ☐ Transfer to dunk tank and allow 3-cycle rinse
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier
   - ☐ Used AZ developer can go down the sink drain
2. Aluminum etch
   - ☐ Hard bake wafers on hotplate at 120°C for 5min
   - ☐ Heat Al-etch to 40°C
   - ☐ Wet wafers with DI-water and immerse under agitation
   - ☐ transfer to dunk tank using Teflon boat and allow 3-cycle rinse
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier
   - ☐ Use the aspirator tube located in the Microvision wet bench to aspirate the used Al Etch solution
3. Resist strip
   - ☐ Acetone in beaker
   - ☐ EKC for 1min at ~60°C
   - ☐ AZ300T for 1min at ~75°C
   - ☐ transfer to dunk tank using Teflon boat and allow 3-cycle rinse
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier

## Polyimide Process II

- ☐ Take PI out of refrigerator min 8 hours prior to use to allow PI to get up to room temperature

1. Activating surface and dehydrate with barrel asher
   - ☐ Fill out log file
   - ☐ Load wafers in dedicated quartz boat for asher
   - ☐ Barrel asher with $O_2$-plasma for 30sec
2. Spinning PI
   - ☐ Use white plastic cover for PI spinning
   - ☐ Spread: 300 rpm, 100 r/sec, 7 sec; Dry: 2750 rpm, 20000 r/s, 40 sec
   - ☐ Dispense PI2721 onto wafer
   - ☐ Prebake wafer using metal template on hotplate for 3min at 60°C and for 3min at 105°C
3. ABM IR aligner (reservation required)
   - ☐ Fill out log sheet
   - ☐ Load mask PL1-PI2 and wafer
   - ☐ Expose 45.0sec
4. PI Development (NO WATER TO BE IN CONTACT WITH POLYIMIDE)
   - ☐ 100% Developer DE6180 for 3min (2min without and 1min with agitation)
   - ☐ 1:1 - Developer DE6180 : Rinse RI9180 for 1min
   - ☐ 100% Rinse RI9180 for 30sec
   - ☐ new 100% Rinse RI9180 for 30sec
   - ☐ dry with $N_2$ gun and load wafers into Teflon boat
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier: Press DRY ONLY button Dry Spine Rinse Drier with air gun if wet inside
   - ☐ Pour wasted developer and rinse into appropriate labeled waste bottles
5. Polyimide curing (reservation required, process time ~8h)
   - ☐ make sure tube is cooled down, check for prior users
   - ☐ Load “PI curing” with parameter:

| Seg Type | Time | Target | N2 Sol | N2 SP | H2 Sol | H2 SP | N2BP Sol |
|---|---|---|---|---|---|---|---|
| Time Target | 30.0 | 150 | open | 60.0 | closed | 0.0 | closed |
| Ramp Rate | 2.0 | 350 | open | 60.0 | closed | 0.0 | closed |
| Time Target | 40.0 | 350 | open | 60.0 | closed | 0.0 | closed |
| Ramp Rate | 2.0 | 400 | open | 60.0 | closed | 0.0 | closed |
| Time Target | 20.0 | 400 | open | 60.0 | closed | 0.0 | closed |
| Ramp Rate | 2.0 | 20 | open | 60.0 | closed | 0.0 | closed |
| End | XXX | 0 | closed | 0.0 | closed | 0.0 | open |

## Reactive Ion Etching for Needle sharpening

3. TRION RIE (reservation required)
   - ☐ Fill out log sheet
   - ☐ Run “Clean”
     - Parameter:

| | | | | |
|---|---|---|---|---|
| Pressure Set: | 185 | Oxygen Set: | 0 |
| RF Power Set: | 105 | CHF3 Set: | 0 |
| Endpoint Set: | 100 | SF6 Set: | 55 |
| Process Time Set: | sec | | 0 |
| Temperature: | 300 | | 0 |
| Base Pressure Set: | 150 | | 0 |

   - ☐ Etch single devices

## A.3 Contact Test Process Listing

### Wafer Preparation / Cleaning

1. Labeling wafers
    - ☐ Scribe code and numbers on wafer: PL-CT-1…
2. Wafer Cleaning (Piranha 4:1 – $H_2SO_4$:$H_2O_2$)
    - ☐ Label: date, time, name, phone number, chemicals/mixture
    - ☐ Wear protective equipment: face shield, heavy latex gloves, heavy acid apron
    - ☐ Use dedicated labeled glass beaker inside labeled white container
    - ☐ Measure 800ml $H_2SO_4$
    - ☐ Slowly pour 200ml $H_2O_2$ from graduate cylinder (CAUTION: exothermic reaction)
    - ☐ Immersion wafers into piranha solution using Teflon boat for 15min
    - ☐ Transfer to dunk tank and allow 3-cycle rinse
    - ☐ Place Teflon boat with wafers into Spine Rinse Drier
    - ☐ Allow piranha solution to cool down
    - ☐ Use the aspirator tube located in the Microvision wet bench to aspirate the solution

### Polyimide Process I

- ☐ Take PI out of refrigerator min 8 hours prior to use to allow PI to get up to room temperature

1. Activating surface and dehydrate with barrel asher
    - ☐ Fill out log file
    - ☐ Load wafers in dedicated quartz boat for asher
    - ☐ Barrel asher with $O_2$-plasma for 10min
2. Spinning PI
    - ☐ Use white plastic cover for PI spinning
    - ☐ Spread: 300 rpm, 100 r/sec, 7 sec; Dry: 2750 rpm, 20000 r/s, 40 sec
    - ☐ Dispense PI2721 onto wafer

- ☐ Prebake wafer using metal template on hotplate for 3min at 60°C and for 3min at 105°C

3. ABM IR aligner (reservation required)
   - ☐ Fill out log sheet
   - ☐ Load mask PL1-PI1 and wafer
   - ☐ Expose 45.0sec
4. PI Development (NO WATER TO BE IN CONTACT WITH POLYIMIDE)
   - ☐ 100% Developer DE6180 for 3min (2min without and 1min with agitation)
   - ☐ 1:1 - Developer DE6180 : Rinse RI9180 for 1min
   - ☐ 100% Rinse RI9180 for 30sec
   - ☐ new 100% Rinse RI9180 for 30sec
   - ☐ dry with $N_2$ gun and load wafers into Teflon boat
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier: Press DRY ONLY button Dry Spine Rinse Drier with air gun if wet inside
   - ☐ Pour wasted developer and rinse into appropriate labeled waste bottles
5. Polyimide curing (reservation required, process time ~8h)
   - ☐ make sure tube is cooled down, check for prior users
   - ☐ Load “PI curing” with parameter:

| Seg Type | Time | Target | N2 Sol | N2 SP | H2 Sol | H2 SP | N2BP Sol |
|---|---|---|---|---|---|---|---|
| Time Target | 30.0 | 150 | open | 60.0 | closed | 0.0 | closed |
| Ramp Rate | 2.0 | 350 | open | 60.0 | closed | 0.0 | closed |
| Time Target | 60.0 | 350 | open | 60.0 | closed | 0.0 | closed |
| Ramp Rate | 2.0 | 20 | open | 60.0 | closed | 0.0 | closed |
| End | XXX | 0 | closed | 0.0 | closed | 0.0 | open |

**Aluminum Process**

1. Activation with barrel asher
   - ☐ Load wafers in dedicated quartz boat for asher
   - ☐ Barrel asher with $O_2$-plasma for 30sec
2. BHF or BOE dip immediately prior to evaporation

- ☐ Wear protective equipment: face shield, heavy latex gloves, heavy acid apron
- ☐ Load wafer into Teflon boat and immerse for 30sec
- ☐ Transfer to dunk tank and allow 3-cycle rinse
- ☐ Place Teflon boat with wafers into Spine Rinse Drier

3. Al evaporation (reservation required)
   - ☐ Fill out log sheet
   - ☐ Density Aluminum: 2.69
   - ☐ Evaporate Al (99%Al, 1%Si) 700nm thick (~7000Å)

**Aluminum Lithography**

1. Spinning Photoresist AZ4620
   - ☐ Spread: 500 rpm, 125 r/sec, 8 sec; Dry: 1500 rpm, 750 r/s, 40 sec
   - ☐ Dispense AZ4620 resist onto wafer
   - ☐ Prebake wafer directly on hotplate for 5min at 70°C and for 5min at 95°C
5. ABM IR aligner (reservation required)
   - ☐ Fill out log sheet
   - ☐ Load mask PL1-AG and wafer
   - ☐ Expose two steps 9.5sec
6. Development
   - ☐ Add 100ml AZ400K developer to 400ml H2O in dedicated glass beaker (4:1 – H2O:AZ400K)
   - ☐ Load wafer into Teflon boat and immerse under agitation for 2-3min
   - ☐ Transfer to dunk tank and allow 3-cycle rinse
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier
   - ☐ Used AZ developer can go down the sink drain
2. Aluminum etch
   - ☐ Hard bake wafers on hotplate at 120°C for 5min
   - ☐ Heat Al-etch to 40°C
   - ☐ Wet wafers with DI-water and immerse under agitation
   - ☐ transfer to dunk tank using Teflon boat and allow 3-cycle rinse

- ☐ Place Teflon boat with wafers into Spine Rinse Drier
- ☐ Use the aspirator tube located in the Microvision wet bench to aspirate the used Al Etch solution

3. Resist strip
   - ☐ Acetone in beaker 3min
   - ☐ transfer to dunk tank using Teflon boat and allow 3-cycle rinse
   - ☐ Place Teflon boat with wafers into Spine Rinse Drier

### Aluminum Annealing

- ☐ make sure tube is cooled down, check for prior users
- ☐ Load “PI curing” with parameter:

| Seg Type | Time | Target | N2 Sol | N2 SP | H2 Sol | H2 SP | N2BP Sol |
|---|---|---|---|---|---|---|---|
| Time Target | 30.0 | 150 | open | 60.0 | closed | 0.0 | closed |
| Ramp Rate | 2.0 | 350 | open | 60.0 | closed | 0.0 | closed |
| Time Target | 40.0 | 350 | open | 60.0 | closed | 0.0 | closed |
| Ramp Rate | 2.0 | 400 | open | 60.0 | closed | 0.0 | closed |
| Time Target | 20.0 | 400 | open | 60.0 | closed | 0.0 | closed |
| Ramp Rate | 2.0 | 20 | open | 60.0 | closed | 0.0 | closed |
| End | XXX | 0 | closed | 0.0 | closed | 0.0 | open |

### Sawing

1. Spinning Photoresist AZ4620
   - ☐ Spread: 500 rpm, 125 r/sec, 8 sec; Dry: 1500 rpm, 750 r/s, 40 sec
   - ☐ Dispense AZ4620 resist on front side
   - ☐ Prebake wafer directly on hotplate for 5min at 95°C
2. blue tape for back side protection
3. Dicing Saw
   - ☐ Sawing speed 10, water pump 5
4. Resist strip with Acetone

## A.4 List of Figures

## A.5 List of Tables

# A.6 Mask Layouts

## A.6.1 Contact Test Masks

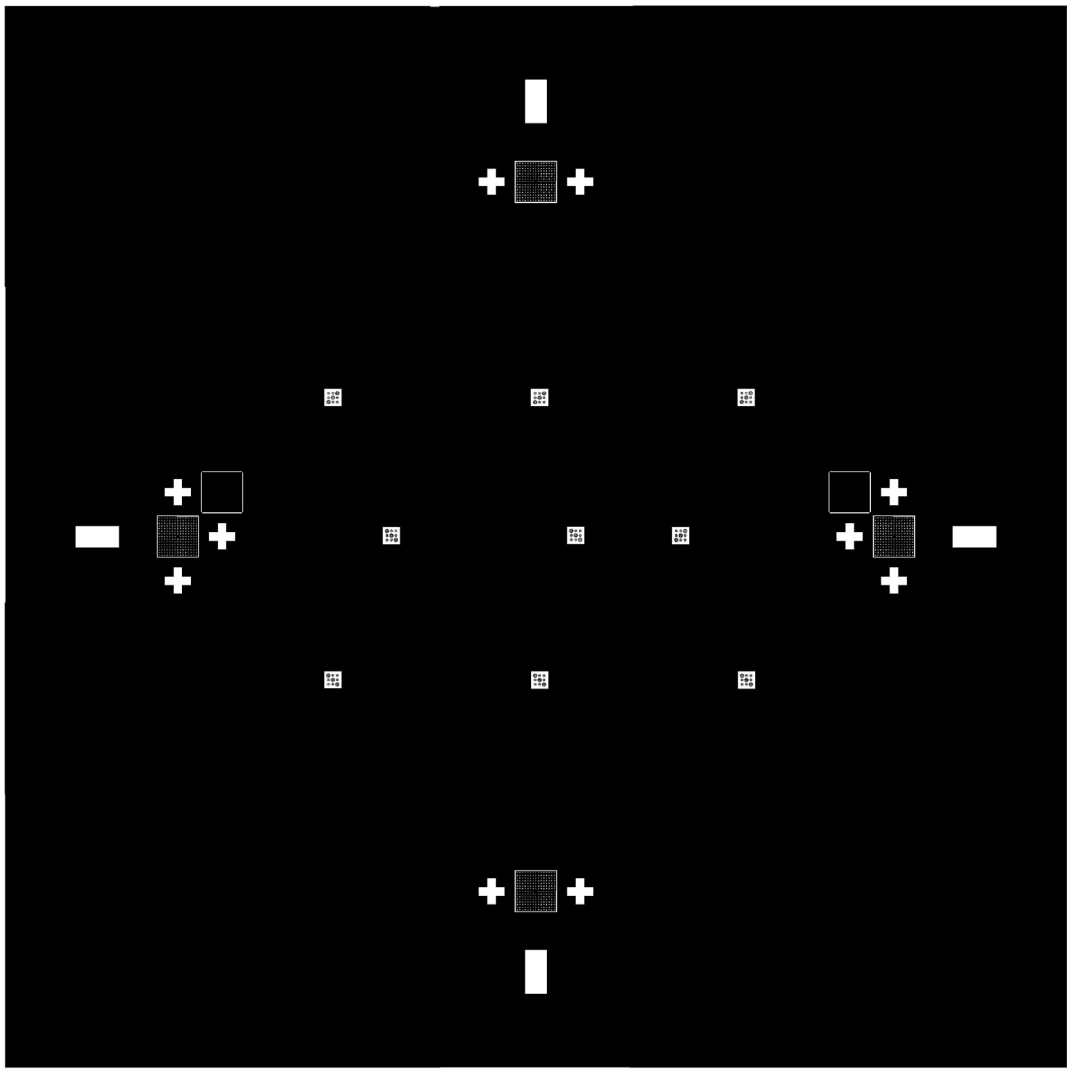


Figure A.6.1: Conductivity Test – DRIE Mask (PL-CT-DRIE)

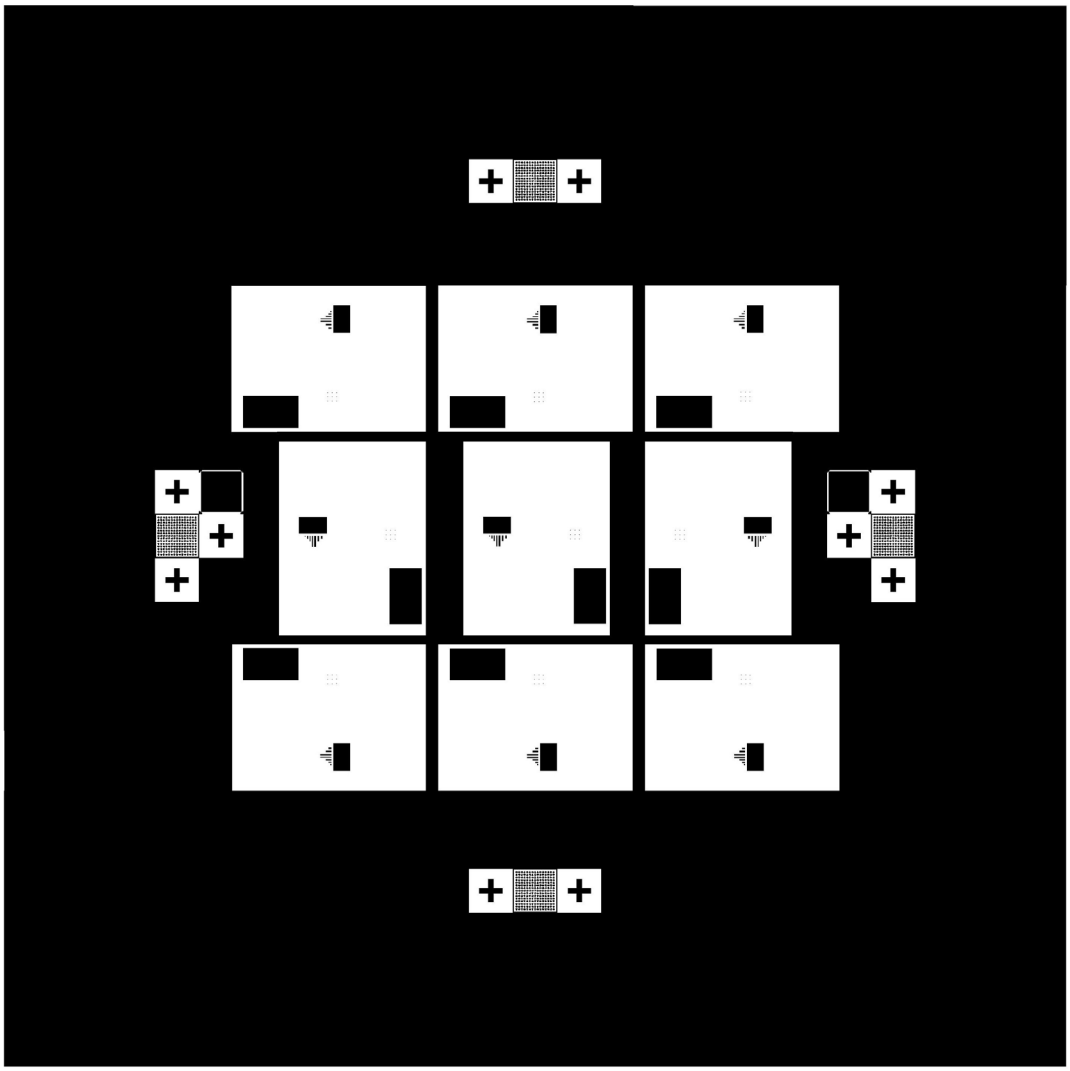


Figure A.6.2: Conductivity Test – Polyimide Mask (PL-CT-POLY)

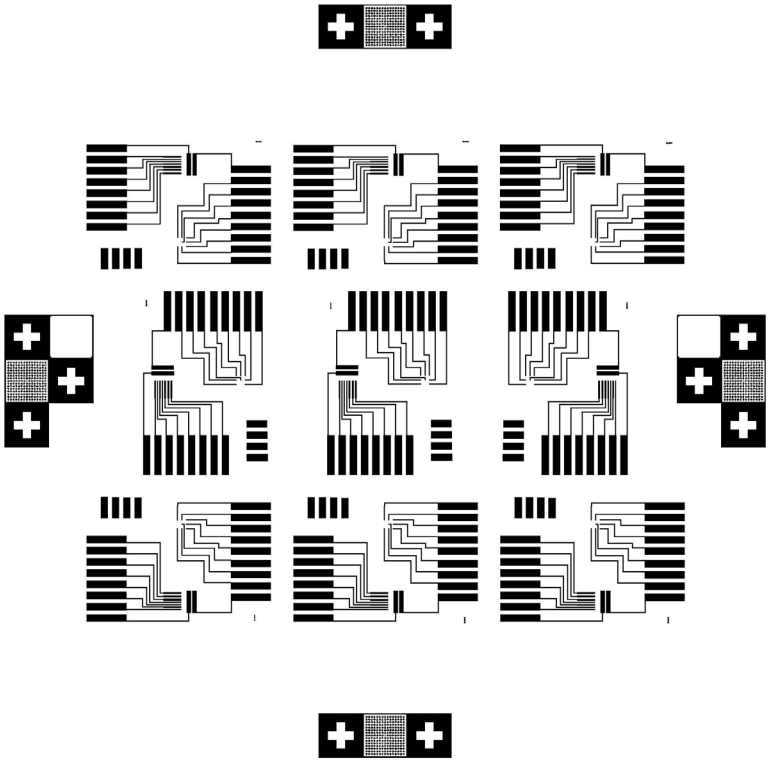


Figure A.6.3: Conductivity Test – Aluminium / Silver Mask (PL-CT-AL)

## A.6.2 Needle Process Masks

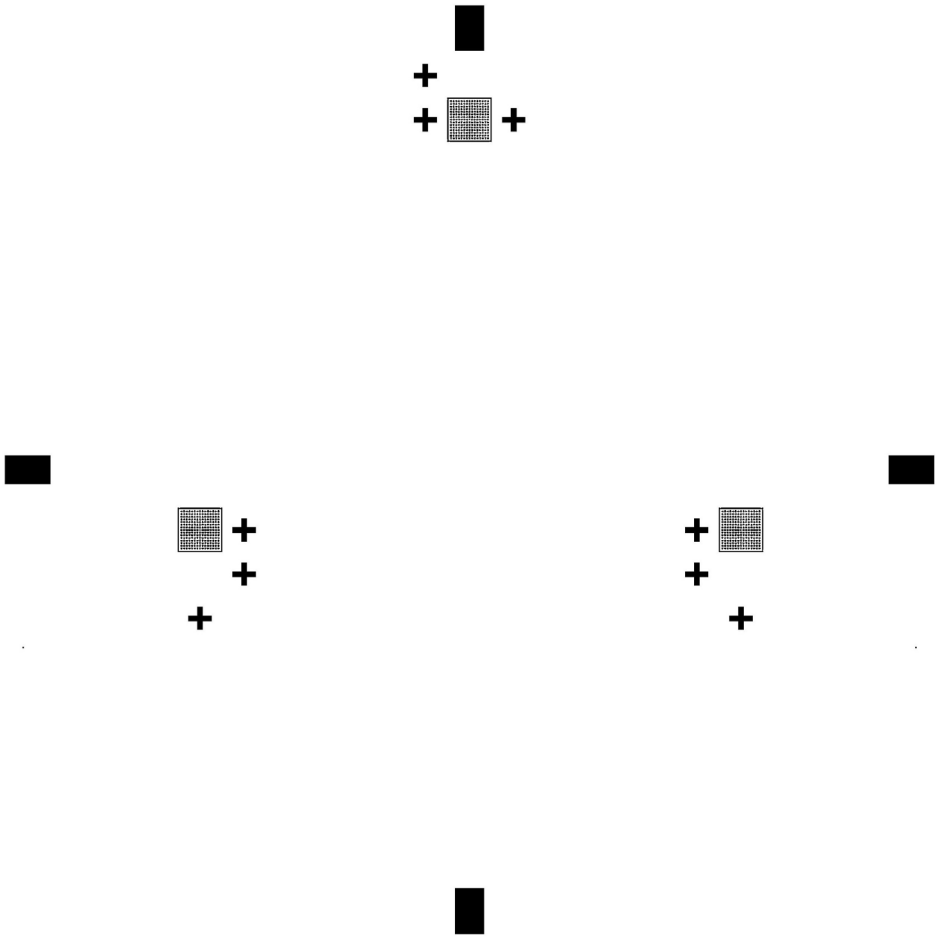


Figure A.6.4: Needle Device – Alignment Mask (PL-ND1-AG)

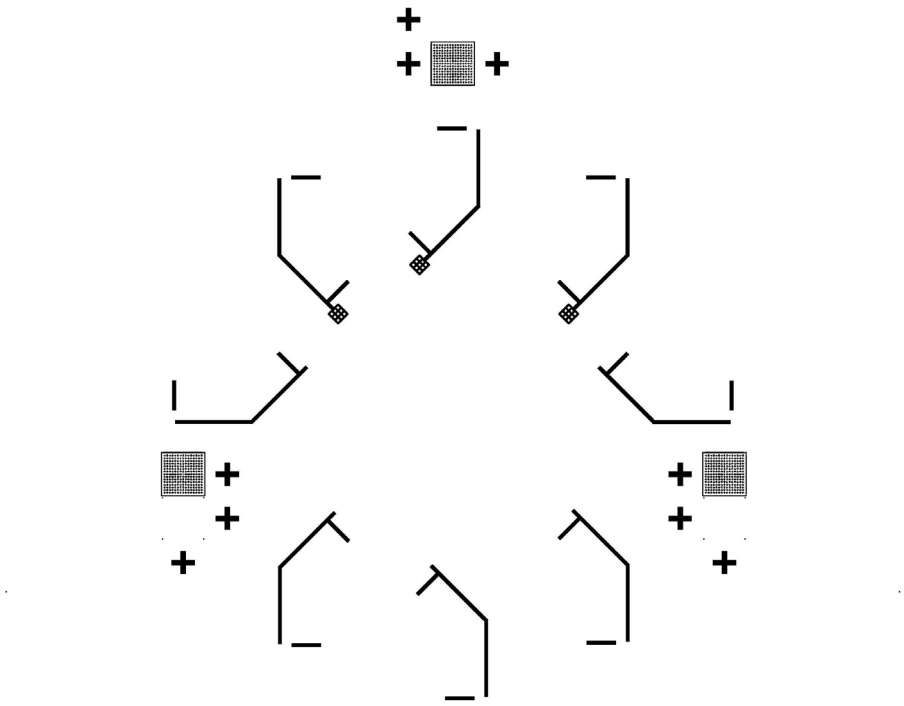


Figure A.6.5: Needle Device – Al Etch Stop Mask (PL-ND1-ETCHSTOP)

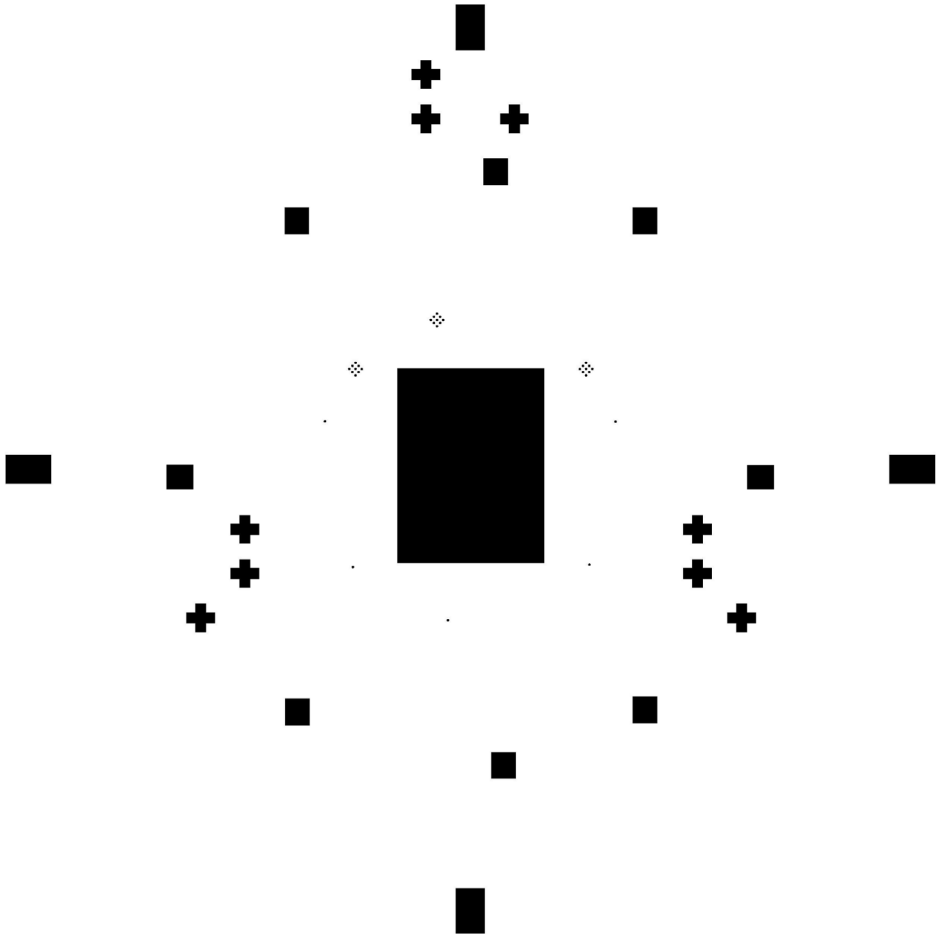


Figure A.6.6: Needle Device – Oxide Etch Stop Mask (PL-ND1-OXIDE)

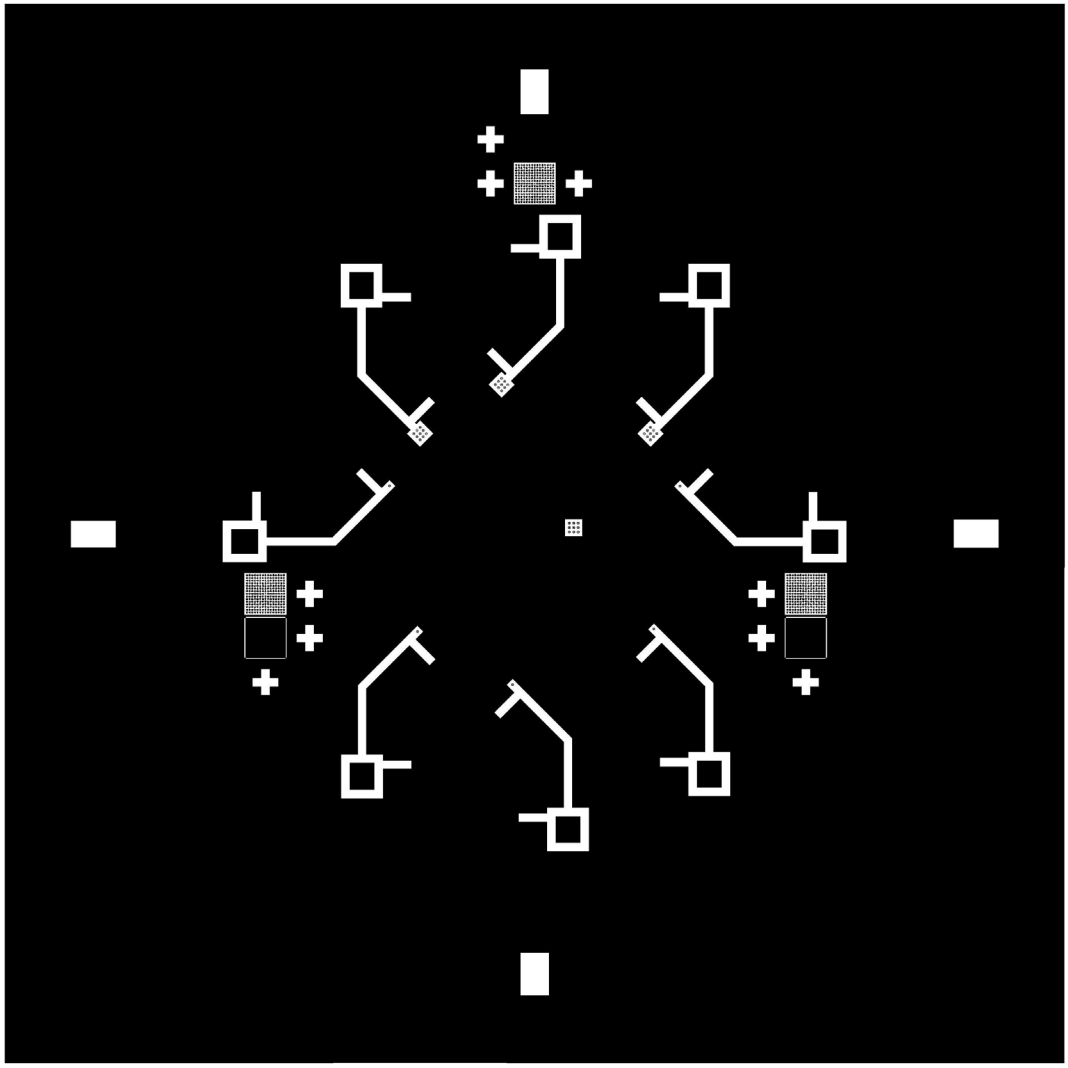


Figure A.6.7: Needle Device – DRIE Mask (PL-ND1-DRIE)

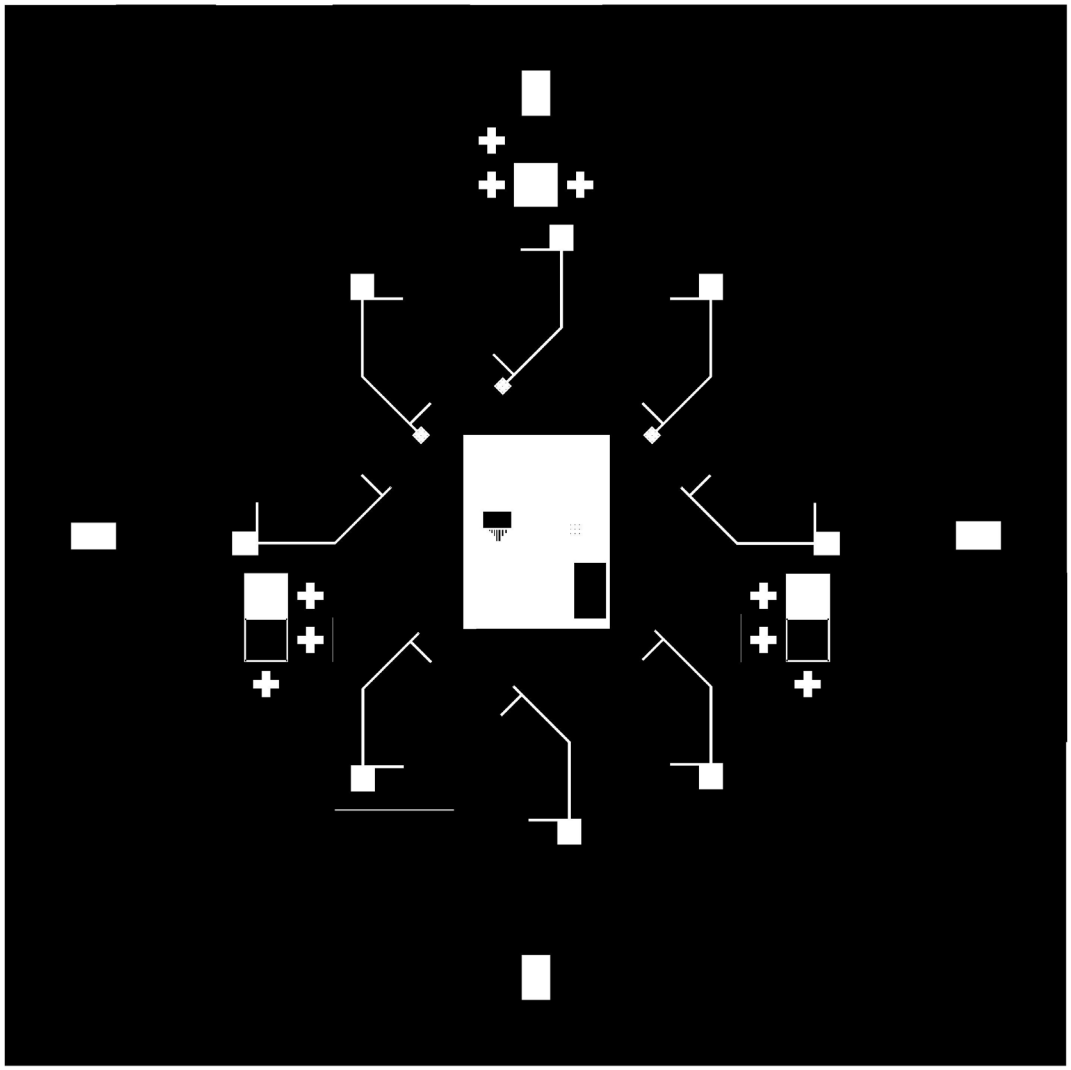


Figure A.6.8: Needle Device – Polyimide 1 Mask (PL-ND1-POLY1)

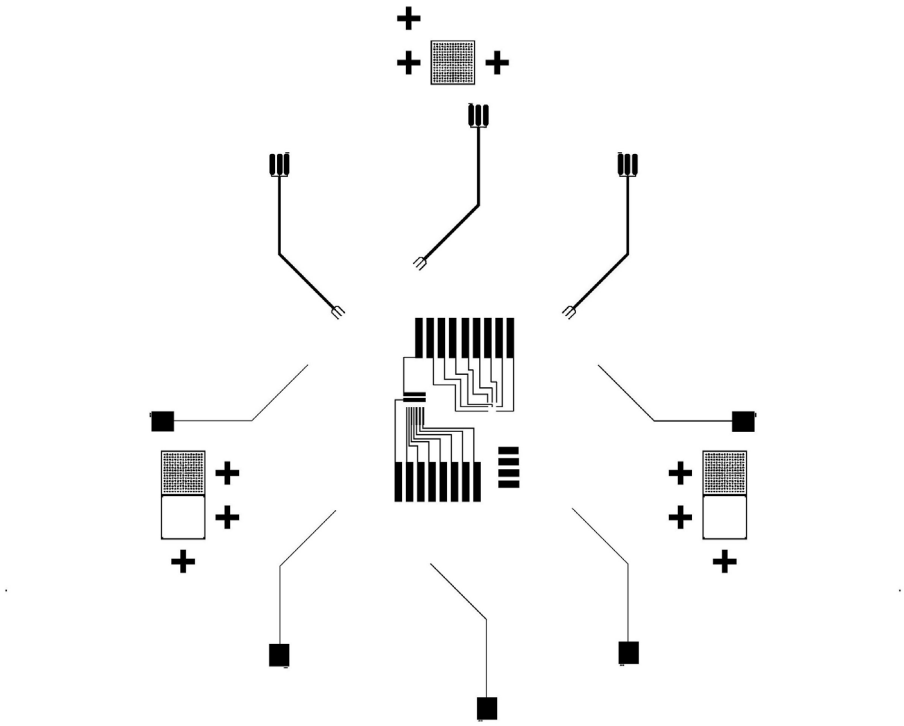


Figure A.6.9: Needle Device – Aluminium Mask (PL-ND1-AL)

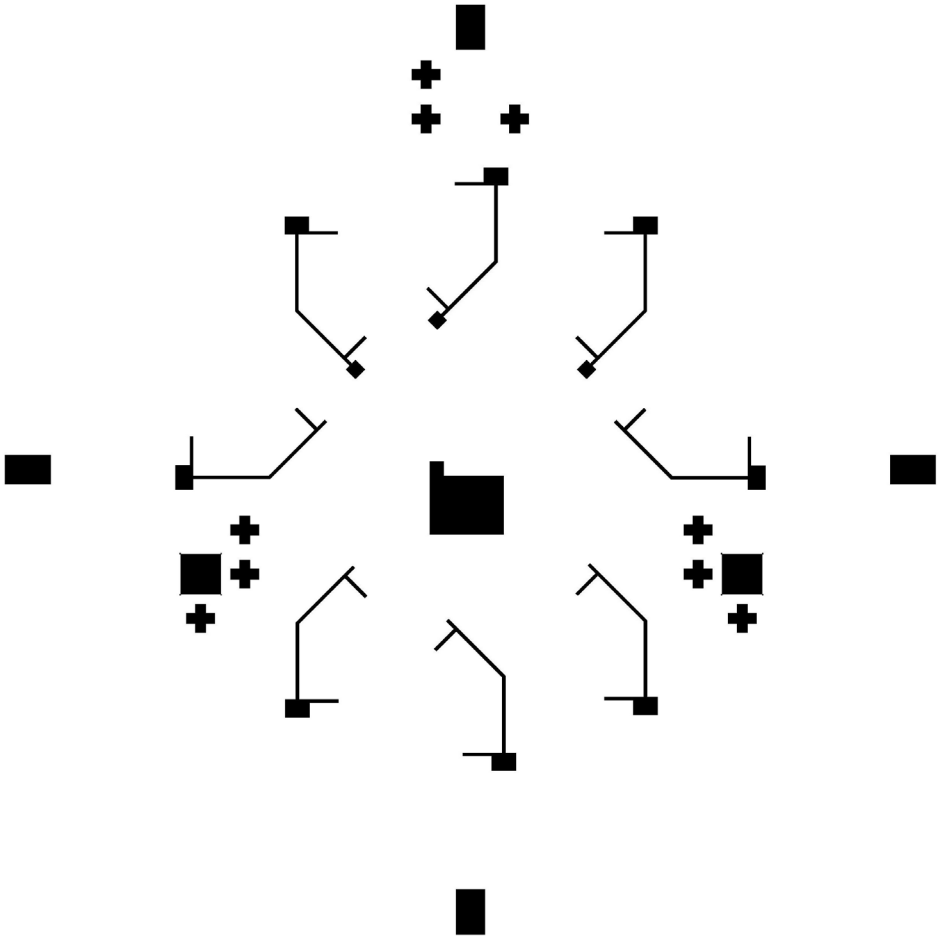


Figure A.6.10: Needle Device – Polyimide 2 Mask (PL-ND1-POLY2)

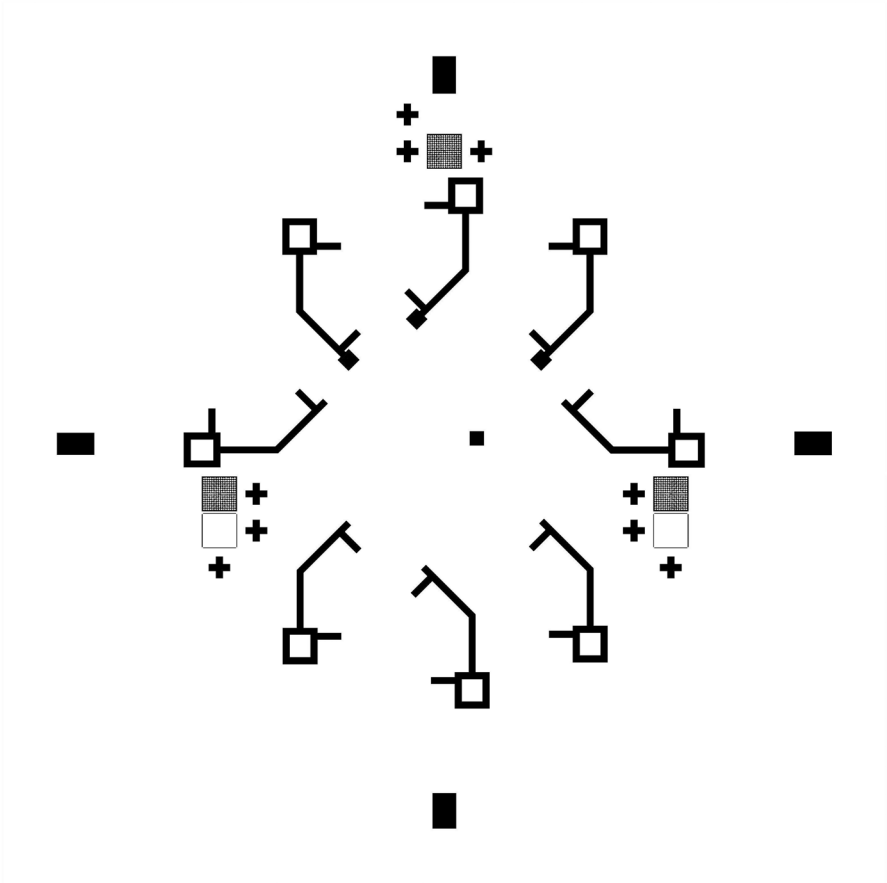


Figure A.6.11: Needle Device – Tip Insulation (PL-ND1-TIP)

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