CMOS Integrated Ciliary Actuator Array as a General-Purpose Micromanipulation Tool for Small Objects

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Abstract— The first micromachined bimorph organic ciliary array with on-chip CMOS circuitry is presented. This ciliary array is composed of an 8×8 array of cells each having four orthogonally oriented actuators in an overall die size of 9.4×9.4 mm. The polyimide-based actuators were fabricated directly above the selection and drive circuitry. Selection and activation of actuators in this array shows that integration was successful. The array was programmed to do simple linear and diagonal translations and squeeze-, centering-, and rotating-field manipulations. All three tasks were demonstrated using silicon pieces of various shapes and either 0.55 mm or 0.10 mm thick. [365]

Index Terms—Actuator, array, CMOS, integration, micromanipulation, polyimide.

I. INTRODUCTION

ONE of the potential applications of MEMS actuators is in the moving and positioning of small parts because the actuators themselves are on a similar scale [1]. Toward the realization of this goal, researchers have been designing and building arrayed actuator systems that can overcome some of the inherent limitations of many micromachined actuators (relatively limited range of motion, degrees of freedom, and force output) through the arrangement of actuators in series or parallel [2]–[4]. A variety of actuation method have

been used including air jets [5]–[7], electromagnetic actuators [8]–[10], piezoelectric actuators [11], electrostatic actuators [12], thermal-bimorph (bimaterial) actuators [13]–[16], and electrothermal (single-material) actuators [17], [18]. Whatever the chosen method, the actuators have two fundamental requirements: 1) the generation of enough force or torque to move not only themselves but also to move external objects, and 2) the generation of large displacements of the moving parts or of the media (e.g., air jets) in which the parts move. Our previously reported ciliary arrays [15], [16] were, to our knowledge, the first ones able to move small parts in a controlled and repeatable manner along any user-chosen direction in an x-y plane.

The arrayed actuators described herein are deformable microstructures that curl into and out of the substrate plane. The curling of the actuators is due to the different coefficients of thermal expansion (CTE) of two polyimide layers that make up the structures. An integrated heater resistor is sandwiched between the two polyimide layers. When an electric current is passed through the heater resistor, the temperature of the actuator increases, and the structure (initially deflected out-of-plane) deflects downward producing both horizontal and vertical displacements. Objects that are placed on the array can be made to move by coordinating the deflections of such actuators.

Another goal of some MEMS researchers has been to merge microelectronics and micromachined transducers since the advantages gained by miniaturization and parallel fabrication can be more fully exploited by closely integrating electronic functions [19]–[21]. Different approaches have been taken, including carrying out bulk micromachining processes on completed dice or whole wafers [22]–[24], the interlacing of micromachining steps within a modified CMOS process [25], [26], the packaging of hybrid solutions such as flip-chip, wire bonding, or wafer-to-wafer bonding [27], [28], the processing of MEMS features prior to CMOS processing [29], or the postprocessing of standard CMOS to add surface micromachined transducers [30]–[32]. For an early discussion on the benefits of circuit integration for distributed actuator arrays see [33].

The purpose of this paper is to describe the first functional ciliary actuator array integrated with CMOS circuitry, providing a means for activating individual cilia and enabling the functions of the array to be altered by software. The overall architecture of the chip and major features, the CMOS

(A) Layout and size of chip

(B) 2-DOF motion pixel

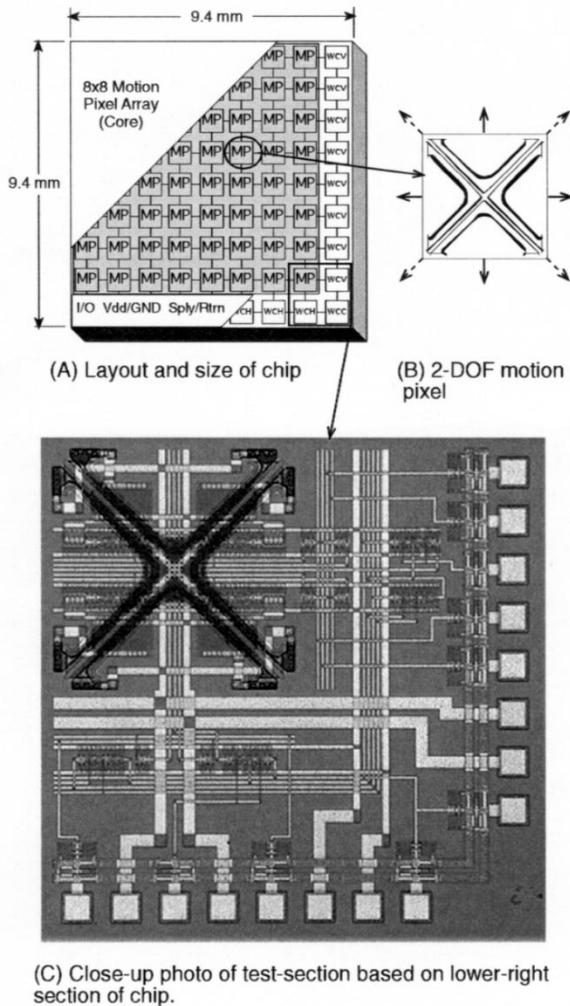(C) Close-up photo of test-section based on lower-right section of chip.

Fig. 1. The general architecture of the CMOS ciliary array is illustrated at left. The majority of the chip is comprised of an 8×8 array of CMOS integrated motion pixels (MP). Surrounding the array core are various circuits for input and output (I/O) for data, clocking, and power. Each motion pixel cell (illustrated at right) has four triangle-shaped ciliary actuators. The photo shows a test cell.

integrated microfabrication process, and the supporting hardware and software components that are needed to operate the ciliary array chip as a general-purpose manipulation tool are described in Section II. Section III outlines the observations and experiments done in this work, and Section IV summarizes the results. A discussion of the performance of the array is provided in Section V, and the final Section VI, is a summary of the paper.

II. METHODS

A. Chip Architecture

The general architecture of the CMOS integrated ciliary array chip is shown in Fig. 1(a). The device is composed of two basic sections: the array core and the periphery surrounding the core on two sides. The array core consists of 256 ciliary actuators each with their associated logic and driver circuitry.

The actuators are grouped into 1×1 mm cells [Fig. 1(b)] and are arranged as an 8×8 array. Along the periphery of the core is a shift register chain, a mode select circuit, and row and column data loading circuits. The shift register chain consists of 16 cells, each of which has a shift register and a serial-parallel/row loader. These circuits provide the option of loading data into the individual cilia in a parallel or serial manner. The periphery also contains the voltage and ground bond pads for the logic circuits (Vdd and Gnd) and the power supply and return bond pads for the ciliary actuators. There are also eight sets of *Supply* and *Return* pads located in the horizontal wiring cells (one set per motion pixel column) to provide for a separate power supply voltage for the actuators (potentially above the logic supply voltage).

1) Motion Pixel Cells: The four ciliary actuators in each motion pixel are arranged orthogonally in a common-tip configuration. Each cilium has a driver circuit consisting of logic circuits and current drivers (Fig. 2). In addition, the motion pixel cell has globally routed power and data interconnect lines that run parallel to its vertical and horizontal axes. Two series-connected D-flip flops (or phase registers) provide a buffering scheme so that one register can be updated while the other register is controlling the actuator state. This arrangement enables simultaneous updating of all cilia. A register transfer signal enables the second register to change its state, thus transferring new data to the buffers and the MOSFET current driver.

The ciliary actuator is a triangle-shaped structure fabricated using surface micromachining methods. It is a multilayered structure made up of polyimide, silicon nitride, aluminum, and titanium-tungsten films. Fig. 3 is an illustration of the actuator with the upper polyimide and silicon nitride layers removed showing the relative placement of the other layers. The width of the cilium varies along its length: at the tip the beam is 107 μm wide and gradually tapers to a width of 39 μm near the base; at the base the actuator again widens to 105 μm. The Ti–W heater resistor ($\approx$1 kΩ) gradually widens from 10 μm near the base to 28 μm at the tip. The resistor is widest at the tip area to limit power dissipation and to lessen current crowding effects [34] where the path of the resistor turns through 90°.

Two important factors in the design of this actuator are the lifting capacity and the tip deflections. Through FEM simulations with the SOLIDIS modeling tool (ISE Integrated Systems Engineering AG, Zurich, Switzerland) [35], the lifting capacity was estimated to be $\approx$80 μN which is more than seven times than the specific weight of a silicon die ($\approx$11 μN/mm^2). Furthermore, the vertical displacement at the tip was computed to be $\approx$ 100 μm. These figures are comparable to another ciliary actuator (described in [15] and [16]) which clearly demonstrated the ability to move a variety of small parts. The material data (Table I) used in the FEM simulations was obtained from various literature sources [36]–[43]. Prior to simulation of the ciliary actuator, the values were verified by running simulations of two-dimensional (2-D) models of trimorph cantilever test structures (e.g., PIQ-3200/Al/PIQ-L200) fabricated alongside the ciliary array. The simulations of the test structures vertical deflections were within 10% of
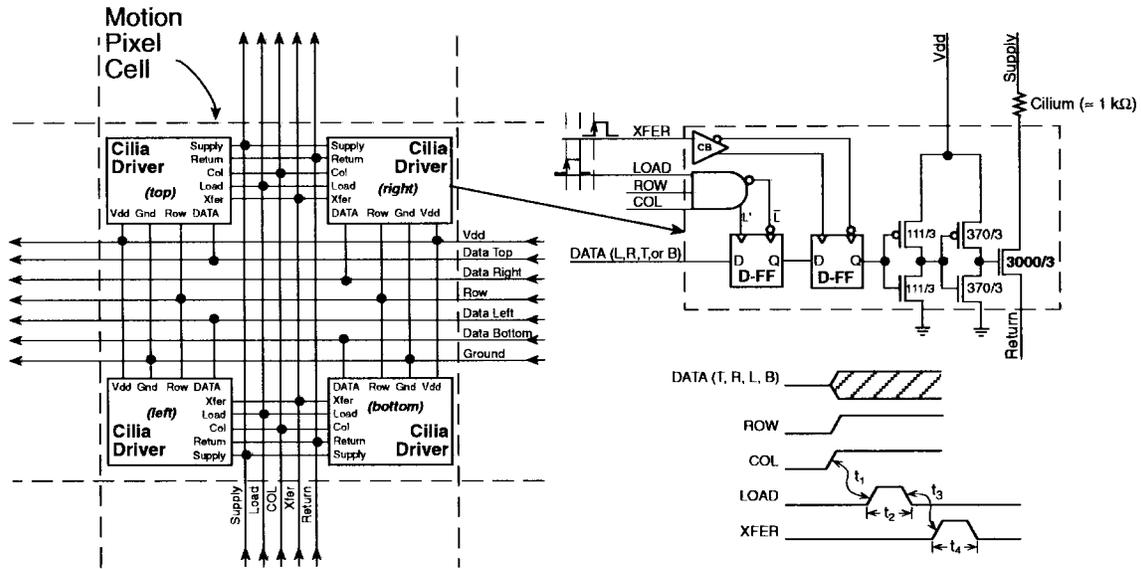
Fig. 2. Block diagram of a motion pixel cell is shown at left. The cilia driver circuit is detailed in the upper right side of the figure. The driver consists of logic circuits, two series-connected D-flip flops and a current driver. The timing necessary to run this circuit is shown in the lower right: t_1 = Data, Row, and col. setup time; t_2 = Load pulse width; t_3 = Load and Xfer clock dead time; t_4 = Xfer pulse width.
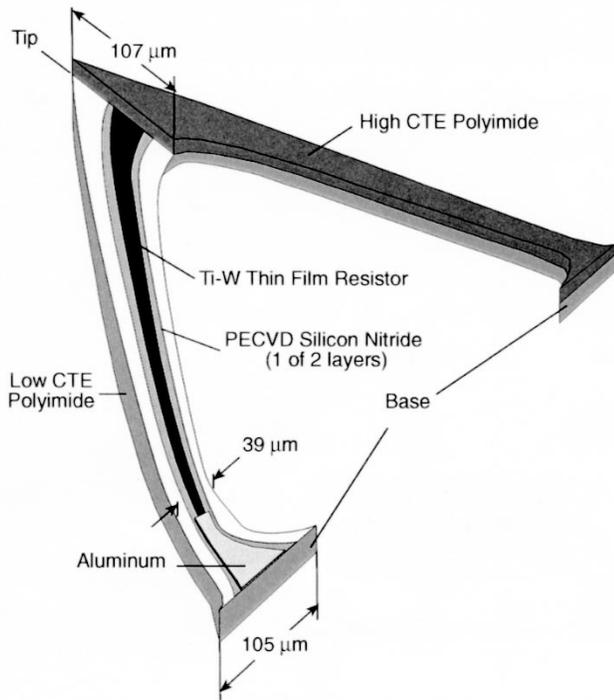

Fig. 3. Illustration of the polyimide-bimorph thermal ciliary microactuator. In plan view, the actuator has the shape of two sides of an isosceles triangle. The actuator is attached to the substrate at two locations (the base). In this illustration, half of the upper polyimide and PECVD silicon nitride layers are shown removed to reveal the middle layers.

those observed from SEM micrographs. Because the actuators are curled out-of-the plane when not powered, the amount of power needed to transport an object across the array depends on how much force it exerts per unit area. In other words, the more an object weighs per unit area the more it depresses the actuators it is on to the substrate, so that adja-

cent actuators need to be correspondingly heated to a higher temperature to match the deflection and receive the oncoming object.

2) Input/Output Cells: The peripheral cells contain voltage and ground pads and circuits that perform input and output (I/O) functions: row and column selection, serial data input/output pads, and cilia selection. The most important function performed by these peripheral cells is serial row and column selection which is accomplished by the 16-cell shift register chain that is routed around two edges of the array core. A simplified block diagram of one example I/O cell is shown in Fig. 4.

Within each unit of the chain is a shift register cell and the serial/parallel row/column load circuit which allows the array to operate in either a serial or parallel loading mode. The serial mode is selected when the global control line *S/P Select* is held at logic HIGH, while a LOW puts the chip into the parallel loading mode. Monitoring of the rows and columns that have been activated can be done when the array is in serial mode since the output of the shift register circuit drives a buffer that in turn drives the bond pads as an output. In parallel mode the pad buffers are put into a high impedance state, and the bond pads for each row or column directly drive the row or column buffers as shown in Fig. 4. Additionally, if the shift register cell output is disabled, the serial inputs have no effect on the row or column states.

B. Fabrication: CMOS Integrated MEMS

Complete processing of the ciliary actuator array chip required 17 masks (see Fig. 5) and can be segmented into two portions: one for our standard CMOS process (9 masks) and the other for the polyimide ciliary actuators (8 masks). Only slight modifications were made to the original bimorph organic actuator process as described in references [15] and [16].

TABLE I
THE MATERIAL AND PROCESS TEMPERATURE DATA USED IN THE DESIGN OF THE CILIARY ACTUATOR. [CURING THE PIQ POLYIMIDES
REQUIRED A WIDE TEMPERATURE RANGE (100–350°C), BUT 240°C WAS USED AS THE PROCESS TEMPERATURE IN MODELING]

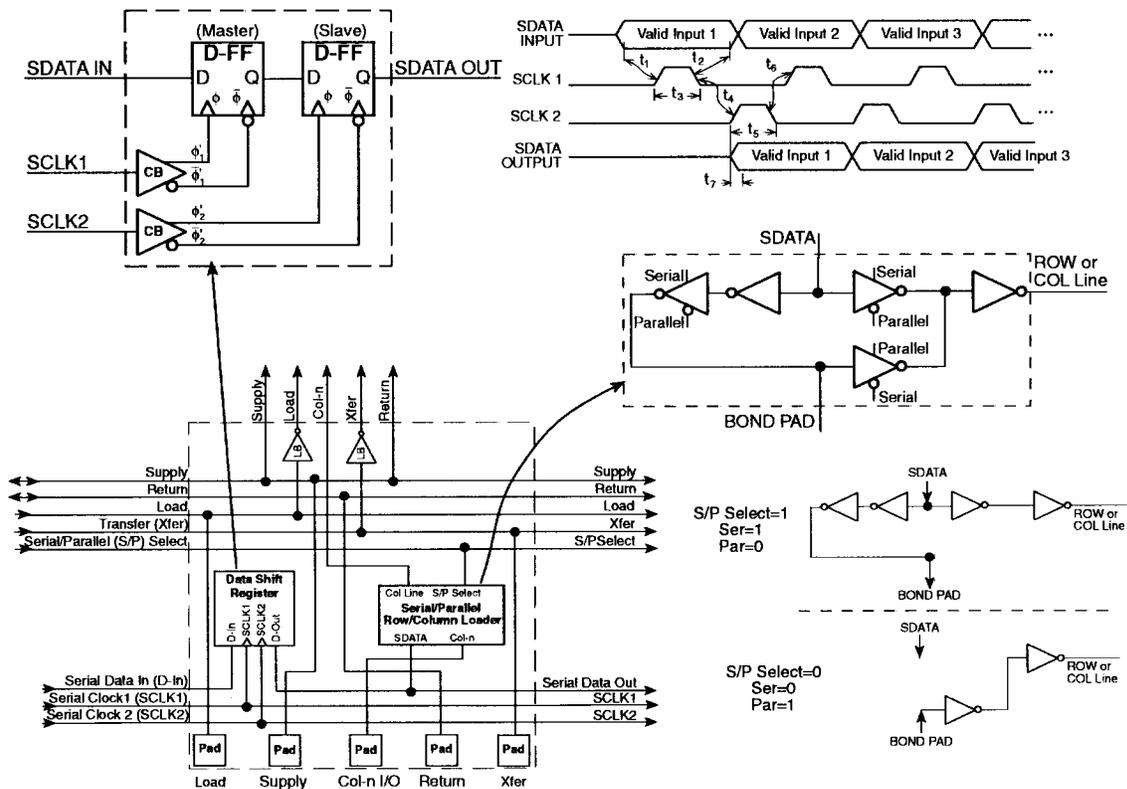| Material	Typical Thickness (µm)	Young's Modulus (GPa)	Poisson's Ratio	CTE (ppm/°C)	Process Temp. (°C)	Refs.
PIQ-3200	3.2 -4.5	8.6	0.33	50	240	[37, 38]
PIQ-L200	3.2-4.5	2.95	0.33	2	240	[37, 38]
PECVD Silicon Nitride	0.12-0.14	183	0.25	1.5	300	[41, 42]
50:50 Ti:W	0.09-0.1	340	0.2	4	25-40	[39, 40, 43]
Al	0.8-1.1	70	0.33	23.6	25-40	[36, 43]

Fig. 4. Simplified block diagram of an example shift register cell. A schematic of the data shift register is shown at the upper left and its timing diagram is shown on the upper right. The Serial/Parallel Row/Column Loader block diagram is shown at the middle right. It can be set to run in either a data output (S/P Select = HIGH) or a data input mode (S/P Select = LOW).

The starting material was a (100), n-type (5–10 Ω · cm), 100-mm Si wafer. The process was begun by growing a 25-nm cleanup oxide (that was removed before field oxidation) prior to a phosphorus blanket implant (1.45×10^{12} at 100 keV) which provided a uniform n-type surface dopant for p-channel gates and field channel stops. Following this, a 0.5-µm field oxide was thermally grown for 1 h and 40 min in a wet ambient at 1000 °C. Then the active areas were patterned (Mask 1) and etched in a buffered hydrofluoric (BHF) acid solution.

Next, a 25-nm sacrificial oxide was grown in the active areas to protect the silicon during the subsequent implant.

After patterning the p-well areas (Mask 2), the wafers were implanted with boron in two steps (one shallow [1.4×10^{12} at 50 keV] and one deep [5.0×10^{12} at 300 keV]) which produces a deep flat well profile. After the implant, the p-wells were driven in at 1000 °C for 3 h to anneal the silicon and to produce a gentle p-well profile. The next steps were to strip the sacrificial oxide, grow a 25-nm-thick gate oxide, and deposit an 0.4-µm-thick undoped gate polysilicon film in a CVD furnace. It was critical to do these last two steps without interruption to minimize exposing the gate silicon and the gate oxide to the ambient. The polysilicon gates were

I. CMOS for Transducers
(9 Masks)

Active
P-Well
Poly-Si
N-Plus
Poly-Si Vias
Metal1
LTO1 Vias
Metal2
LTO2 Vias

II. Bimorph Polyimide MEMS
(9 Masks)

this step shared in integrated process

Metal1
Metal2
Nitride1 Cap
Polyimide1 Vias
Nitride2 Cap
Metal3 (TiW)
Metal4
Nitride3 Cap
Polyimide2 Vias

order switched in integrated process

III. CMOS Integrated MEMS
(17 Masks, w/ one shared step)

Active
P-Well
Poly-Si
N-Plus
Poly-Si Vias
Metal1
LTO1 Vias
Metal2
LTO2 Vias
Nitride1 Cap
Metal3
Polyimide1 Vias
Nitride2 Cap
Metal4 (TiW)
Metal5
Nitride3 Cap
Polyimide 2 Vias

Base
Tip
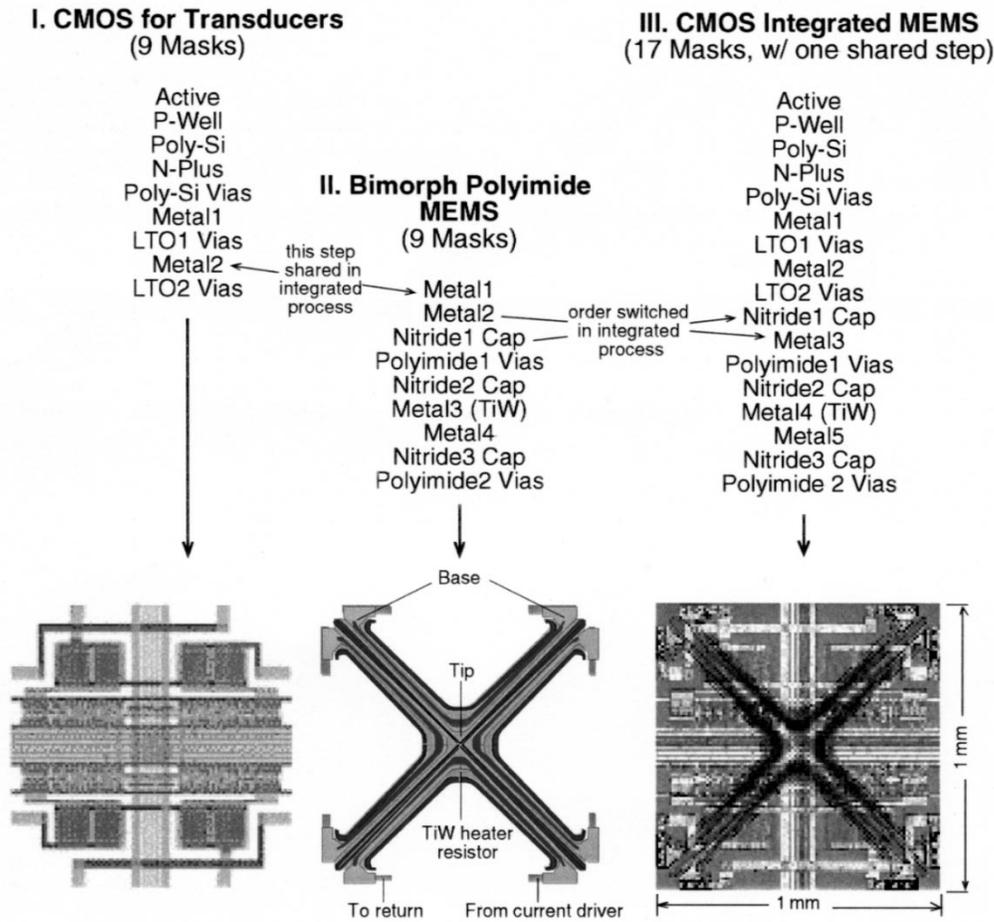TiW heater resistor
To return
From current driver
1 mm
1 mm

Fig. 5. The approach for fabricating the CMOS ciliary array was to combine a CMOS and a MEMS fabrication process. The MEMS process was developed to be post-CMOS compatible. The left and middle illustration at the bottom show the CMOS and MEMS motion pixel module layouts, respectively. The right optical microphotograph shows one cell of a completed motion pixel cell.

subsequently patterned (Mask 3) and anisotropically etched using an SF_6/Freon™ 115 plasma.

Next, the n+ regions were defined in patterned photoresist (Mask 4) and arsenic was implanted to form self-aligned source/drains (the dosage and energy [5.0×10^{15} at 64 keV] were chosen to counter-dope the subsequent p+ implant). The arsenic was driven in at 950 °C for 1 h to deepen the n+ contacts without further altering in the p+ implant profile. The remaining source/drains were formed with a self-aligning, blanket boron implant (1.0×10^{15} at 32 keV). This implant does not alter the previously doped n+ regions because the arsenic was at a higher dose and has a higher solid solubility than the boron.

Then a 0.6-μm layer of 8% phosphosilicate glass (PSG) was deposited, flowed for 20 min at 950 °C, patterned (Mask 5), and etched using a CHF_3/O_2 plasma to form the contact areas to polysilicon. Metal1 (0.5 μm of Al/1% Si) was sputter deposited, patterned (Mask 6), etched in a solution consisting of (parts by volume) 20:3:77 CH_3COOH:HNO_3:H_3PO_4, and dry etched in an SF_6/F115 plasma to remove the silicon residue. Next, an 0.6-μm-thick undoped low-temperature oxide (LTO) was deposited (this LTO does not contain phosphorous to avoid corroding the Metal1 aluminum with phosphoric

acid). The LTO was then patterned (Mask 7) and etched in a CHF_3/O_2 plasma to form vias for the Metal1/Metal2 contacts. After that, 1.0 μm of pure Al (Metal2) was sputter deposited, patterned (Mask 8), and etched in a 20:3:77 acetic:nitric:phosphoric acid solution. The Metal2 was covered with an LTO passivation layer (1.2 μm, undoped) deposited at two temperatures: the first at 300 °C and the second at 380 °C (the first temperature setting minimizes damage to Metal1 and Metal2, and the second temperature facilitates quicker deposition). This passivation layer was patterned (Mask 9) and etched using a CHF_3/O_2 plasma to form contact pads. This step concluded the CMOS process processing.

The first step in the bimorph organic actuator process was to deposit a 0.5-μm-thick mixed-frequency PECVD silicon nitride. This low-stress silicon nitride (<20 MPa) was patterned (Mask 10) and etched using a SF_6/CF_4 plasma to form etch-protection caps for the bond pads since the pads would be later exposed to an Al wet etch. A 2.0-μm layer of pure Al (Metal3) was deposited, patterned (Mask 11) and etched into both sacrificial mesas and interconnects. An adhesion promoter (PI-Coupler-3 from Hitachi Chemical Co. Ltd., Santa Clara, CA, USA [44]) was spun-on and cured at 350 °C for 30 min followed by the application of the first polyimide (polyimide

isoindoloquinazolindeione- or PIQ-L200 from Hitachi). This layer was cured in a nitrogen purged oven using a three step profile: 20 min at 105 °C, 30 min at 160 °C, and 60 min at 350 °C. The final, cured polyimide thickness ranged from 3.2 to 3.5 μm.

A 150-nm-thick PECVD silicon nitride layer was then deposited, patterned (Mask 12), and etched using an SF_6/CF_3Br plasma to from a hard mask used to define the vias between Metal3 and Metal4. The silicon nitride was re-patterned (Mask 13) and etched using an SF_6 plasma to form the lower encapsulation layer for the subsequently sputtered metals. (Encapsulation was seen as a precautionary measure to prevent corrosion of the metal that might occur due to the moisture permeability of the polyimide.) The nitride also acted as a mechanical stiffener for the actuator. Next, a 100-nm-thick layer of 50:50 Ti-W (Metal4) was sputter deposited, patterned (Mask 14), and etched in an SF_6 plasma to form the thin-film resistive heaters. Electrical connections between the Ti-W and the pure Al at the bottom of the polyimide via were made by sputter depositing a 1.0-μm-thick Al layer (Metal5). Upon patterning (Mask 15) and etching this Al layer in a 20:3:77 acetic:nitric:phosphoric acid solution, another 125- to 150-nm-thick PECVD silicon nitride layer was deposited, patterned (Mask 16), and etched using an SF_6 plasma to complete the metal encapsulation.

The second polyimide (Hitachi PIQ-3200) was then spun-on and fully cured (it was typically 3.1 to 3.3 μm thick) with the same three-step profile used to cure the PIQ-L200 polyimide. The final deposition was a 250-nm-thick PECVD silicon nitride. It was patterned (Mask 17) and etched using an SF_6/CF_4 plasma to form the outlines of the actuators and the openings the to bond pads. Prior to polyimide etching, the wafers were diced into individual chips. The polyimide layers were etched in an oxygen RIE plasma to form vertical walls down to either the silicon nitride over the bond pads or the sacrificial Al mesas (Metal3). The actuators were released from the substrate by wet etching the aluminum beneath the actuators in an 20:3:77 acetic:nitric:phosphoric acid solution. A final SF_6/CF_4 plasma etch was then done to remove the silicon nitride caps from the bond pads and the polyimide etch mask. The released actuators curled upward because the polyimides were cured at an elevated temperature and the upper polyimide has a higher coefficient of thermal expansion than the lower. This natural tendency to curl out of the substrate plane assisted the release process by reducing the chance of sticking and by allowing the wet etch to more easily reach the areas beneath the actuators (no actuator out of several thousand released has ever been observed to have remained stuck to the substrate).

C. Experimental Setup

1) Hardware: A custom-designed printed circuit board (PCB) was made to package the ciliary array chip and to provide the interface between the chip and the controlling personal computer (PC) system (see Fig. 7). A long-working distance microscope (Navitar, Rochester, NY) was attached to a CCD camera (Sony-IRIS-DXC-107A, Sony Electronics Inc.,

Park Ridge, NJ) in which its output was viewed on a television monitor and recorded on a VHS tape recorder/player. The PC system was used to provide the user interface in addition to sending command data to the array.

The circuit board was designed to accommodate up to four ciliary array chips [Fig 6(a)]. A square hole in the center of the board was made so that a copper heat sink could be fastened to it. If necessary, heat can be actively drawn away by attaching a Peltier cooling device to the bottom of the heat sink. The ciliary chip was first bonded to the copper heat sink using a high-temperature curable die attach. Once attached, gold wire bonds were made between the chip and PCB using a ball bonder.

The assembly includes two ports for receiving command data: a DB-25 connector that receives data from a standard PC parallel port and a 2×8 pin header array which can be used to send data directly to each column and row [see Fig 6(b)]. The 8-bit signal from the PC is routed to an octal bus buffer (74HCT244). The second shift register clock (*SClk2*) is generated on the board by the dual, monostable multivibrator (CD40948) and associated resistors/capacitors. The logic states of the shift registers can be monitored using an octal-bus transceiver (74HCT245) to receive data from the ciliary array. Alternatively, the bus transceiver can be used to directly load the rows and columns. (This requires 22 data inputs compared to the 8 input needed for operating the chip in serial mode.) The timing required to update the array in either serial or parallel mode is shown in Fig. 6(c).

2) Software: Except for the power supply voltage settings, the ciliary array chip was completely under software control. Diagnostic software was first used to verify that each motion pixel could be individually controlled. The major function of the software was to regulate the gait sequences or to alter the way the actuators induced translation. It also allowed the array to be subdivided into smaller fields that are needed for doing vector field manipulations. Having the chip under software control enabled an unprecedented level of flexibility in operating a MEMS ciliary actuator array. A variety of low and high-level software functions have been programmed for both linear translation and squeeze field based manipulations [46].

Control software was written in PASCAL and was implemented on a 80486-based PC. Signals were transferred by using the parallel port of the PC. The ports 8 data bits consisted of the *DataTop*, *DataRight*, *DataLeft*, and *DataBottom* bits for activating the appropriate actuator, the *Load* and *Xfer* bits for writing the actuator state and activating the actuators, the *SData* (serial data) bit for writing addressing information into the shift register, and the *SClk1* bit.

a) Low-level and benchmark functions: A number of functions were used for testing of the basic functionality of the ciliary chip hardware.

- Write One Byte. This function allowed writing arbitrary user-specified test patterns without the need for function or word generators.The data can be typed in as binary or hexadecimal number.
- Write Byte Sequence: A sequence of control signals was written at a user-specified frequency. These sequences usually consisted of a data signal for the actuator flip-
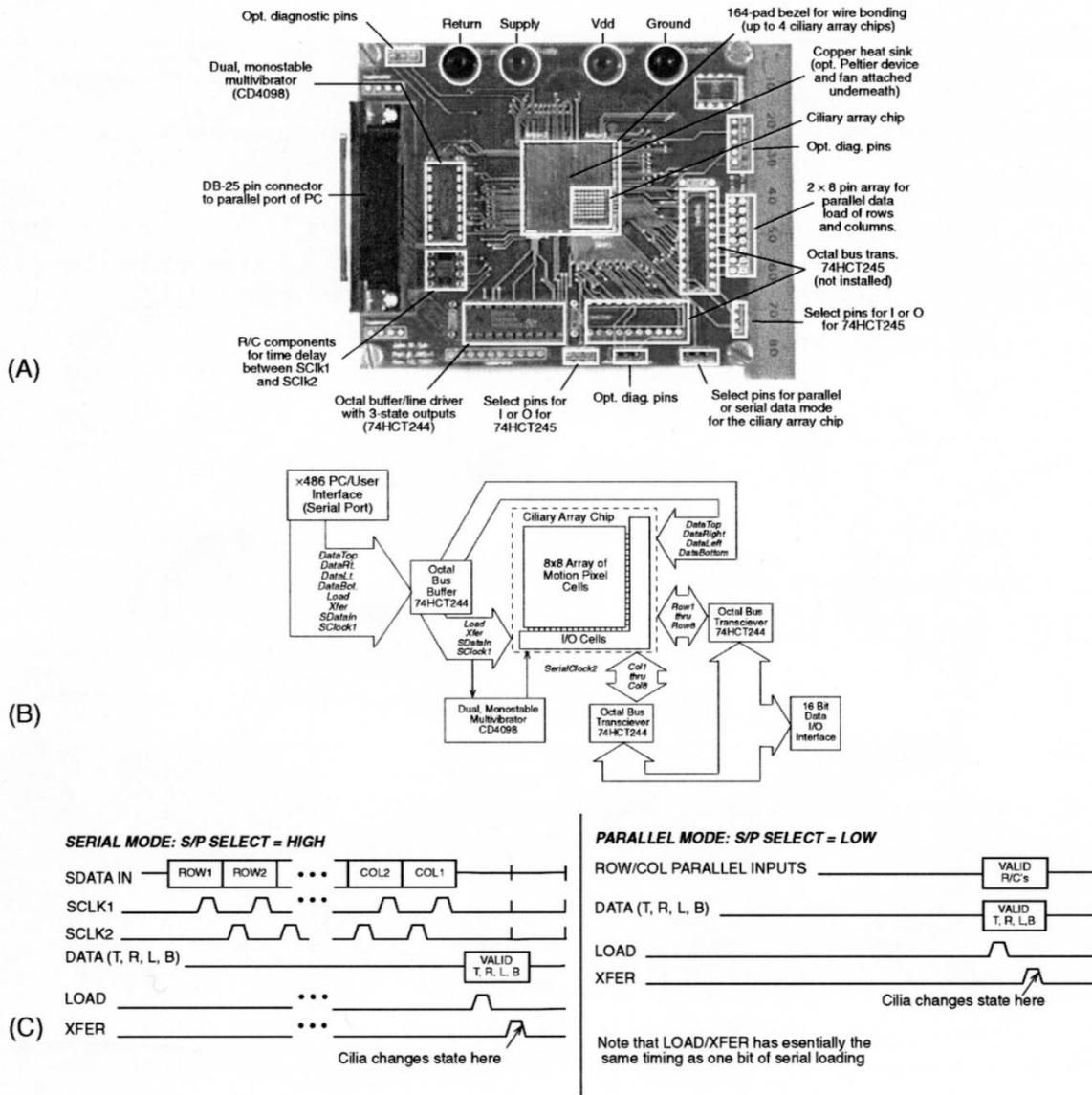
Fig. 6. (A) Overview of the general purpose micropositioning system. The CMOS ciliary array chip is packaged in a custom circuit board designed to operate up to four chips shown at the top figure, with a centimeter ruler shown along its right edge. (B) The block diagram shows the relation of the various components and connectors to the ciliary array chip. (C) The timing diagram illustrates how the array can be operated in either serial or parallel mode.

flops or for the address register, followed by triggering of the *SClk1* bit.

- Move One Actuator: This function allowed a user to specify the address of an actuator. The software then generated a sequence of signals to: 1) rewrite the data in the address register; 2) rewrite the data in the motion pixel; and 3) activate the motion pixel.
- Scan All Pixels: All actuators in the ciliary array were triggered in sequence at a user-specified frequency. This allowed easy visual inspection of malfunctioning cilia.
- Speed Test: A sequence of bytes was continuously written to the parallel port at a high frequency. This allowed determining the maximum switching speed of the CMOS circuitry.

b) High level functions: An actuator moved only if the data bit in its corresponding phase register was changed.

Therefore, the actuators required a continuous flow of control signals. In general, these signal sequences consisted of address data, motion pixel data, and clock signals, which all depended on the intended array vector field. The software wrote a specific sequence of signals to the parallel port in real time.

Software for the higher level functions allowed the user to manipulate an object in a preprogrammed or in an interactive manner. Several useful control strategies were preprogrammed and can be chosen from a menu such as linear translations for moving a part in the up, right, left, or down direction and vector fields for orienting a part along a vertical or horizontal squeeze line. For each of these strategies, a sequence of control signals was repeatedly written to the parallel port and can consist of many hundreds of individual byte signals. Implementation of Bresenhams line scan algorithm [45] lead
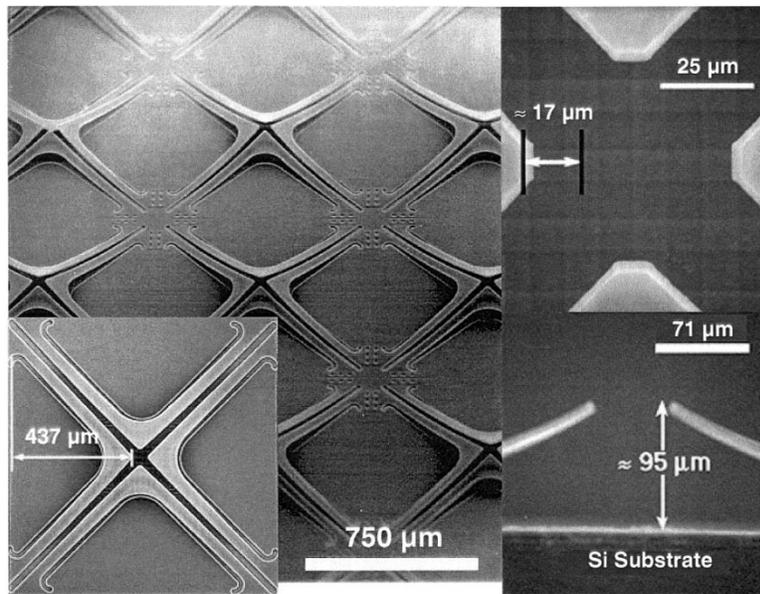
Fig. 7. SEM micrographs of ciliary array after complete fabrication. The image on the left shows a group of actuators from the array with the plan view of one motion pixel cell inset at the lower-left. Each motion pixel is 1×1 mm in size. The two images on the right were used to measure vertical and horizontal tip deflections, which were 95 and 17 μm, respectively.

to the development of an interactive mode in which a user could, through keyboard commands, move an object along any vector and at a variety of rates.

III. OBSERVATIONS AND EXPERIMENTS

Five main sets of observations and experiments were done with the arrays. The first were microscope-based observations of the completed actuators and arrays. The second (and perhaps the most critical) set of experiments were done to verify that the ciliary actuators were successfully integrated with the CMOS circuitry. The third set of tests centered on characterizing the array as a positioning tool using silicon dice cut from wafers as the test objects. (Silicon dice were used because our previous work with the passive ciliary arrays have shown that the flatness and relative smoothness of the dice facilitate the translation and vector-field tests. Also, wafers in a variety of thicknesses are commercially available should thinner or thicker samples than standard be needed.) The fifth set of tests were done to demonstrate various vector-field theory based manipulations [46], [47] enabled by CMOS integration. The overall observations and results from these experiments would also be the basis for evaluating the yield of the fabrication process.

Following the microscope based inspections of the completed chips, the initial experiments were done on a test device representing a subsection of the array to verify the integration between the on-chip circuitry and the ciliary actuators. (The ciliary array was essentially a tiled version of this test module.) In order to verify the integration, five modules containing a single motion cell and peripheral logic circuitry were tested. The ciliary actuators were connected to a variable power supply, and the logic circuitry was connected to a separate power supply set to 5 V and current limited to 100 mA.

Because serial data loading simplifies the data input to the actuators, it was important to check the peripheral circuits located on two sides of the perimeter of the chip. Two ciliary array chips were used to see if the shift register chain was operational by setting the *S/P Select* pad at logic HIGH, connecting the *SClk1* and *SDataIn* pads to a digital word generator (HP 8006A), and monitoring the *SDataOut* pad.

Tests were also done to characterize the ciliary array as a simple x-y positioning tool for silicon dice. Both a three- and a four-part gait were used to in these experiments, and, to our knowledge, the three-part gait has not been previously reported in the literature on this kind of micromachined actuator array. Two sets of experiments were conducted for each type of gait-constant input voltage to the actuators and varying the time interval per gait, and constant time interval per gait and varying the input voltage. For each setting in each type of experiment for both kinds of gates, five or six runs were videotaped and the relative displacement of the silicon die was determined by comparing the images taken at the start and finish of each run. The estimated distance was then recorded into distance per gait and plotted against either voltage or gait interval.

Three kinds of vector field experiments had been done on the previously reported arrays that were not integrated with CMOS circuitry [15]. However, those demonstrations required the arrangement of two or four ciliary arrays because the arrays had no provision for subdividing the array into two or more different vector-fields. Identical demonstrations were implemented here with only one ciliary array chip. In addition, a universal feeder-orienter (which can uniquely orient nonsymmetric parts) experiment was conducted. The combination of the linear translation and vector-field experiment was intended to show the general purpose functionality (specifically, arbitrary x-y translation and ϕ rotation) of this ciliary array.
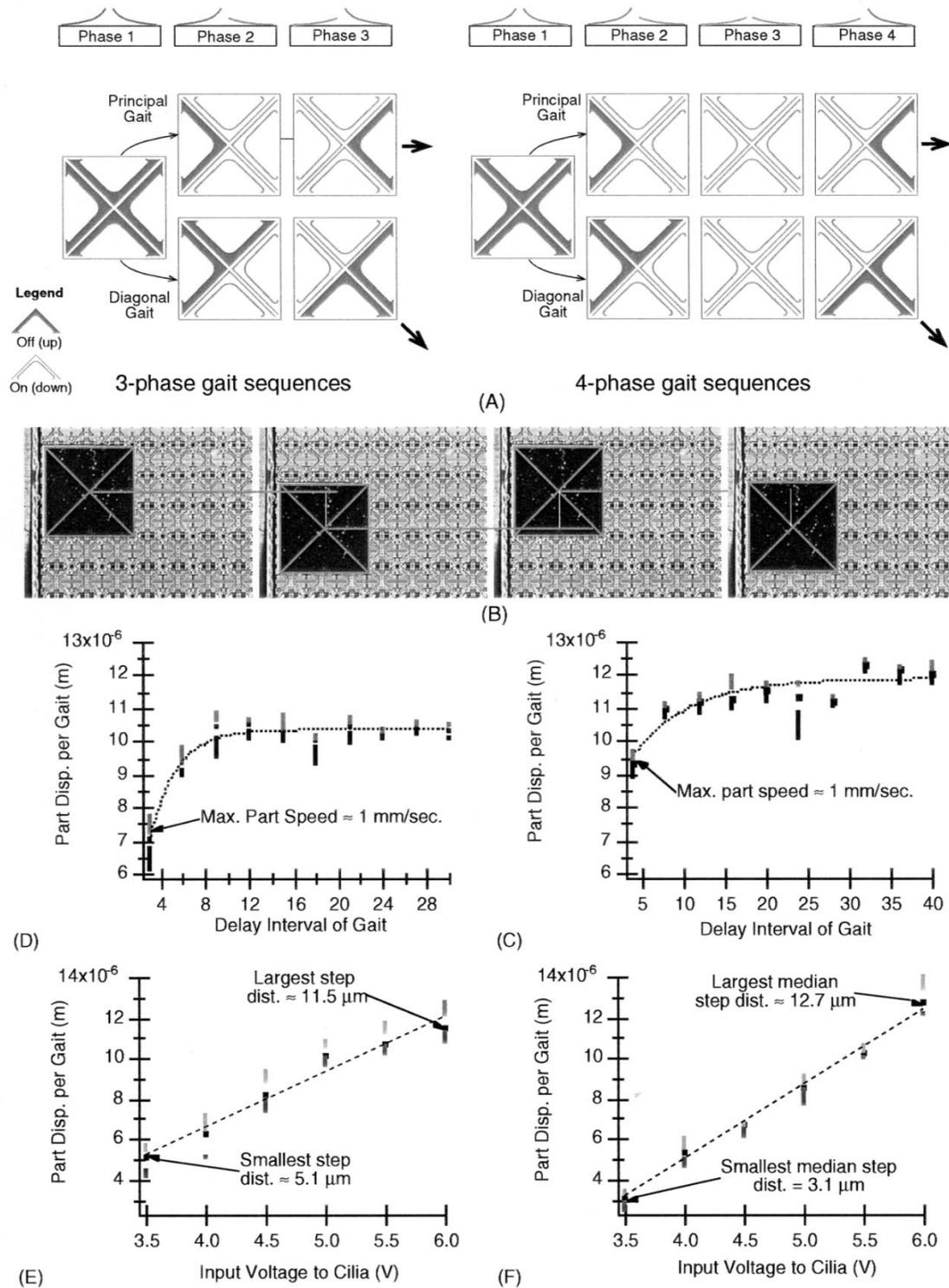
Fig. 8. (A) Illustration of standard and virtual (diagonal) three- and four-phase gaits. (B) The four video frames are examples from tests characterizing the linear positioning performance of the ciliary array on a 3 × 3 Si die (≈100 μm thick). (C and D) Part displacement versus gait time interval, and (E and F) part displacement versus input voltage for three- and four-part gaits, respectively.

IV. RESULTS

A. In and Out-of-Plane Displacements

The "first silicon" run of the 17-mask CMOS Integrated MEMS process consisted of a batch of three 4-in wafers. These three wafers were diced, and approximately 20 chips were sent through the actuator release procedure for subsequent packaging and testing. A random pick of one chip out this batch was chosen for observation and in a SEM, from which micrographs were taken and are shown in Fig. 7. The photo shows a displacement at tip of ≈95 μm vertically (out-of-plane) from the substrate compared to the FEM simulation
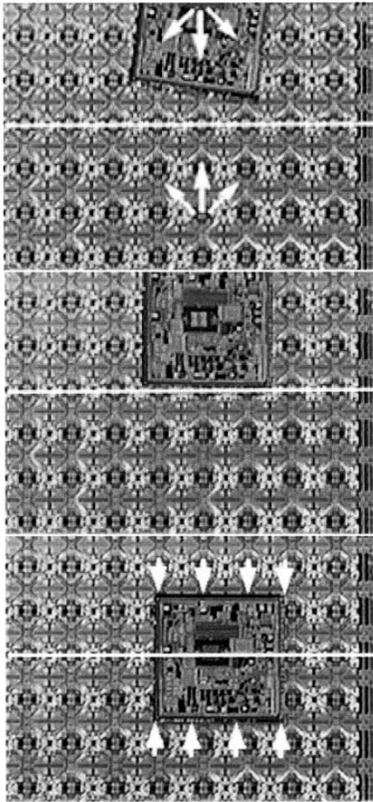
Fig. 9. The three images are from a video taken during a squeeze field manipulation test. Two diagonal gaits are used to produce a net perpendicular motion to the horizontal squeeze line (see top image). The middle frame shows the part about to make contact with opposing linear field. Bottom frame shows the part in rotational and translational equilibrium about the squeeze line.

result of ≈ 100 μm. The in-plane (horizontal) displacement of ≈ 17 μm. While this is less than the thermal/electrostatic ciliary array reported in [15], the ciliary actuators appeared to have sufficient displacement for moving the test objects, as discussed below.

B. CMOS Integration and Serial Data Loading Circuitry

For the five test modules [see Fig. 1(c)] tested for CMOS integration, all worked as expected, and the power required to achieve full deflection (in ambient air) ranged from 35 to 38 mW (input voltage range: 6.0–6.3 V; input current range: 5.5–6.4 mA). Full deflection was estimated by visual inspection of the actuators under a light microscope as the voltage increased and observing when the Ti–W heater resistor was fully planar. On the array chips in which the shift register chain was tested a data transfer rate of 25 kHz was achieved, which was higher than necessary to run the manipulation tasks (described below). Since both the basic CMOS circuit-to-actuator integration and the serial loading circuits tests were positive, the experiments on the array (translation and vector-field) were carried out and are summarized in the paragraphs below.

C. Simple Translation Experiments

1) Linear Translation with Principal Gaits: Both a three- and a four-part gait [Fig. 8(a)] were implemented and demon-

strated using a $3 \times 3 \times 0.1$-mm silicon die (wafers from Virginia Semiconductor, Inc., Fredericksburg, VA) weighing 1.7 mg [Fig. 8(b)]. The results from the constant voltage and constant gait interval tests are summarized in Fig. 8(d)–(g). The constant input voltage/varying gait interval tests suggest that the part displacement is characteristic of the temperature rise in thermal actuators [Fig. 8(d) and (e)] [47]. The constant gait interval/varying input voltage tests show a fairly linear relationship between part displacement and voltage [Fig. 8(f) and (g)]. The lowest input voltage was determined on the basis where consistent stepping of the test object was observed. The highest input voltage was set where the actuators appeared to be flat (or nearly so) based on visual observation.

2) Translation with Virtual Gaits: The secondary method of moving an object were gaits that move objects directly along the arrays diagonals (e.g., top-right or bottom-left). Since two actuators are commanded to act as one, diagonal gaits done in this way are also called virtual gaits. Both three- and four-part gait patterns can also be implemented as virtual gaits. In translation tests with a $3 \times 3 \times 0.55$ mm Si die (8.6 mg), the standard, linear translation gaits could only intermittently move the die, however, a four-part virtual gait was able to position test objects. Modulation of step size by varying voltage was not evaluated since only at the highest voltage input settings to the actuators (6.0–6.5 V) did the object move consistently.

Since at the motion pixel level the virtual gait has a 50% duty cycle, the total average power consumed by the entire array per gait was 5.0 W (each actuator receiving ≈ 35 mW) with a 6.0-V input to the actuators. The virtual-gait pattern uses the less power for a given input voltage than the principal-gait because its duty cycle for actuator hold-down is 75%. Another feature of virtual-gait is that with two ciliary actuators working as one, the lifting capacity is effectively doubled. This feature was useful in this case where a 0.55-mm-thick Si die was used as the test object. The 0.55-mm-thick Si die loaded the ciliary actuators with a force per unit area of ≈ 9.4 μN/mm^2 whereas the 0.10-mm-thick Si die exerted nearly 1.9 μN/mm^2.

D. Vector Field Experiments

1) Squeeze Field: To carry out this experiment the ciliary array was subdivided horizontally into two fields' each consisting of 8×4 (horizontal squeeze line) array of motion pixel cells. Squeeze fields with both principal and virtual-gaits were implemented. In the example shown in Fig. 9, virtual-gaits were used because a $3 \times 3 \times 0.55$-mm Si die was used as the test object. The diagonal gaits had equal proportions $\pm 45°$ to produce a net translation toward the squeeze line (that is, the skew factor [46] was zero). Images from the video taken during these experiments are shown in Fig. 9.

2) Centering: The squeeze field demonstrated above achieved a centering effect only along one axis. A radial field can center an object in two dimensions. With the previous generation of four-quadrant passive ciliary chips [15], [16], an approximation of the ideal radial field was implemented, however the gaps in between the four chips used hindered smooth translation of the part. With the CMOS integrated
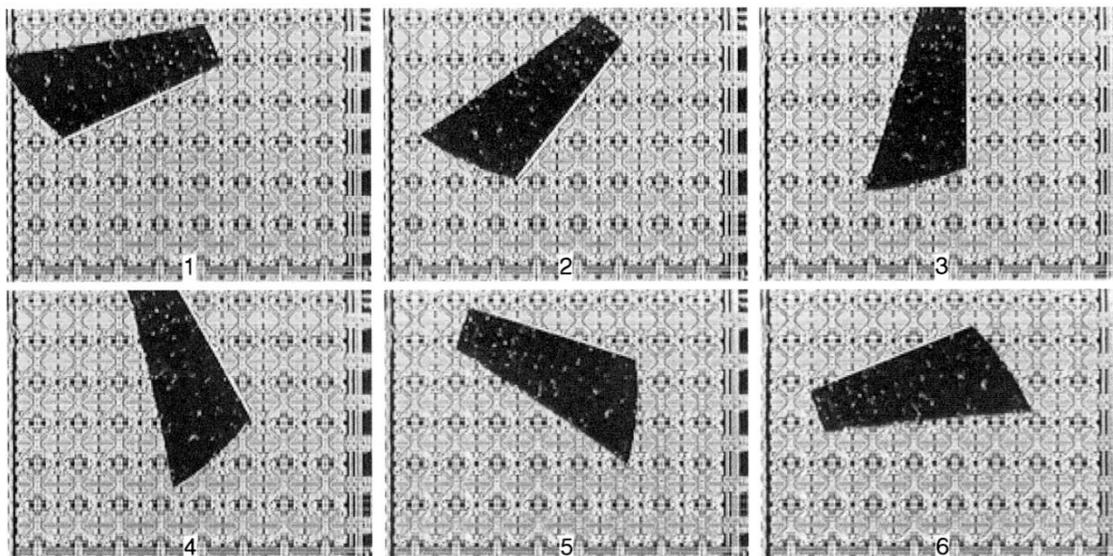
Fig. 10.   Six images from a video taken during a centering experiment. A stable configuration is reached by the object int his radial field.

ciliary array, a single chip sufficed to generated such a field. Part centering was demonstrated in with a nonsymmetric part ($\approx 1.1 \times 5.3 \times 2.5 \times 4.3$ and 0.1 mm thick) and representative images are shown in Fig. 10.

3) Rotation: Squeeze fields and radial fields cause stable equilibria in parts placed onto them. In the previous two demonstrations, this effect was exploited to perform open-loop positioning and orienting strategies, and to predict the final orientation of a part. However, an equally useful task might be the continuous translation and rotation of a part, for example, inspection of micromachined parts under a light or scanning electron microscope [48].

A field that causes rotation was described by Fujita [49] and Liu and Will [50]. The four quadrants generate forces in the left, right, up, and down directions, creating a discretized vortex. This field was implemented by dividing the ciliary array into four 4×4 subarrays and a sampling results from that experiment is shown in Fig. 11. With the previous ciliary array [15], [16], this demonstration was implemented by a skewed squeeze field generated by two chips, however that demonstration was hindered because the rotation occurred on top of the gap between two separate chips. Furthermore, the field was not selfcentering so the part tended to drift in a path parallel to the gap. The current implementation provided control over rotation rate and part centering.

4) Universal Feeder-Orienter: In [51] it was proposed that there exist a force field that every nonsymmetric planar object has only one unique equilibrium. A part feeding and positioning device such as this has been termed a universal feeder-orienter (UFO) because it could uniquely position a part without the need of a clock nor information of the objects position from sensors. Nor would the device require sequencing vector fields or hardware adjustments even though a design of a part has changed. While simulations of a UFO device have been developed showing this property, no physical demonstrations have been reported and only recently has a rigorous proof been presented [52].
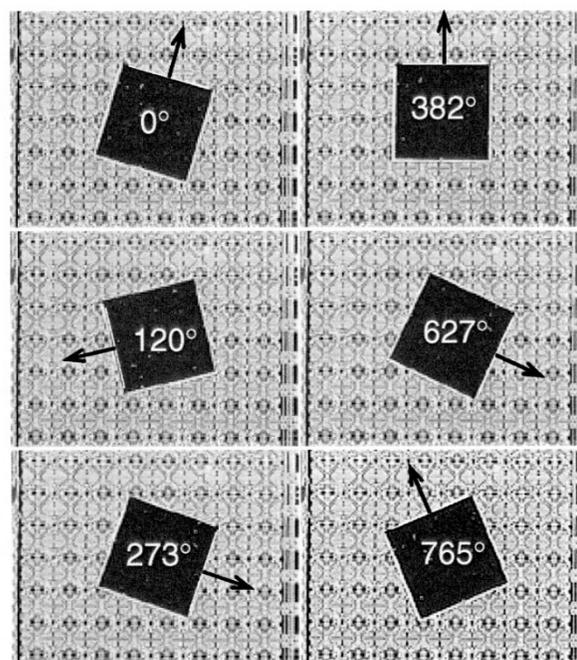

Fig. 11.   These images are from a video taken during a rotation demonstration of a $3 \times 3 \times 0.1$-mm Si die. The input voltage to each ciliary actuator is approximately 5.0 V. A four-phase gait with a gait interval of 4 was used and resulted in a rotation rate of ≈ 35 s/rotation. The die rotated continuously in this demonstration, however, just over two complete revolutions are shown.

In [53] it was also stated that a combined radial and "gravitational" field $R + \delta G$ would have this property (δ is a small positive constant, and G is defined as $G(x,y) = (0,-1)$). This concept was implemented with the CMOS integrated ciliary array by running a centering field program and tilting the array at a small angle ($\tan \phi = \delta$) to introduce a gravitational component. In one set of experiments a slightly nonsymmetric silicon piece (0.10 mm thick) was used. When $\delta = 0$, the piece tended to rotate and no unique equilibrium
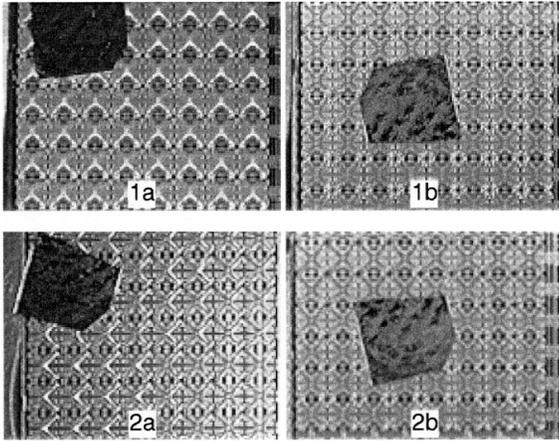
Fig. 12. Video frames from two "universal field" experiments. Though the starting positions are similar the final positions are different due a change in the tilt direction. For (1) the bottom portion of the array is tilted and for (2) the right side is tilted higher.

was observed. When a tilt ($\delta \approx 0.125$ rad) was introduced the object tended to reach a stable and unique equilibrium. Two instances are shown in Fig. 12 in which the initial position of the object on the array was similar, and yet the final stable positions were different.

V. DISCUSSION

A total of nine ciliary array chips were packaged during the testing portion of this paper. Of the nine, five arrays were fully functional while the remaining four had reduced functionality due to unknown problems in the circuitry which may be related to processing. All nine arrays had no visible mechanical defects and there were no unreleased actuators. Furthermore, there were no signs of thermal damage and no signs of polyimide delamination in the actuators or in the actuator-to-CMOS interface. Considering that these chips were chosen at random from the very first completed run of this experimental process and that the processing was conducted in a general-purpose multiuser microfabrication facility, the overall fabrication yield was regarded to be good.

In terms of the actuators alone, the lifting capacity was not as high as expected. The original FEM simulations indicated that the lifting capacity was ≈ 80 μN; however, these experiments indicate that the lifting capacity was less. The finite element model originally developed to study the lifting capacity of the actuator was checked, remeshed and the load-deflection simulations run again after it was suggested that the original mesh might have led to an erroneous result. The new simulation results indicated that the actuator's lifting capacity was nearly 23 μN which is only a factor of two greater than the force per unit area (≈ 11 μN/mm^2) of the 0.55-mm-thick Si die used during testing. This result explains the difficulties seen when attempting to transport parts that are heavier than the 0.55-mm-thick Si die. Therefore, the reason for the difference in the predicted force level and observed lifting capabilities was due to the sensitivity of the simulation to the actuator's mesh representation. However, the design of

the actuator did allow for improved quality of movement over the previous (thermal/electrostatic) ciliary actuator: at nearly any gait interval the actuators moved with nearly the same repeatability and consistency.

VI. SUMMARY

The ciliary chip described herein is the first micromanipulation array fabricated directly on top of control circuits. This level of integration enables each actuator to be separately addressable and turns the array into a reconfigurable micromanipulation device. The design of the previous ciliary array described in [15] and [16] limited it to performing linear translations. The current array was designed to perform simple array manipulations such as linear and diagonal translations and more complex vector-field manipulations such as orienting, alignment, and centering in addition to arbitrary linear translations (without having to tile chips together as was done previously). All these demonstrations were successfully performed including a new three-part gait and a universal-feeder orienter, which may be a forerunner to a new generation of part feeding and positioning devices that do not need a clock, sensors, reprogramming, nor hardware changes to uniquely align arbitrary polygonal objects.

Realization of this ciliary array was carried out by surface micromachining polyimide-based actuators on substrates with prefabricated CMOS circuits. Validation of this approach was achieved through the demonstration of the chip as individual motion pixels, single, and subdivided vector fields each of which was controlled via keyboard control from a PC. A total of nine chips were packaged for the tests in this paper, and of those, five performed as designed. And at no time during testing were there problems of thermal degradation or loss of adhesion between layers.

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Henry Baltes (M'81), for a biography, see this issue, p. 432.

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