A Low-Power High-Speed High-Resolution Zero-Crossing Based Pipelined Analog to Digital Converter

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Abstract

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In this dissertation, techniques with zero-crossing based circuits (ZCBC) to achieve high speed and high resolution in scaled technologies with very low intrinsic gain are proposed. A coarse phase followed by a level shifting capacitor for a fine phase current source is employed to achieve higher accuracy and sub-ADC flash comparators are strobed immediately after the coarse phase for high frequency operation. The systematic offset voltage between the coarse and fine phases manifests itself as systematic offset in the sub-ADC comparators. This offset is caused by the coarse phase undershoot and the fine phase overshoot. It is cancelled with background calibration by residue range correction circuits within the following stage's sub-ADC. The sub-ADC's random comparator offset is calibrated with a discrete-time charge-

pump based background calibration technique. A prototype device based on the aforementioned concepts was realized in a 55nm CMOS process. The ADC occupies 0.282 mm^2 and dissipates 30.7mW. It achieves 64.6dB SNDR and 82.9 dBc SFDR at 200 MS/s for a FOM of 111 fJ/conversion-step. The SNDR degrades gracefully above the designed sampling frequency to 62.9 dB at 250 MS/s, and remains above 50 dB at 300 MS/s. To minimize the power consumption further when using the ZCD technique, a dynamic biasing technique is proposed and employed. The bias current feeding the ZCD preamplifier is dynamic and depends on input ramp voltage. This method reduces current consumption by supplying bias current only when needed during a zero crossing event. This ADC consumes 27.1mW and achieved 61.2 dB SNDR for a FOM of 143 fJ/step.

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Dedication

To my family

1 Introduction

Analog-to-Digital converters (ADCs) are a fundamental building block in modern integrated circuits which serve to process, and convert real world analog signals into a format where digital signal processing and computation may take place. Applications are virtually ubiquitous from sensors which detect temperature, and acceleration, to interfaces for image processing and converters for uses in wireless and wireline communication channels. The rapid growth of portable electronic systems such as tablet computers, cellular phones, portable music players, laptop computers, and components for autonomous long-battery life sensor applications has made power consumption one of the most critical performance factors in the consumer electronics to enhance battery life, or perhaps eliminate batteries altogether. As CMOS processes continue to scale, the increased device cutoff frequency and the associated smaller parasitic capacitance allow more power efficient and faster logic which improves the performance of the digital electronics, allowing more sophisticated and larger systems on a single chip.

However, these same scaling properties fundamentally challenge the design of analog integrated circuits because of lower intrinsic transistor output resistance, lower power supply voltages, and increased leakage currents. In short, the inherent gain associated with a single-transistor stage ($g_m r_o$) decreases with finer geometry CMOS processes. Simultaneously, the available output swing is reduced due to the lower supply voltages which are mandated by device reliability concerns. Thus, the design of high gain, low noise op-amps has become the main bottle-neck in many switched-capacitor based circuits. A parallel trend with respect to analog-to-digital converters is the demand for higher resolutions and sampling rates. This is all set in the context of ever-present constraint on area and power consumption. Pipelined ADCs,

given their area and power efficiency, are an excellent architecture to simultaneously achieve both high sampling rate and high resolution [1]-[5]. However, most pipelined ADCs require high-gain op-amps for accurate residue amplification. Op-amp-based switched capacitor ADCs rely on a principle of charge transfer where the closed-loop gain depends on a ratio of capacitor values which is relatively insensitive to process, voltage, and temperature (PVT) variations.

However, the accuracy and tolerance to PVT variations in the closed-loop gain relies on a sufficiently large DC open-loop op-amp gain. Moreover, the op-amp closed-loop bandwidth and settling time in switched-capacitor circuits are limited by the need for sufficient phase margin. To improve the DC open-loop gain of the amplifiers, design techniques such as cascaded gain stages or gain boosting must be employed, which result in increased power consumption. Other techniques to overcome the challenges presented by modern silicon processes include calibration algorithms that can tune the closed-loop gain error using low gain op-amps with incomplete settling due to limited bandwidth or poor linearity of the residue amplifier [6]-[8]. However, foreground calibration algorithms, normally performed at power-on or during periods of inactivity of the converter, are frequently employed, but any sudden environmental changes may make the calibration result invalid. On the other hand, background calibration can track real-time environmental changes but can require additional power and complexity, as well as slower or less-effective calibration results compared to foreground calibration.

Zero-crossing based circuits (ZCBC) are an alternative to op-amp switched capacitor circuits where the op-amp is replaced with a zero-crossing detector (ZCD) and a set of current sources [9]-[14], [16]-[22]. A ring amplifier [23], [46] was introduced as another alternate approach for op-amp based circuit in scaled technologies. However, this method has been limited

to sampling rate of 100 MS/s to date. The ring amplifier approach has similar stability issues like the op-amp-based approach since it uses several inverters as gain stages in the feedback. Compared to op-amp based circuits, ZCBC are more power-efficient because they detect a virtual ground condition rather than utilizing an op-amp to force a virtual ground. The largest source of nonlinearity in ZCBC is the nonlinearity of the ramp caused by the finite output resistance of the current sources. In this work circuit techniques that improve ADC speed, ramp linearity and comparator offset are proposed, including an early sub-ADC decision, unidirectional dual ramps with level shifting capacitors, and residue range calibration.

The dissertation is organized as follows. Chapter 2 discusses the various ADC architectures. Chapter 3 gives a brief overview of published ZCBC pipelined ADCs. Chapter 4 describes design issues related to high speed and high resolution ZCBC ADCs. Following this, Chapter 5 presents implementation details of a high resolution high speed ZCBC ADC and its building blocks. Chapter 6 describes a low power dynamic ZCD and implementation. Chapter 7 summarizes measurements. Finally, conclusions are drawn in chapter 8.

2 Overview of ADC Architectures

An ADC converts signals from the analog domain, which is continuous in time and amplitude, to the digital domain. Converting to the digital domain requires processing in two steps, sampling the applied analog input signal, and quantizing it to its digital representation by comparing to reference voltages. Many architectures of analog-to-digital converters are chosen and developed based on the best combination of speed, area, power consumption and accuracy for each application. In this chapter, we will review characteristics of several ADC architectures.

2.1 Flash ADC

This architecture is the fastest and simplest ADC as shown in Figure 2-1. The N bit analog-to-digital (A/D) conversion can be implemented by comparing simultaneously the input signal to the reference voltages generated from a resistor string with ~ 2^N comparators. The differences between input and reference voltages are amplified to digital levels and it generates a thermometer code. Then, this code is encoded to binary or gray code. The advantage of this architecture is that only one clock cycle is required to make the A/D conversion. However, the power consumption of this architecture increases exponentially as the resolution increases. For instance, while a 6 bit flash ADC requires 63 comparators, a 12 bit flash ADC requires 4095 comparators. The power consumption and input capacitance from such a large number of comparators are unrealistic for practical implementations. In addition, the comparator offset requirement becomes exponentially smaller with the resolution.

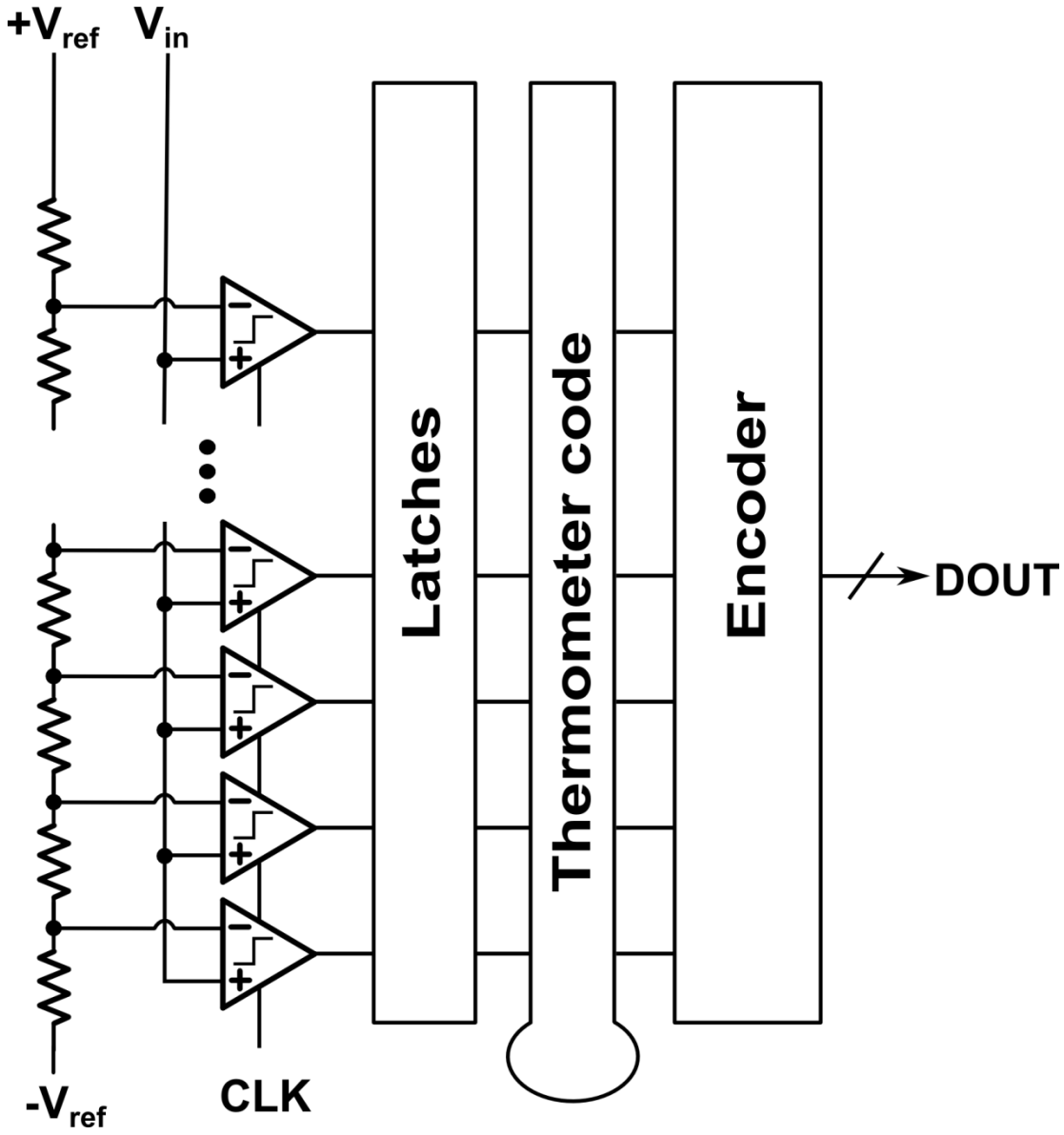


Figure 2-1: A flash architecture.

Another big disadvantage of flash architectures is the fact that the input bandwidth is usually much lower than the sampling frequency without a dedicated input sample and hold (S/H) circuit because the signal source has to drive many comparators at the same time. Any mismatch in the signal paths may result in wrong decisions due to all signals being in parallel. This error degrades the overall signal-to-noise ratio (SNR) for high frequency input signals. At higher

resolutions, this problem becomes worse since a large number of comparators laid out over a large area have more process variation and the error budget gets tighter with smaller least significant bit (LSB) size. Therefore, this architecture is only attractive for applications that require 6-bits or less resolution.

2.2 Folding ADC

Folding and interpolating ADCs are suitable for mid to high speed (several hundred MS/s) applications in the 8-10 bit range. Similarly to flash ADCs, folding ADCs can convert the input signal in one clock period. In addition, the number of comparators can be dramatically reduced because instead of comparing the input signal to all the possible thresholds of an N-bit quantizer with 2^{N-1} comparators, the most significant bits (MSBs) and the LSBs are separately quantized with one comparator array (2^{M+1}) for the MSBs and another array (2^{N-M}) for the LSBs, where N is the total number of bits and M is the number of bits in the coarse converter. For an N-bit flash ADC, 2^{N-1} comparators are required. In the case of a folding ADC, the required comparator number is reduced to $2^{N-M} + 2^{M+1}$.

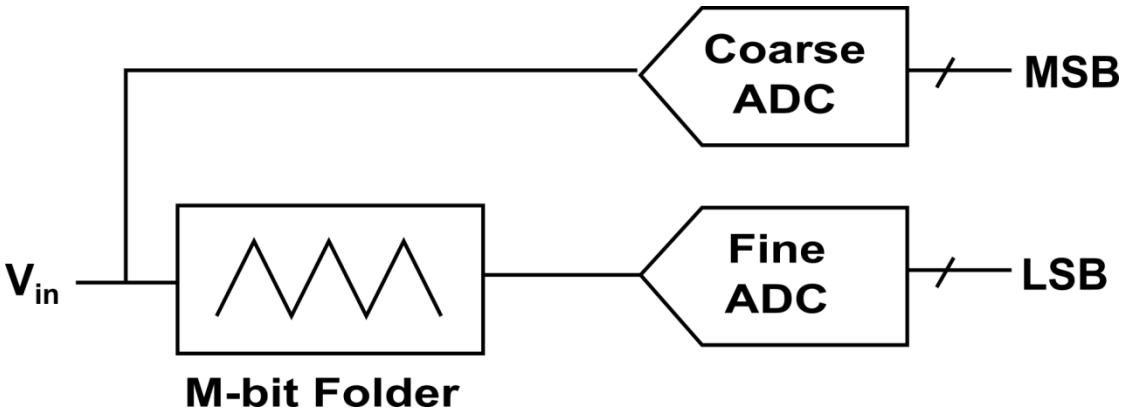


Figure 2-2: A folding architecture.

Figure 2-2 shows a simplified block diagram of a folding A/D converter architecture. Compared to the flash ADC, an additional preprocessing circuit and bit synchronizer are needed. The preprocessing circuit is needed to fold the input signal into several identical segments. In each segment, the folded signal is compared with reference voltages for LSBs generation. Since MSBs and LSBs are quantized separately, the coarse and fine quantizer offset difference can falsely generate a huge nonlinearity by pointing to the wrong segment of the folded signal. The digital output of the fine quantizer and the coarse quantizer are used to correct the nonlinearity caused by inconsistent offsets of the coarse and fine quantizers. One disadvantage of the folding architecture is the strict linearity requirement on the folded signal that affects the linearity of the quantizer.

2.3 Two-Step Flash ADC

Another way to reduce the number of comparators in the flash ADC is to separate the coarse and fine conversion into two time periods. A conceptual block diagram of this approach is shown in Figure 2-3. The input signal is first sampled on the sampling capacitors of both coarse and fine comparators. The coarse conversion is then performed by the N/2 bit coarse flash ADC. According to the outcome of the coarse conversion, the quantized signal is subtracted from the input signal and the residual voltage is again quantized by the N/2 bit fine flash ADC. The corresponding digital output is generated by collecting bits from both coarse and fine ADCs. During this process, a total of three clock periods is required per sample for input sampling, coarse conversion and fine conversion. Although the number of comparators is greatly reduced compared to the flash architecture, path mismatch is still a major problem and the input bandwidth is limited to a relatively low frequency compared to the conversion rate. The

comparator accuracy must also still meet the full resolution requirement and the offset voltage of the comparator must be less than an LSB. The overall linearity of the converter is determined by the front-end S/H, the intermediate DAC and the gain stage.

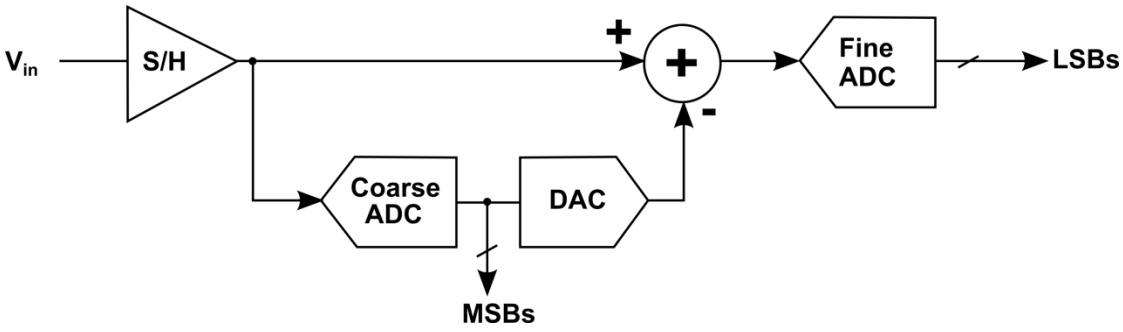


Figure 2-3: A two-step architecture.

2.4 Successive Approximation ADC

The successive approximation converter architecture shown in Figure 2-4 usually consumes very low DC power. Excluding the digital-to-analog (DAC) power, it dissipates only comparator and switching current. The conversion algorithm is based on successive approximation register (SAR). A SAR ADC uses a comparator and an N-bit DAC. The comparator compares the analog signal with the reference voltage generated by the DAC. The architecture also implements S/H to convert the continuous time signal into a discrete time signal. Conversion begins by turning on the MSB input on the DAC and comparing the input signal with the DAC output. If the input signal is greater than the output of the DAC, the MSB and the next lower bit of the DAC are turned on and another comparison performed. This will continue until the DAC output is within ½ LSB of the input signal. Thus, for N-bit output this converter needs N cycles.

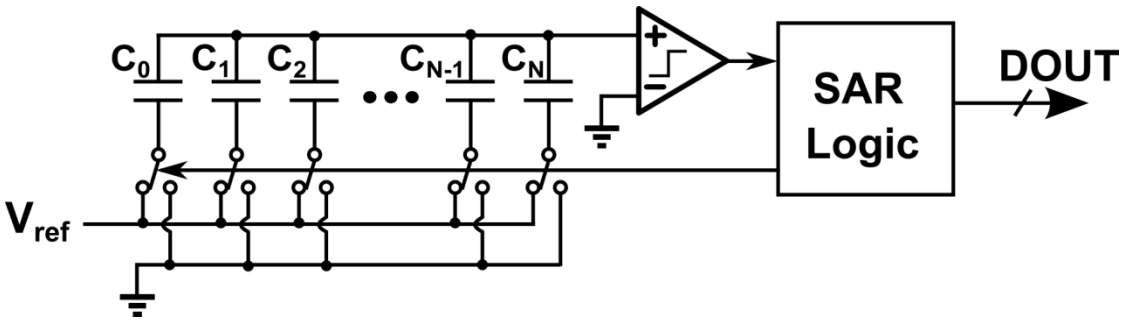


Figure 2-4: A SAR architecture.

One of the key features of this converter is that it requires very few analog components. The overall linearity of the converter is limited by the linearity of the DAC and S/H circuits. SAR ADCs have very low power consumption and low cost but they are also low speed because N cycles are needed for a single conversion. Thus, it is ideally suited for applications that require high resolution but low speeds.

2.5 Pipelined ADC

A pipelined ADC is a multi-step quantizer in which digitization is performed by a cascade of low resolution ADC stages which work on successive input samples as shown in Figure 2-5. Each sub-stage samples the amplified residue signal from the previous stage and quantizes it to M bits. The quantized signal is then subtracted and the residue amplified through an interstage amplifier so it can be sampled by the subsequent stage.

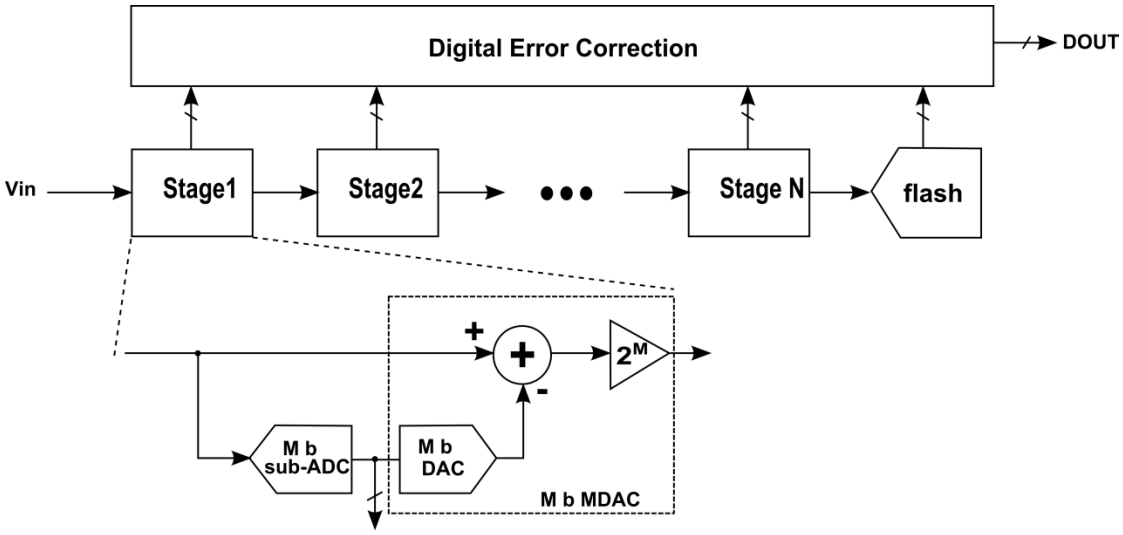


Figure 2-5: A pipelined architecture.

The same procedure is repeated in each stage to perform A/D conversion. The number of comparators required is the product of the number of stages and the number of comparators in each stage. The required number of stages is approximately the ADC resolution divided by the effective per-stage resolution.

The sub-ADC in each stage has to be only M bits of resolution due to the interstage gain and digital correction. Therefore the lower the M relaxes the more the comparator requirement. Both interstage amplifier and DAC requirements get relaxed on later pipeline stages.

2.6 Noise Shaping ADC

Noise shaping ADCs use oversampling. The signal band occupies a small fraction of the Nyquist interval making it possible to use digital filtering on the relatively large fraction of the quantization noise. It consists of ΔΣ modulator and digital filtering to achieve high resolution from a single bit quantizer. As shown in Figure 2-6, a basic noise-shaping ADC has an integrator, comparator (1-bit quantizer), digital filter and 1-bit DAC. The noise-shaping structure transfers most of the quantization noise outside the signal band with oversampling. Thus filtering in digital domain can achieve very high SNR since it removes the noise in the high frequency. Noise shaping ΔΣ modulator have found wide spread use in audio applications where the Nyquist frequency is several orders of magnitude lower than the process f_t. In addition, nowadays this type of ADCs is widely used in wireless receivers with low to moderate bandwidth requirements.

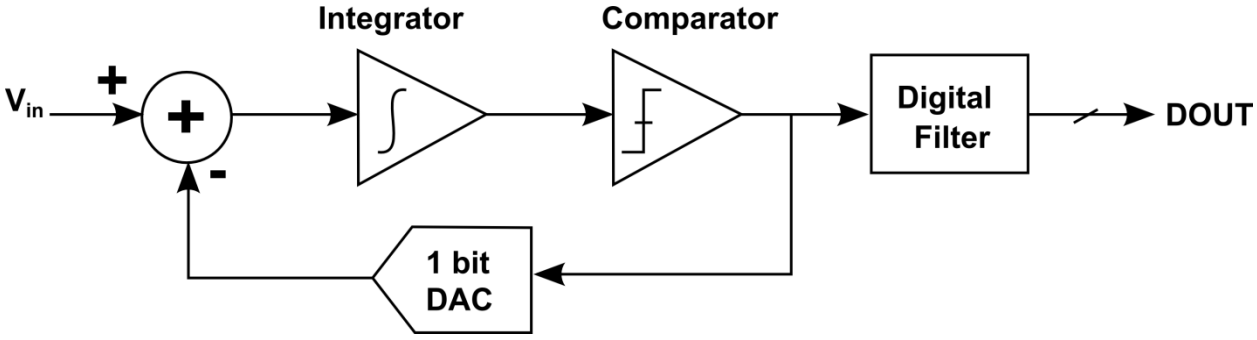


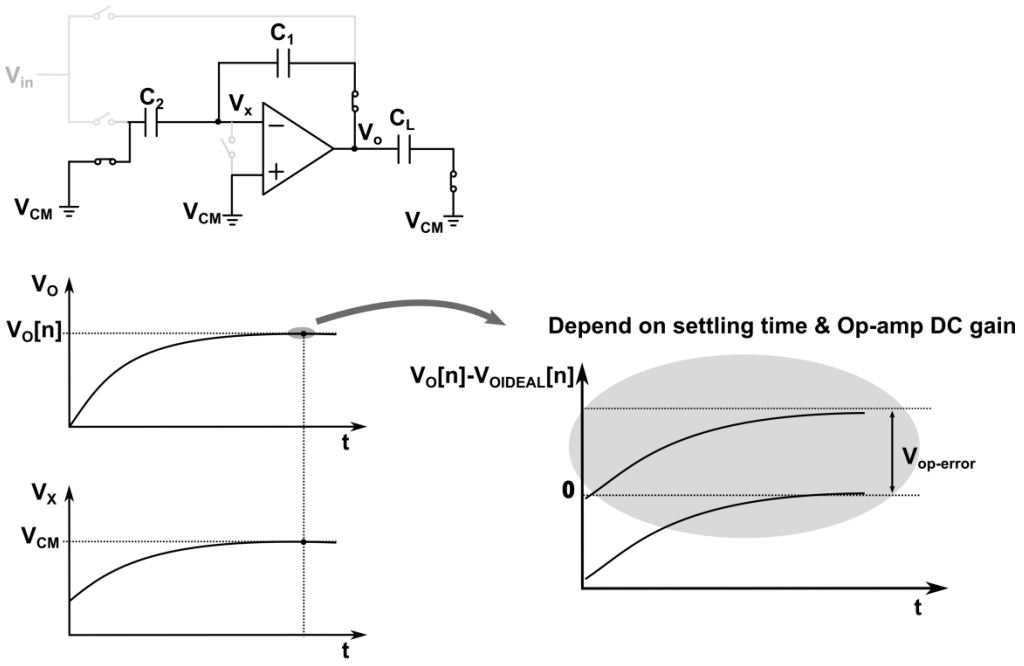
Figure 2-6: A typical noise shaping architecture.

3 Zero-Crossing Based Circuits (ZCBC) Pipelined ADCs

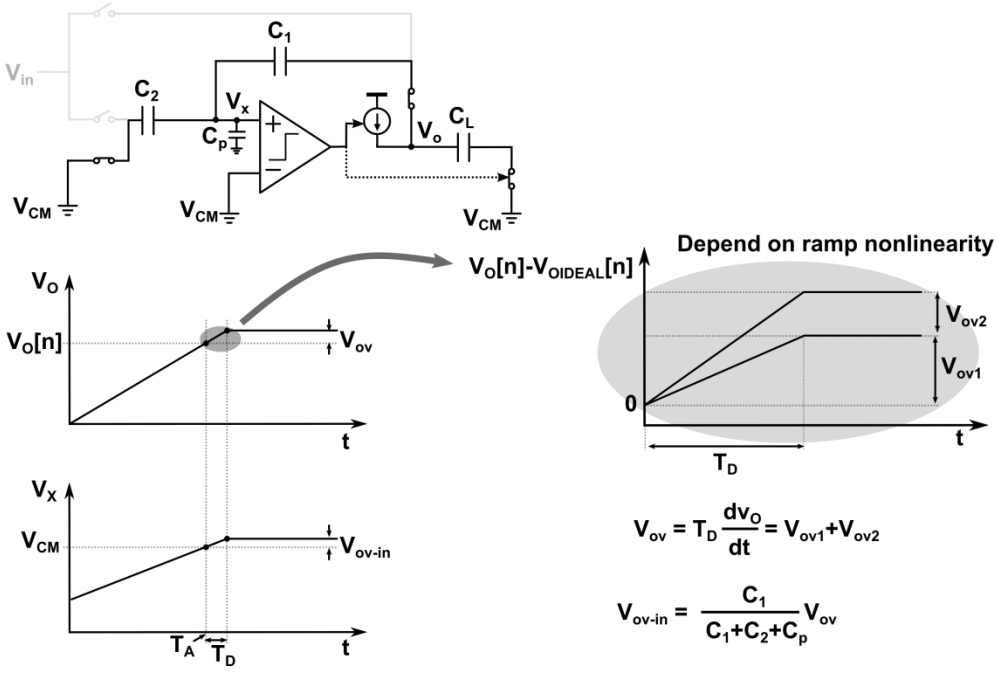
Zero-crossing-based circuits (ZCBC) were developed as an alternative way to build switched capacitor circuits without using op-amps. It has been shown that ZCBC are more power efficient and more suitable for submicron processes with low intrinsic device gain compared to traditional op-amp based switched capacitor circuits [25]. However, increasing both sampling speed and resolution has been challenging in both ZCBC and op-amp based circuits. This chapter will describe the published circuit techniques of ZCBC that improve sampling speed, resolution, and power consumption. Most of the published ZCBCs used pipelined architectures and their characteristics will be discussed in this chapter.

3.1 Fundamentals of ZCBC Architectures

Figure 3-1 illustrates the basic differences between an op-amp based switched capacitor circuit and a zero-crossing based switched capacitor circuit. Both circuits utilize a virtual ground to realize an accurate gain stage, however the methods employed to achieve a virtual ground condition and the resulting non-linearities are quite different between the two implementations. Typical time-domain voltage waveforms at the input and output of an op-amp-based and a ZCBC gain stages are shown in Figure 3-1 (a). The virtual ground of the op-amp based gain stage is forced by the closed loop. An error voltage $V_{op\text{-}error}$, results due to the finite op-amp DC gain and incomplete settling. Figure 3-1 (b) depicts the time-domain waveforms for the ZCBC, where the virtual ground of the gain stage is detected by the zero-crossing detector. The error voltage, V_{ov}, in this case is now a function of the ramp waveform and the detection operation, as will be discussed to follow.



(a)



(b)

Figure 3-1: Conceptual diagram. (a) Op-amp based circuits. (b) Zero-crossing based circuits.

In ZCBC, the output ramp is typically generated by charging the capacitors with a current source. The nonlinearity associated with the current source creates an output-dependent overshoot variation which is analogous to the variation of the virtual ground voltage of the op-amp based circuit with a finite op-amp gain. If the ZCD's delay is zero then the sample is taken precisely at the zero-crossing instant T_A, the sampled output voltage is accurate. In practice, the ZCD delay is finite, which results in an overshoot. The magnitude of the output voltage overshoot in ZCD circuits is a function of the output ramp slope $\frac{dv_O}{dt}$ and the ZCD delay T_D.

$$V_{ov} = T_D \frac{dv_O}{dt} = V_{ov1} + V_{ov2} \quad (1)$$

The ZCD overshoot, V_{ov}, has two components; a constant component, $V_{ov1,}$ and a signal dependent component, V_{ov2}. The constant component V_{ov1} is easily corrected, or tolerated, in most circuits. The variable component, V_{ov2}, typically results from the nonlinearity of the output ramp. The current source's finite output resistance as well as non-linear parasitic capacitance at the output determines the ramp non-linearity. If the T_D is signal dependent then this will also affect linearity, however, the T_D variation is small compared to the ramp non-linearity. This can be explained by noting that the ZCD sees nearly the same ramp input at the same input common mode regardless of the output residue. Thus, we can treat T_D as a scalar that only depends on the time-constant of the ZCD. The ZCD input referred overshoot is defined as follows:

$$V_{ov-in} = V_{ov} \frac{C_1}{C_1+C_2+C_p} \quad (2)$$

where C_1 is feedback capacitor, C_2 is sampling capacitor, and C_p is parasitic capacitance at V_x node.

3.2 Single-Ended ZCBC Topologies

The comparator of comparator-based-circuits (CBSC) [9] is replaced with a zero crossing detector (ZCD) because only the function of detecting zero crossing is necessary from the threshold detector in a CBSC circuit. Figure 3-2 shows a stage of a dynamic ZCBC in a pipelined ADC. A dynamic inverter was used as the ZCD [10]. The dynamic ZCD dissipates power only during the transition moment when the input crosses the virtual ground and the output changes. The dynamic ZCD is therefore very power efficient. The input voltage is sampled on C_1 and C_2 during the sampling phase. Then the ZCD output V_p is precharged to V_{DD} by M_2 and the output voltage V_O is discharged to ground by M_4. After this preset phase the current source charges V_o with constant ramp rate. At the moment the ZCD input voltage crosses the threshold of the ZCD, its output voltage V_p drops quickly. The correct output is then transferred to the next stage's sampling capacitors. Similar to digital circuits, the ZCD consumes only CV^2f power.

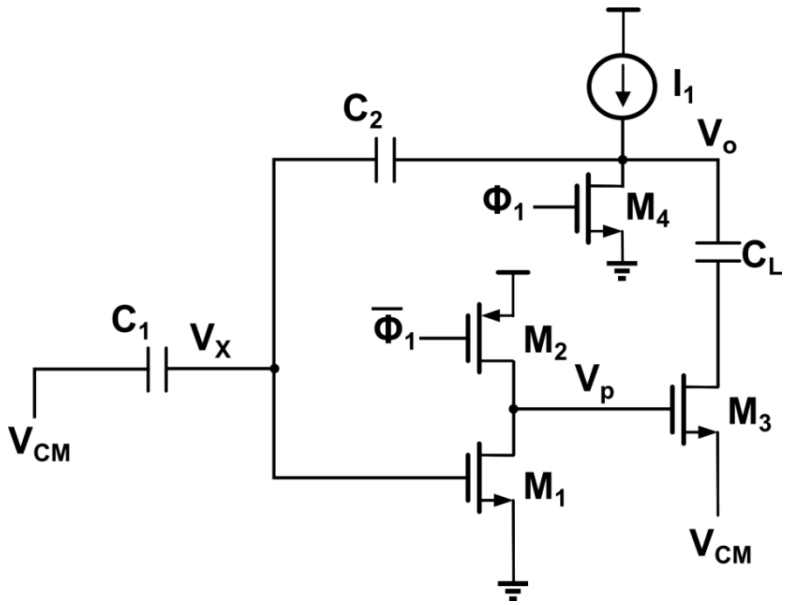


Figure 3-2: A stage of the dynamic ZCBC pipelined ADC.

3.3 Differential ZCBC Topologies

To improve power supply and common mode rejection of single ended ZCBCs, differential ZCBCs have been developed. Single and dual phase ramp techniques have been introduced with differential ZCDs for higher resolution and high speed [11]-[13], [17]-[22].

3.3.1 ZCBC with Dual Phase Ramp

To achieve higher resolution, a differential ZCBC is implemented with a differential preamplifier driving a dynamic threshold detector. Differential signal paths have better power supply and common mode rejection compared to single-ended architectures. Their main drawback is reduced power efficiency because of the constant bias current in the preamplifier. The first differential ZCBC was introduced [11] with a bidirectional dual ramp. As shown in Figure 3-3, it has overshoot correction (OCC) circuits to cancel out some of the overshoot after the coarse phase. To maintain matched rising and falling ramps, capacitive common mode feedback (CMFB) is used in the falling current source. Another dual phase approach is the unidirectional ramp scheme shown in Figure 3-4. One advantage of the unidirectional scheme is that the ZCD can be optimized in one direction, which makes the ZCD simpler and faster. Another advantage is that the operation is faster because of the shorter coarse phase. Moreover, it is more energy efficient compared to the bidirectional approach because the unidirectional charge transfer does not charge and discharge the capacitors unnecessarily. It only charges or discharges until the ZCD detects zero crossing [17].

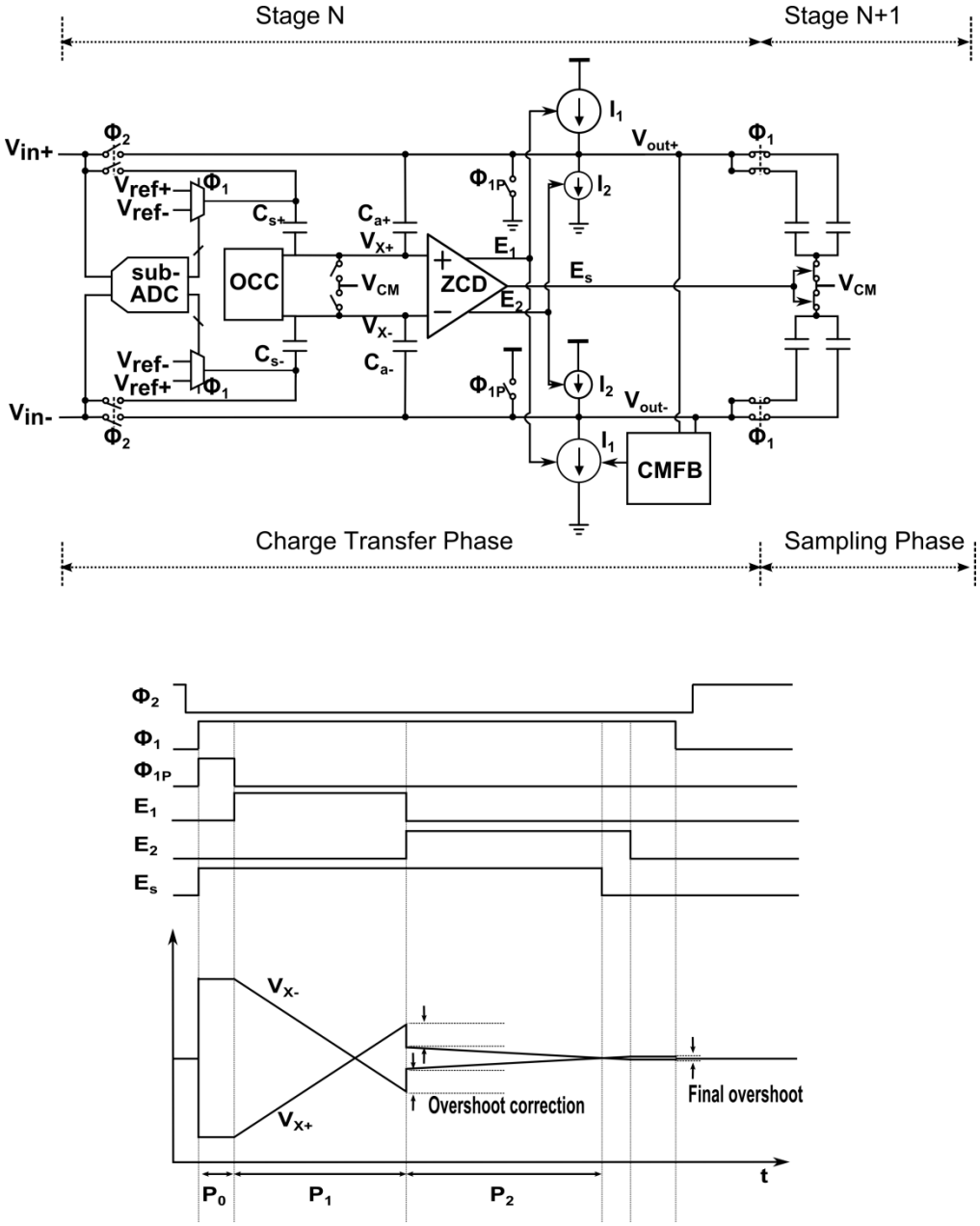


Figure 3-3: The first fully differential ZCBC pipeline ADC with bidirectional ramp.

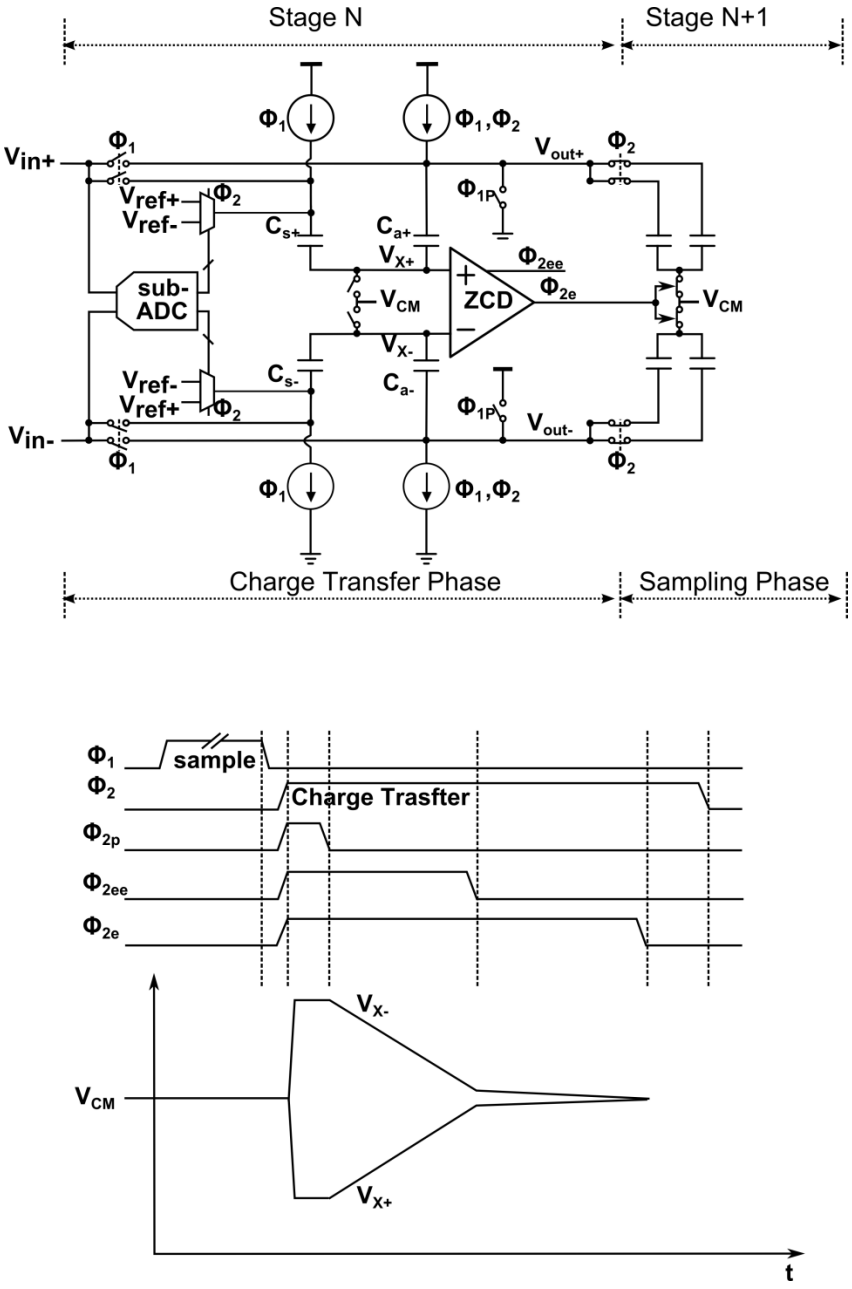


Figure 3-4: Schematic of two phase fully differential ZCBC pipelined ADC with unidirectional ramp.

3.3.2 ZCBC with Single Phase Ramp

A single phase ramp does not require complex switching methods. This architecture is used in ZCBCs for higher speed operation [12],[13] and is shown in Figure 3-5.

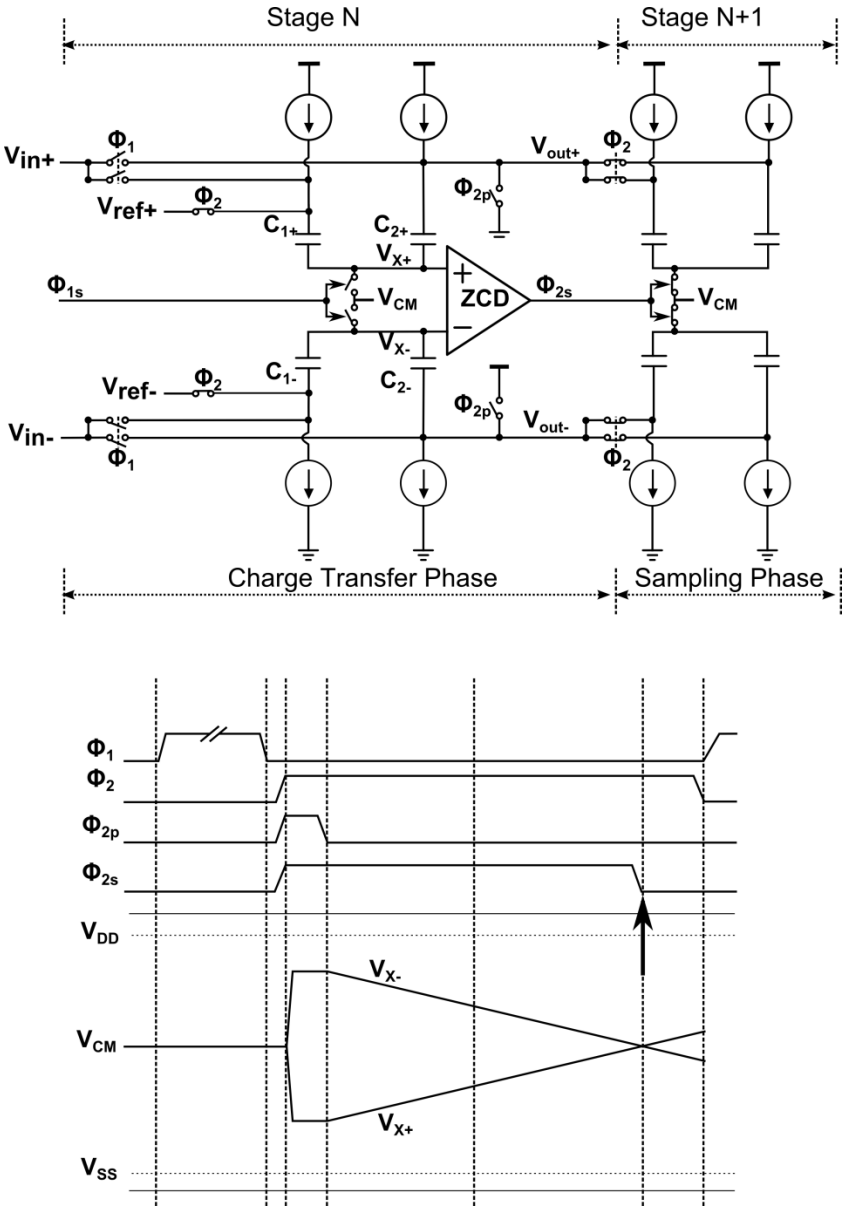


Figure 3-5: Schematic of single phase fully differential ZCBC pipelined ADC.

For fast operation, the programmable current mirror load used for offset and overshoot cancellation of the ZCD [12] is removed to reduce parasitic capacitance loading. Instead, offset and overshoot cancellation is accomplished by a tiny capacitor array tied to the input of the ZCD, which has negligible effect on speed [13]. The tail current source is cascoded to improve the amplifier's common mode and power supply rejection. Preamplifier duty-cycling has also been disabled for faster operation with a modest increase in power consumption tradeoff. A Decision Boundary Gap Estimation (DBGE) technique is used in [12] to calibrate errors due to capacitor mismatch, finite gain, and ramp nonlinearity in the ZCB circuits, which causes INL jumps at the bit decision boundaries.

3.4 ZCBC with Op-amp

Correlated level shifting (CLS) [15] has been introduced to reduce finite op-amp gain error and increase the op-amp's useful output swing. By splitting the op-amp in CLS into two separate amplifiers and then designing each amplifier with its specification requirements, the overall performance of CLS improved in terms of power, speed, and accuracy [16]. CLS uses a ZCBC for coarse phase and an op-amp for fine phase with linear settling. The schematic of a split-CLS pipeline stage with corresponding timing and waveform diagrams is shown in Figure 3-6. In addition to the op-amp and ZCBC circuitry, the structure contains a set of capacitive DACs which are used to cancel ZCBC overshoot prior to the start of op-amp settling.

During ϕ_S the input capacitors sample the input while the ZCD and current sources are shut off and the op-amp is idle. At the beginning of ϕ_A the amplification operation begins with a short pre-charge phase ϕ_{PC}, the op-amp output and bottom plate of C_{CLS} are connected to V_{CM}. When the pre-charge switches open at the end of ϕ_{PC} the current sources charge the output load

with a linear ramp until zero crossing is detected by the ZCD and the current source is turned off. C_{DAC} is then connected to cancel overshoot. After this the op-amp settles to the final output voltage until the end of ϕ_A. The ZCBC is only used for the coarse phase so its accuracy requirement is not high. Dynamic biasing is adopted to save power while sacrificing accuracy. Because the op-amp's output swing is very small due to the CLS technique, a telescopic double cascoded op-amp can be used to achieve high gain for better accuracy.

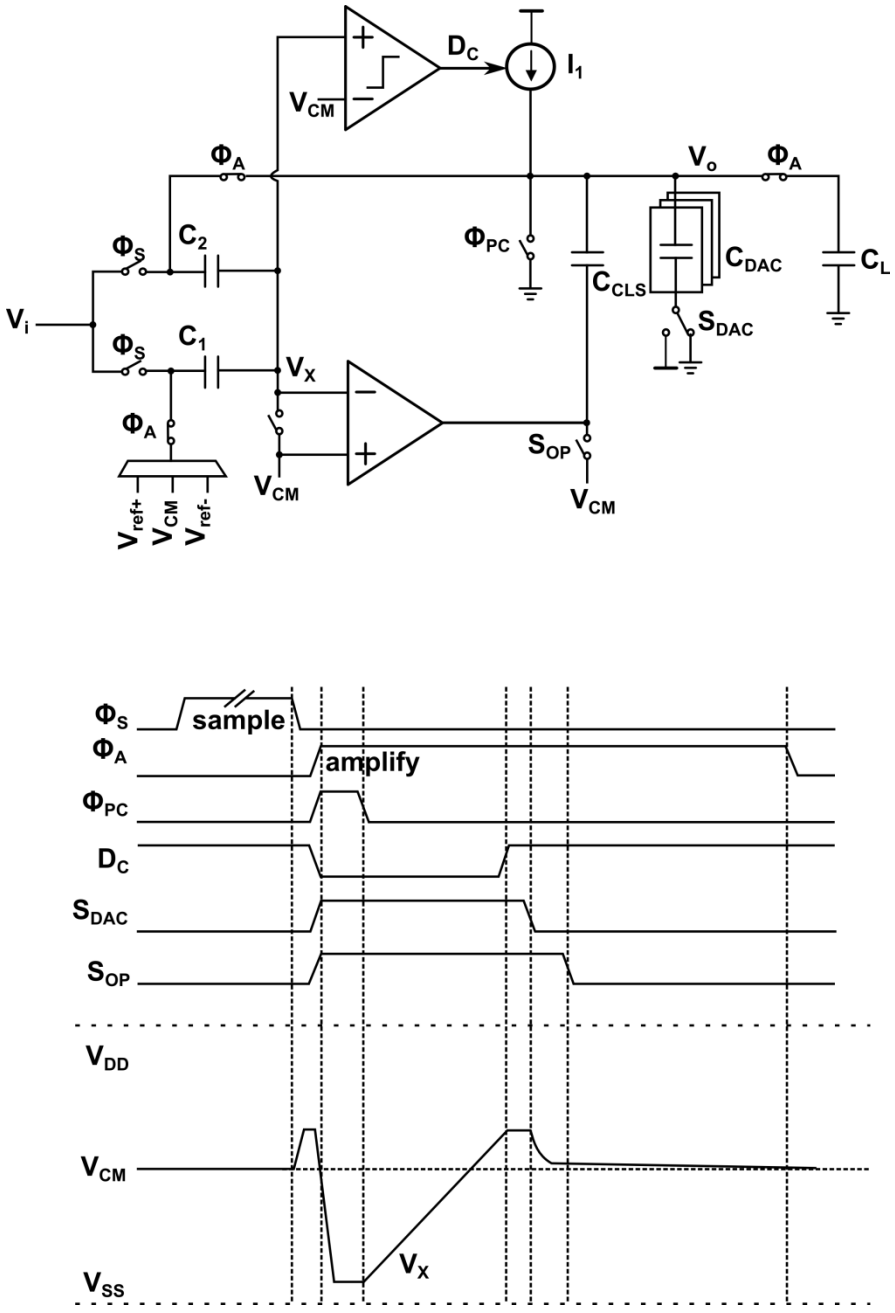


Figure 3-6: Schematic of a split-CLS pipelined ADC with ZCBC.

3.5 Characteristics and Non-Idealities of ZCBC Pipelined ADCs

This section describes issues related to ZCBC and op-amp based pipelined ADCs. A ZCBC pipelined ADC has very similar characteristics compared to an op-amp based pipelined ADC in terms of gain error, comparator offset, and DAC mismatch. The main differences are the current source, ZCD, and preset switches in the ZCBC design. The similarities and differences between the designs are illustrated with several techniques used to improve nonlinearities.

3.5.1 Pipelined ADC architecture

The functional building block of a pipelined ADC with a ZCBC is the same as an op-amp based pipelined ADC. The only difference is in the MDAC stage's implementation. The basic characteristic of op-amp based circuits is that they settle linearly with time constant. Various non-idealities therefore degrade performance of the ADC. In a typical 3.3 bit stage with an analog input range of ± V_{ref}, the residue transfer function can be written as

$$V_{out} = 4\left[V_{in} + \sum_{n=1}^{8} D_n \frac{V_{ref}}{4}\right],\ D_n = -1,1 \tag{3.1}$$

Figure 4-2 shows an ideal residue plot for 3.3 bit stages with gain of 4. With the digital redundancy, the correction range is depicted as a gray area. The comparator offset can be tolerated up to ± V_{ref}/8.

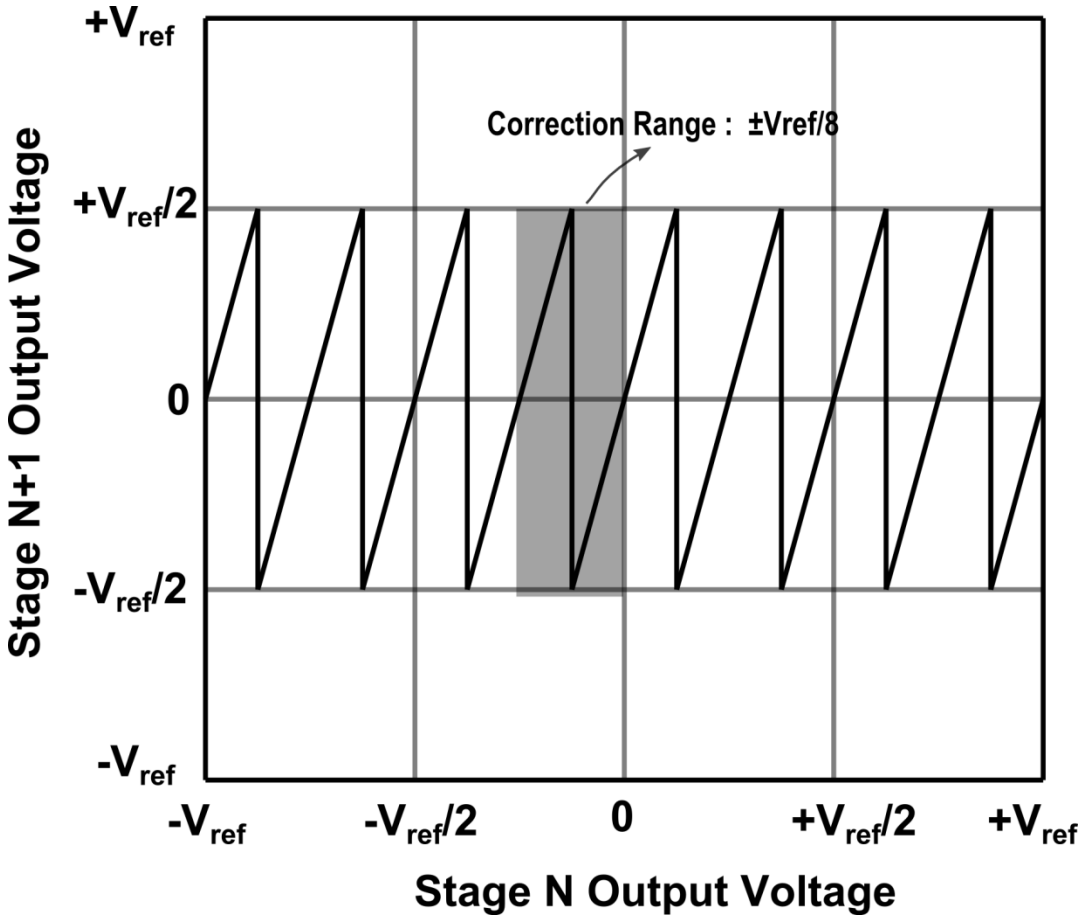


Figure 3-7: Ideal input/output transfer curve.

3.5.2 Gain error

Gain error is caused by mismatch between the sampling capacitor and feedback capacitor or not enough open-loop gain of the op-amp. The final output voltage in an MDAC stage with an op-amp is

$$V_{out} = \left(\frac{C_S+C_F}{C_F}\right)\left(\frac{1}{1+\frac{1}{A\beta}}\right)(V_{in} - V_{DAC}) \quad (3.2)$$

where $\beta = C_F/(C_F + C_P + C_S)$ is the feedback factor, C_F is the feedback capacitor, C_S is the sampling capacitor, C_P is the parasitic capacitance at the op-amp input, and A is the DC gain of

the open loop. The op-amp must provide output accuracy less than 0.5LSB, which means that the open loop gain of the op-amp should be larger than that given in equation 3.2. For a given total resolution of N bits and first stage resolution of M bits, if C_F is a shared sampling capacitor then

$$A_{op-amp\ DC\ gain} > (2^{N-M})\left(\frac{2^M C_{F+C_P}}{C_F}\right) \approx 2^N \tag{3.3}$$

ZCBC designs have a similar constraint. The overshoot variation can be understood as an effect of DC gain which in turn can be understood as how small errors occur in a virtual ground node. The total nonlinearity is a function of the voltage variation at the input of the ZCD.

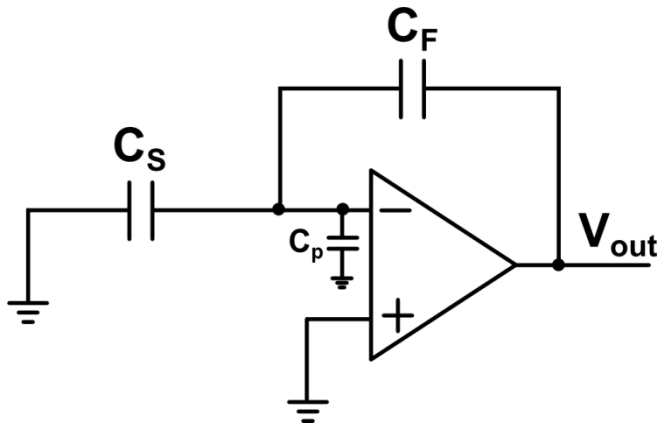


Figure 3-8: A switched capacitor configuration in amplification phase.

The overshoot variation is very similar to gain error because it is data dependent. It has two factors, constant offset and data dependent error. A constant overshoot produces an offset in the pipelined ADC, but data dependent error introduces nonlinearity into the ADC and degrades its performance.

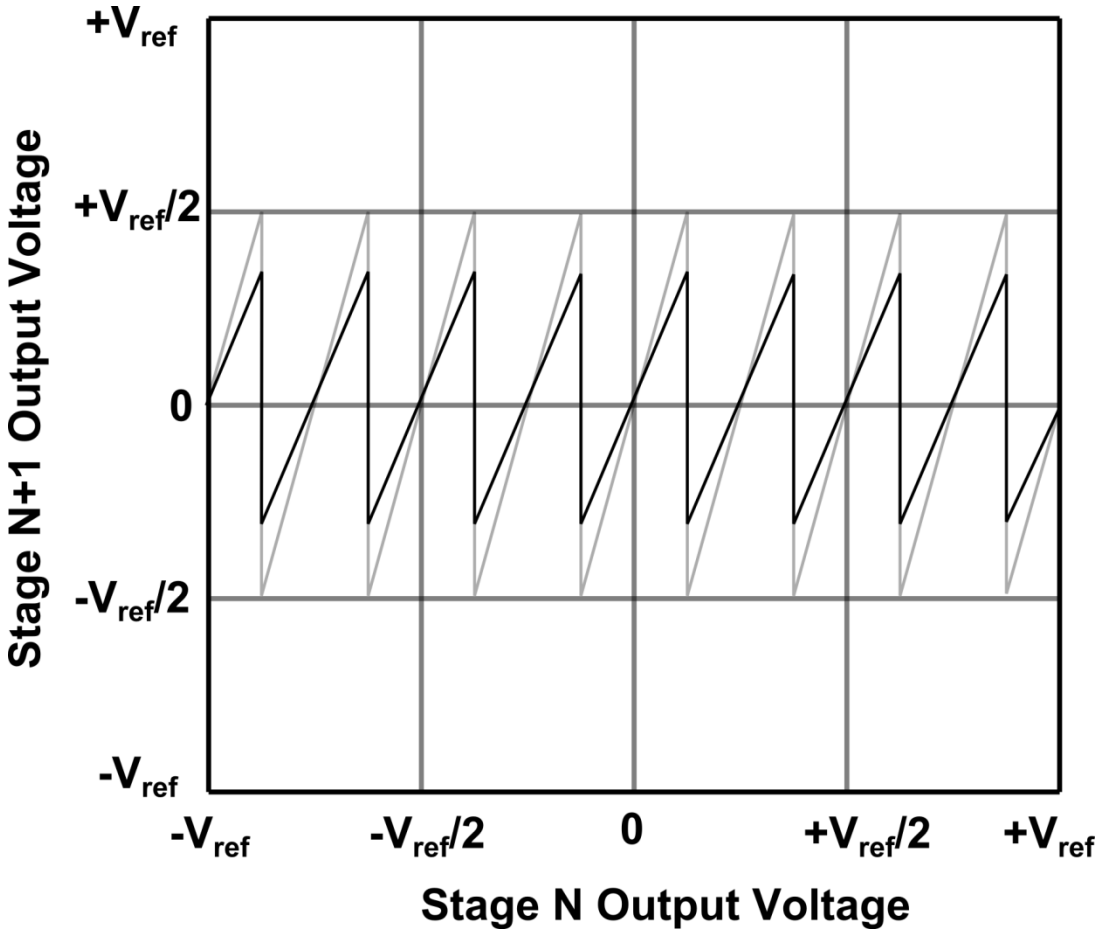


Figure 3-9: Input/output transfer curve with gain error.

3.5.3 Incomplete Fine Phase in ZCBC

An incomplete fine phase in a ZCBC is similar to incomplete settling of a residue amplifier. To get a certain accuracy the settling time constant must be met with op-amp circuits. In ZCBCs, however, ramping has to be finished and ZCD has to detect zero crossing within half a clock period. Otherwise, ZCBC has errors from the charge transfer phase. An incomplete fine phase ramp causes a data dependent error because the runway lengths depend on input voltage.

3.5.4 Capacitor DAC nonlinearity

DACs can be made with resistor ladders or capacitor arrays, but mismatch among them can generate data dependent reference levels. This causes DNL error in the ADC. The DNL due to capacitor mismatch can be written as follows [35]:

$$DNL = \frac{\Delta C_i 2^N}{C_{total}} \tag{3.4}$$

where ΔC_i is the error of each individual capacitor in the first stage, C_{total} is the total capacitance of the first stage, and N is the resolution of the entire ADC. The total capacitance can be increased to reduce DNL, but the settling time constant of an op-amp based circuit is proportional to the load capacitance. Thus, the power must also be increased proportionally to maintain unity gain frequency.

A higher resolution for the first stage can reduce the DNL contribution due to capacitor mismatch. Mismatch among the capacitors in the array can result in non-uniform reference levels. Figure 3-10 shows the effect of non-uniform reference levels on the residue curve. This leads to significant DNL of the overall ADC. The DNL resulting from capacitor mismatch in the first stage, normalized to LSB can be written as follows:

$$DNL = \frac{k 2^{N-\frac{M}{2}}}{\sqrt{C_{total}}} \tag{3.5}$$

where N is the resolution of the overall ADC, M is the resolution of the first stage, C_{total} is the total capacitance of the first stage, and k is a constant related to the random variation of the capacitors. DNL improves by $\sqrt{2}$ for every additional bit resolved in the first stage or doubling of the total capacitance in the first stage. On the other hand, the ADC nonlinearity due to the

finite gain, A, of the first stage op-amp, does not change with stage resolution. The DNL of a pipelined ADC is proportional to the op-amp gain error $1/A\beta$ and number of quantization steps of the remaining stages 2^{N-M} [39] as follows:

$$|DNL|_{max} \propto \frac{2^{N-M}}{A\beta} \tag{3.6}$$

For every 1-bit increase in the resolution M of the first stage, the feedback factor β decrease by approximately 2.

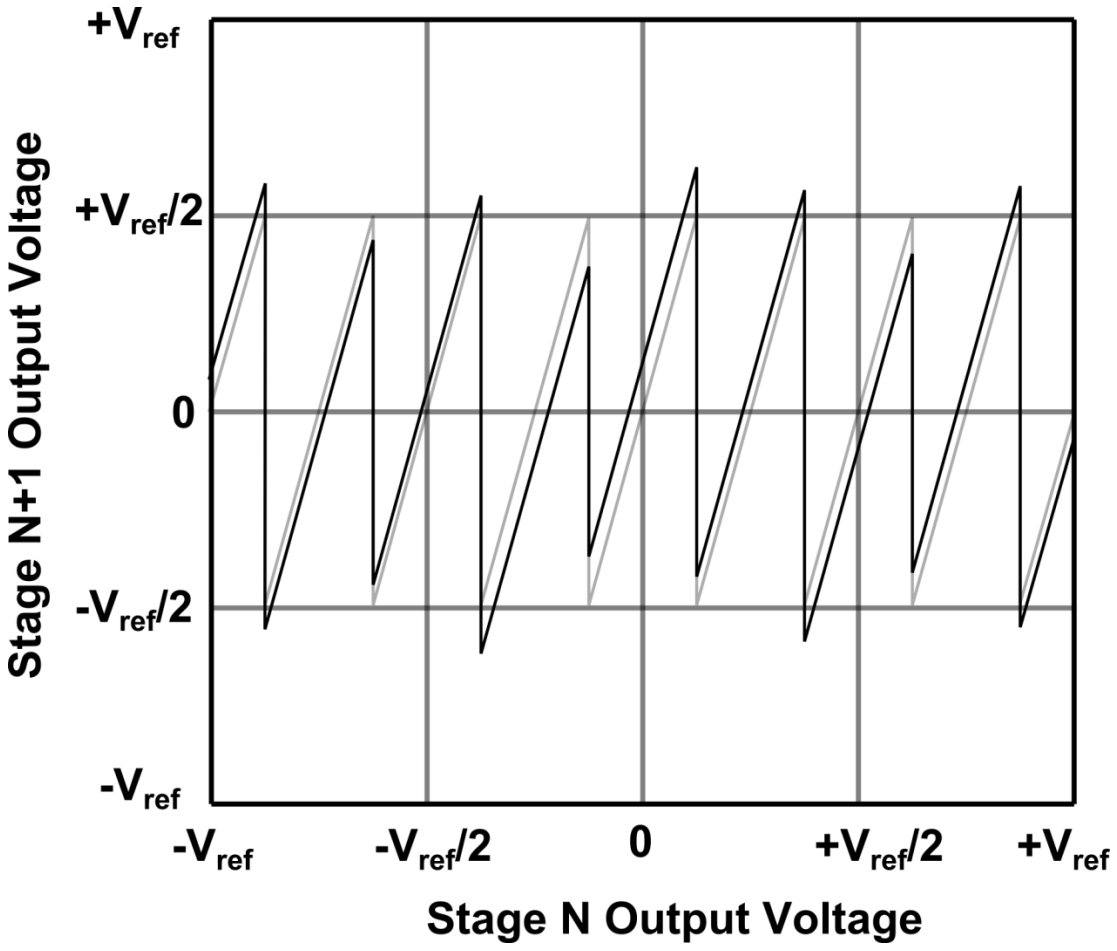


Figure 3-10: Input/output transfer curve with DAC nonlinearity.

3.5.5 Switch nonlinearity

The on-resistance of the MOS switches affects the settling time of the circuit. High on-resistance in MOS switches can not only slow down the circuit but also make the feedback system poorly damped or unstable if they are in the feedback loop. Using a switch which is too large adds a significant amount of drain/source junction parasitic capacitance at the output reducing the overall bandwidth. Nonlinearity due to MOS switch resistance and junction capacitance causes harmonic distortion. Especially for ZCBCs, this nonlinear resistance degrades the ramp linearity.

This nonlinearity problem can be improved by bootstrapping the input signal to the gate of the MOS switch. Current source splitting technique between the switches can also reduce this nonlinearity [10].

3.5.6 Sub-ADC comparator offset

The accuracy of the comparator within each sub-ADC has to be good enough to produce accurate residual voltages for the following stages. The residue voltage typically goes out of the normal range due to comparator offsets. Figure 3-11 shows the 3.3bit MDAC residue curves with random offsets in the sub-ADC's comparator. Positive comparator offset exceeds the output residue and negative offset goes below the normal range. Exceeding the correction range leads to loss of information about the signal. That is why a redundant bit, in other words overlap, is included. The function of a comparator is to compare the applied input signal voltage to a reference voltage, and the simplest way to implement a comparator is to use regenerative cross-coupled inverters. The signal is then amplified to the digital logic level for subsequence processing.

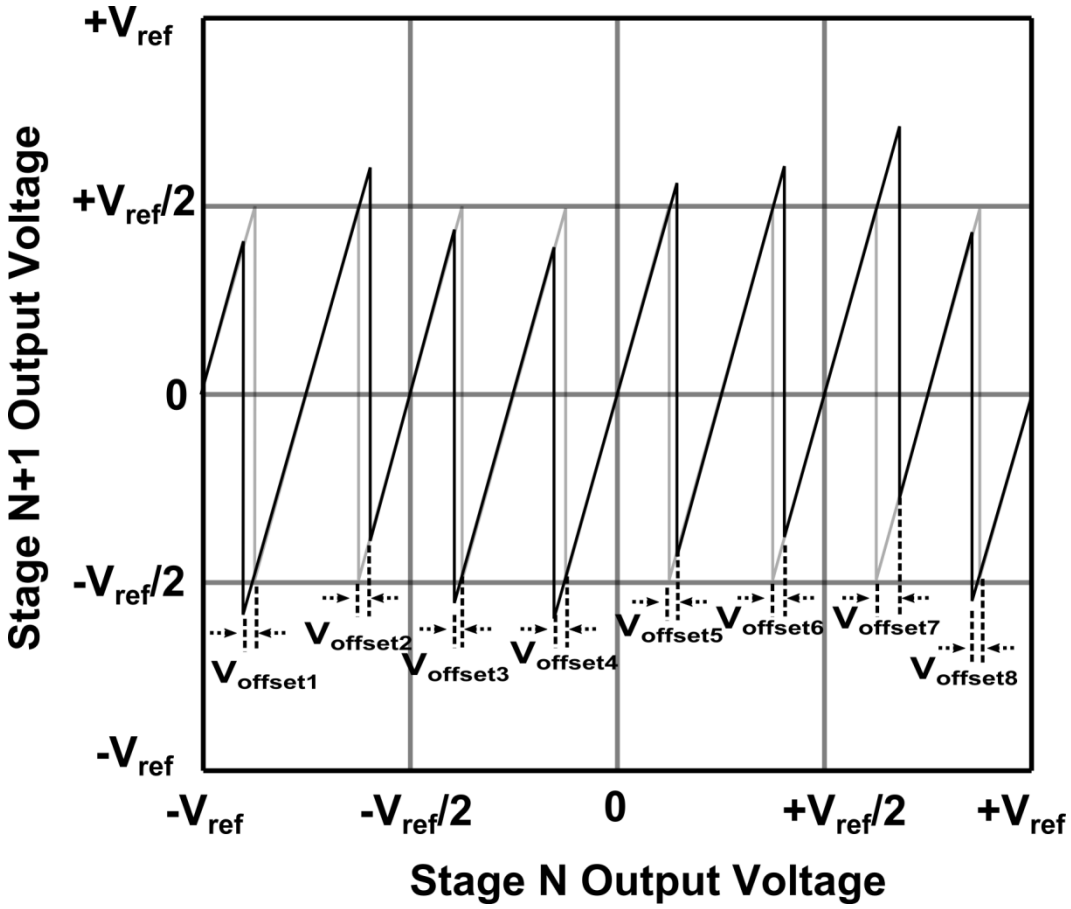


Figure 3-11: Input/output transfer curve with sub-ADC's comparator offset.

3.5.7 Op-amp offset

Figure 3-12 shows the effect of op-amp offset in an MDAC residue curve. It shifts up or down depending on the polarity of the op-amp offset. Combined comparator and op-amp offsets must be covered by over-range protection within the pipeline stages. This op-amp's offset corresponds to the constant portion of the overshoot voltage in a ZCBC.

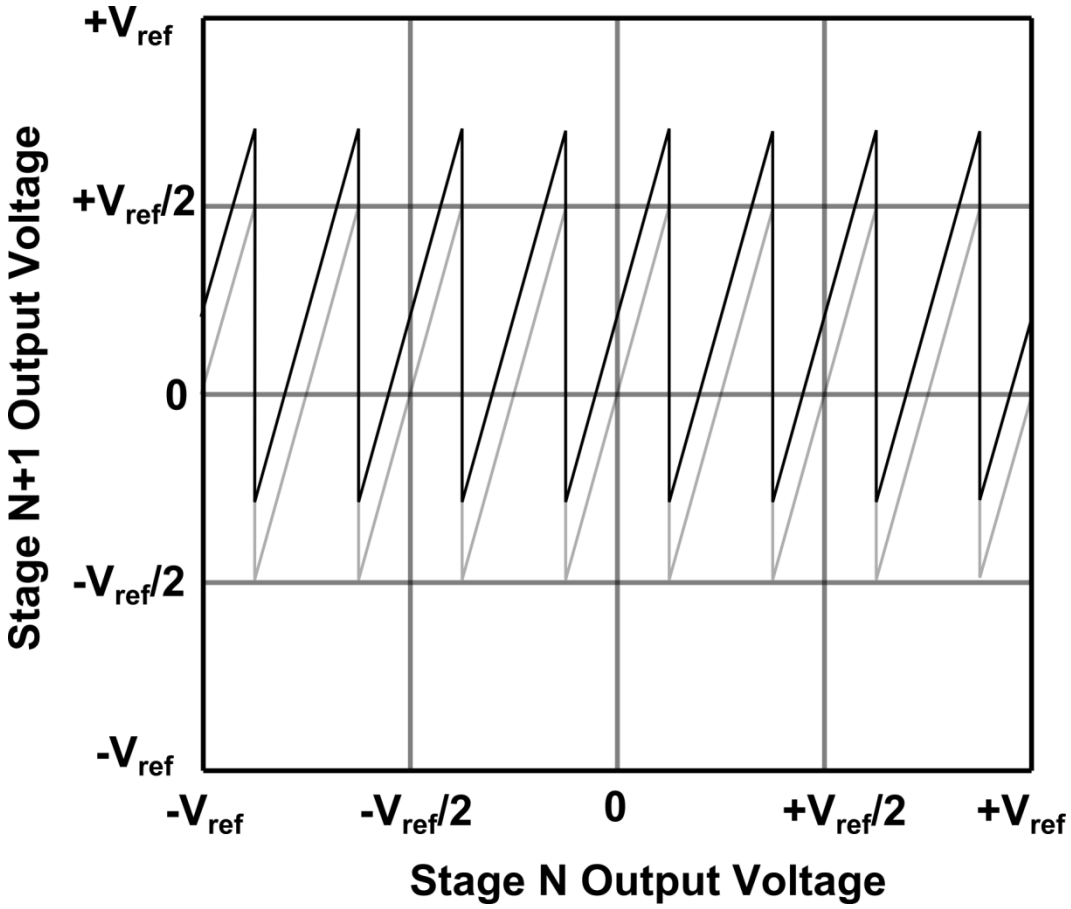


Figure 3-12: Input/output transfer curve with op-amp offset.

3.6 Overshoot Voltage of ZCBC

Because of the finite delay of the ZCD and ramp rate the final value overshoots the ideal output value. The overshot voltage is shown as V_{ov} for fast and slow ramp in Figure 3-13. The overshoot voltage is constant if the ramp slope and ZCD delay are constant. However, due to finite output resistance and non-linear parasitic junction capacitance the ramp slope is non-constant. ZCD delay can also vary due to noise and common mode voltage variation, which will generate non-linearity in the ADC.

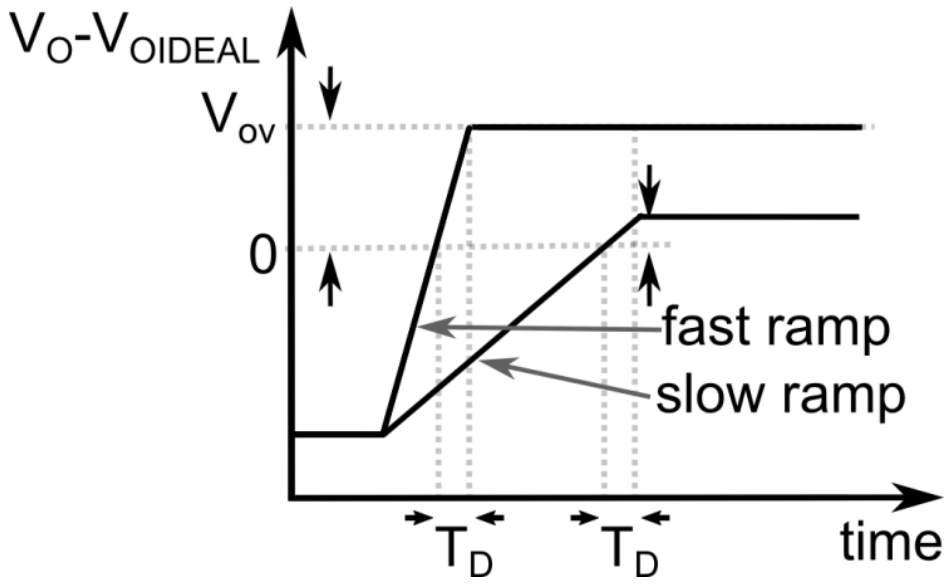


Figure 3-13: Overshoots of fast and slow ramp rates.

In a ZCBC, the output ramp is typically generated by charging a capacitor with a constant current source. The nonlinearity associate with the current source creates a signal-dependent overshoot variation. This is a similar effect to that associated with the finite gain in an op-amp that creates a signal-dependent virtual ground condition. The output capacitive loading varies with the output voltage due to the transistor's PN junctions between drain and body nodes. Thus, the linear sampling capacitor should be much bigger than these nonlinear parasitic capacitances.

3.7 Ramp Nonlinearity of ZCBC

In ZCBCs the output ramp is generated by a constant current source. The ramp rate is

$$\frac{dV_o}{dt} = \frac{I_0}{C_t} \tag{3.7}$$

where I_0 is the current from the current source and C_t is the total capacitance at the output node. Ramp nonlinearity causes overshoot variation. This nonlinearity comes from current changes with output voltage due to the finite output impedance. Another ramp nonlinearity source is parasitic junction capacitance that varies depending on voltage.

3.8 Noise in ZCBC

The thermal noise of a ZCD contributes to timing jitter and changes the sampling time. The error in sampling time creates a voltage error. For ZCDs with high bandwidth, the traditional steady state noise analysis can be applied because the ZCD has settled during the zero-crossing instant.

Assuming a first-order, low-pass response with a 3-dB bandwidth of ω_0, the transfer function of $H(s)$ is given by

$$H(s) = \frac{1}{1+s/\omega_0} \tag{3.8}$$

This results in the magnitude of the response $H(s)$ being equal to

$$|H(j\omega)| = \sqrt{\frac{1}{1+\left(\frac{\omega}{\omega_0}\right)^2}} \tag{3.9}$$

An input signal, $V_{ni}(\omega)$, is a white noise source given by

$$V_{ni}(\omega) = V_{nw} \tag{3.10}$$

where V_{nw} is a constant.

The total output noise rms value of $V_{no}(\omega)$ is equal to

$$V_{no(rms)}^2 = \int_0^\infty \frac{V_{nw}^2}{1+\left(\frac{\omega}{\omega_0}\right)^2} d\omega = \frac{V_{nw}^2 \pi \omega_0}{2} = V_{nw}^2 \left(\frac{\pi}{2}\right) \omega_0 \tag{3.11}$$

where $\left(\frac{\pi}{2}\right) \omega_0$ is the noise bandwidth.

The total output noise mean-squared value is calculated by multiplying the spectral density by the noise bandwidth.

3.9 Bandwidth requirements for ZCBC

In ZCBC, the bandwidth requirements are determined by two factors. First, available time for ZCBC operation is determined by sampling speed. The ZCD delay can be approximated by its open loop time constant τ [41]. Second, overshoot variation that is product of ramp rate and ZCD delay must be less than accuracy requirement for overshoot variation [42] as follows:

$$V_{error} = T_D \Delta \frac{dV}{dt} \tag{3.12}$$

$$\Delta \frac{dV}{dt} = \left.\frac{dV}{dt}\right|_{V_{out}=V_{max}} - \left.\frac{dV}{dt}\right|_{V_{out}=V_{min}} \tag{3.13}$$

where V_{max} is the maximum output voltage and V_{min} is the minimum output voltage.

The V_{error} must be at least less than half LSB given resolution.

4 ZCBC Techniques for High Speed and High Resolution

ZCBCs require a fast ramp to achieve high speed since ZCBCs have to finish ramping within half a clock cycle. However, a fast ramp rate degrades ramp linearity, which directly affects the accuracy of ZCBCs. In this chapter we will describe high speed issues associate with ZCBCs and discuss proposed techniques to achieve high speed and high resolution in ZCBCs.

4.1 Ramp Rate with Single Phase

For a given sampling clock frequency, the ZCBC ramp must be finished within a half clock cycle. Figure 4-1 shows the waveform of a single ramp ZCBC. The minimum single ramp rate is

$$\left.\frac{dv}{dt}\right|_{min} = \frac{\frac{v_{p-p}}{2}+v_{dsat}}{\frac{T}{2}-t_p} \tag{4.1}$$

where $V_{p\text{-}p}$ is the input peak to peak voltage, t_p is the preset phase duration, V_{dsat} is over drive voltage, and T is the period of the sampling frequency. Figure 4-2 shows the required minimum ramp rate as a function of sampling frequency.

The overshoot voltage is calculated as follows,

$$V_{ov} = t_{ZCD}\left.\frac{dv}{dt}\right|_{min} = t_{ZCD}\frac{\frac{v_{p-p}}{2}+v_{dsat}}{\frac{T}{2}-t_p} \tag{4.2}$$

where V_{ov} is the overshoot voltage of ZCBC, t_{ZCD} is the ZCD delay, and dv/dt is the ramp rate. The overshoot variation is

$$\Delta V_{ov} = V_{ov}|_{max} - V_{ov}|_{min} \tag{4.3}$$

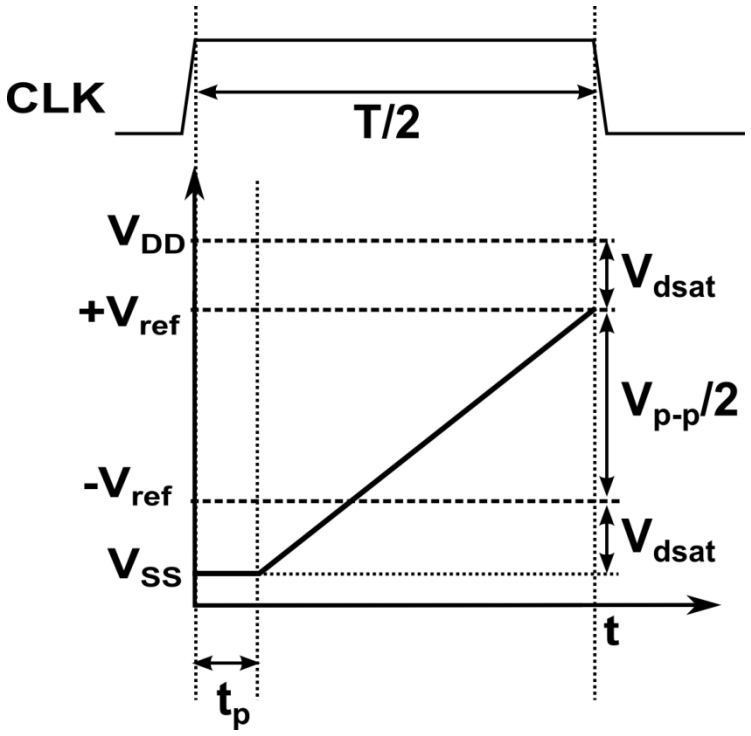


Figure 4-1: Single ramp ZCBC.

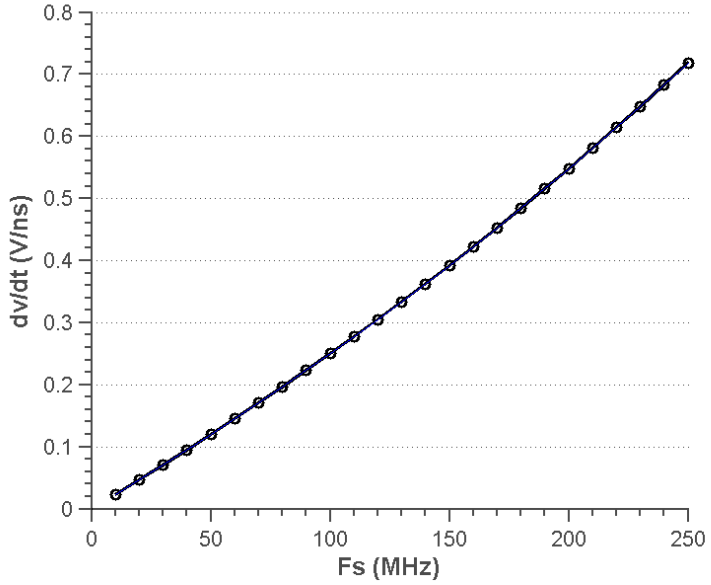


Figure 4-2: Required ramp rate versus sampling frequency.

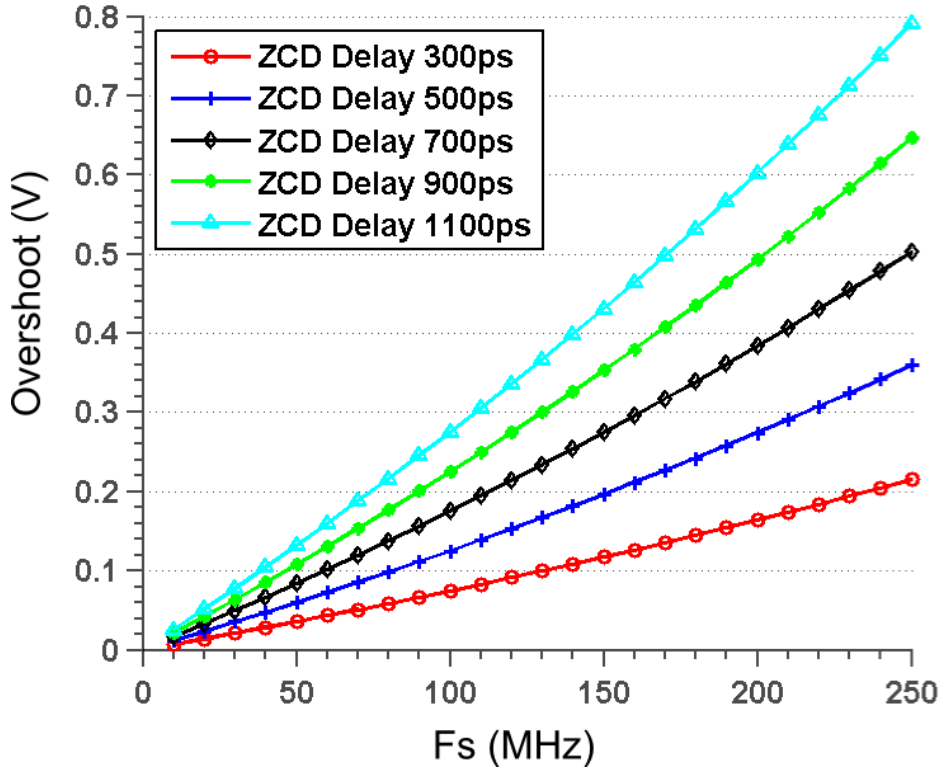


Figure 4-3: Overshoot versus sampling frequency with single ramp ZCBC.

Figure 4-3 shows examples of overshoot versus sampling frequency for various comparator delays using a single phase ramp. As the sampling frequency increases, the overshoot becomes larger. Reducing the ZCD delay costs power and also increases the noise bandwidth.

For *N*-bit accuracy with 1V reference voltage

$$\Delta V_{ov} < \frac{1}{2^N} \tag{4.4}$$

$$t_{ZCD}\Delta\frac{dv}{dt} < \frac{1}{2^N} \tag{4.5}$$

$$\Delta\frac{dv}{dt} = \frac{I_o}{V_A C_t} \tag{4.6}$$

where N is resolution, V_A is effective Early voltage, I_o is charging current, and C_t is total load capacitance of the current source. Slope variation can be described by Equation 4-9 where $\Delta\frac{dv}{dt}$ is the ramp nonlinearity across the output signal swing range.

$$\frac{dV_o}{dt} = \frac{I(V_o)}{C_t} \tag{4.7}$$

$$I(V_o) = I_o\left(1 - \frac{V_o}{V_A}\right) \tag{4.8}$$

$$\Delta\frac{dv}{dt} = \left.\frac{dv}{dt}\right|_{V_o=V_{max}} - \left.\frac{dv}{dt}\right|_{V_o=V_{min}} \tag{4.9}$$

So the required output effective Early voltage of the current source for a given sampling frequency and resolution is given as follows [41]:

$$\Delta\frac{dv}{dt} < \frac{1}{2^N}\cdot\frac{1}{t_{ZCD}} \tag{4.10}$$

$$V_A > \frac{I_o}{C_t}\cdot 2^N \cdot t_{ZCD} \tag{4.11}$$

where $\frac{I_o}{C_t}$ Is the ramp rate

Figure 4-4 shows one example of V_A requirement versus sampling frequency for 12 bit accuracy. Fast ZCDs have relaxed effective Early voltage of current source requirements.

There are two methods with the same output resistance for current source to achieve high accuracy with the ZCBC technique. One is making a fast ZCD and the other is using a slow ramp. The goal for both of these cases is to reduce overshoot itself. The constant portion of overshoot

becomes an offset in the ADC but any data dependent variation produces a nonlinearity which degrades accuracy.

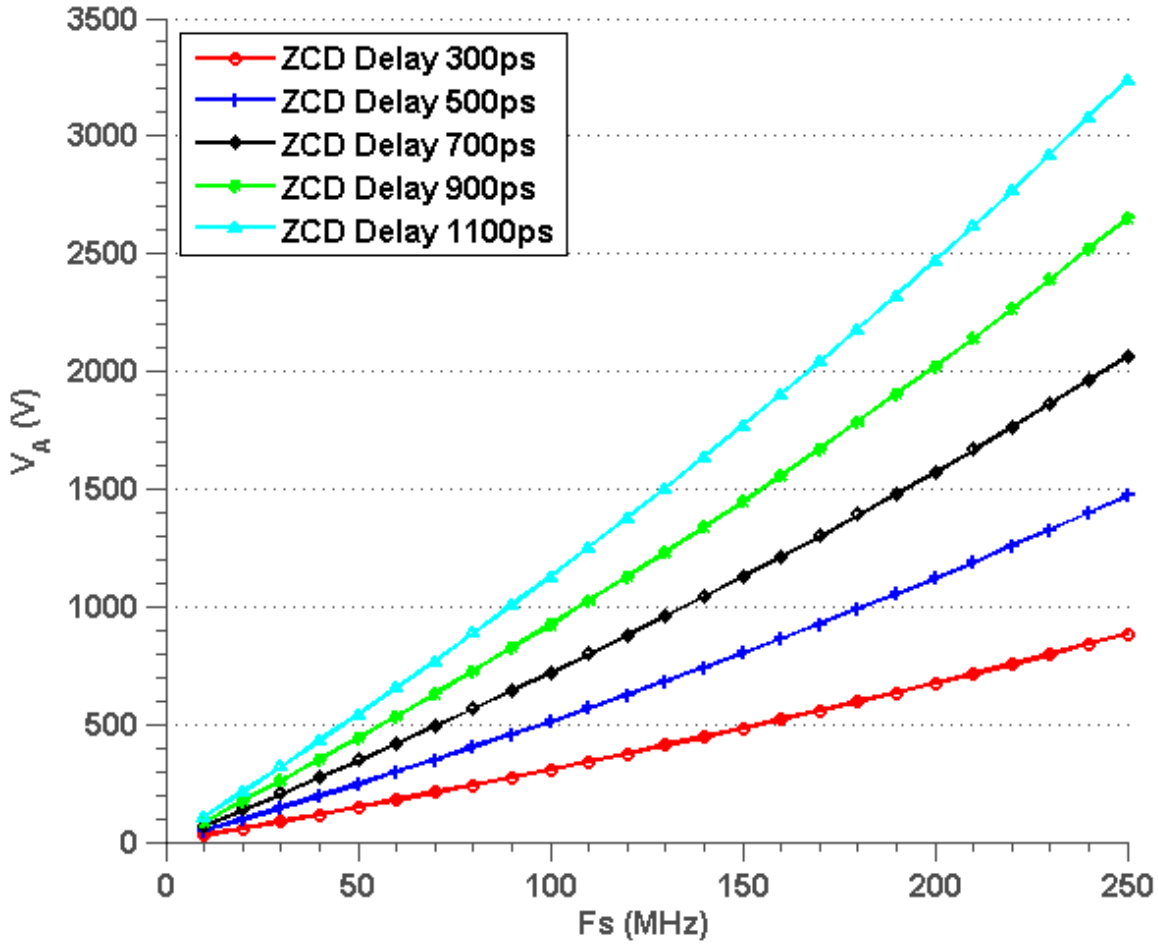


Figure 4-4: Required V_A for 12bit accuracy versus sampling frequency.

4.2 Ramp Rate with Two Phases

Ramp rate can be reduced with dual fine and coarse ramp rate architecture. For the coarse ramp, the minimum ramp rate is

$$\left.\frac{dv_c}{dt_c}\right|_{min} = \frac{\frac{v_{p-p}}{2}+v_{dsat}-V_{FINE}}{\frac{T}{2}-t_p-t_f} \tag{4.12}$$

where V_{FINE} is the difference between the fine phase and the coarse phase, t_p is preset time, and t_f is the fine phase duration time.

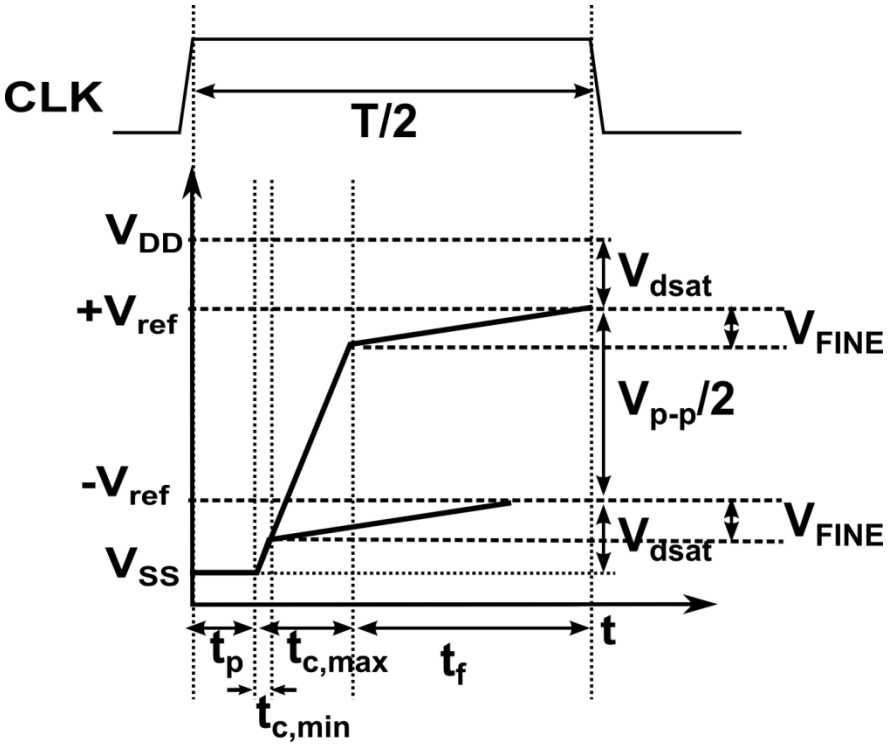


Figure 4-5: Dual ramp ZCBC.

The fine ramp rate can be written as follows

$$\frac{dv_f}{dt_f} = \frac{V_{FINE}}{t_f} = \frac{I_{fine}}{C_t} \tag{4.13}$$

Thus, more time for the fine phase is better for reducing the fine phase ramp rate. If we assume the fine phase duration covers half of the charge transfer phase and the coarse ramp covers one third then we get a much relaxed requirement on effective Early voltage of current source.

$$V_A > \frac{I_{fine}}{C_t} \cdot 2^N \cdot t_{ZCD,fine} \tag{4.14}$$

However, because of the limited speed of the coarse detector, the maximum coarse ramp rate is limited by

$$\left.\frac{dv_c}{dt_c}\right|_{max} \cdot t_{ZCD,coarse} \leq \frac{v_{p-p}}{2} + v_{dsat} - V_{FINE} \tag{4.15}$$

$$\left.\frac{dv_c}{dt_c}\right|_{max} \leq \frac{\frac{v_{p-p}}{2} + v_{dsat} - V_{FINE}}{t_{ZCD,coarse}} \tag{4.16}$$

4.3 Sub-ADC Decision

In the previous dual ramp ZCBC [11],[17] shown in Figure 4-6, while N^{th} stage is in the charge transfer phase the next stage's sub-ADC samples N^{th} stage's output right after fine phase and sub-ADC generates decision. N^{th} stage's decision must therefore be finished before N^{th} +1 stage enters the charge transfer phase. However, the sub-ADC's decision time gets to be a bigger portion of the half-clock duration as the sampling frequency increases, because the regeneration time for a given size and technology is fixed. Thus, this sub-ADC decision time reduces the available charge transfer time in high speed operation. To allow for an increased sample rate, this sub-ADC decision can be moved to the right after the coarse phase as shown in Figure 4-6, but the sub-ADC must be able to compensate for the voltage difference between the coarse and fine sampled voltage.

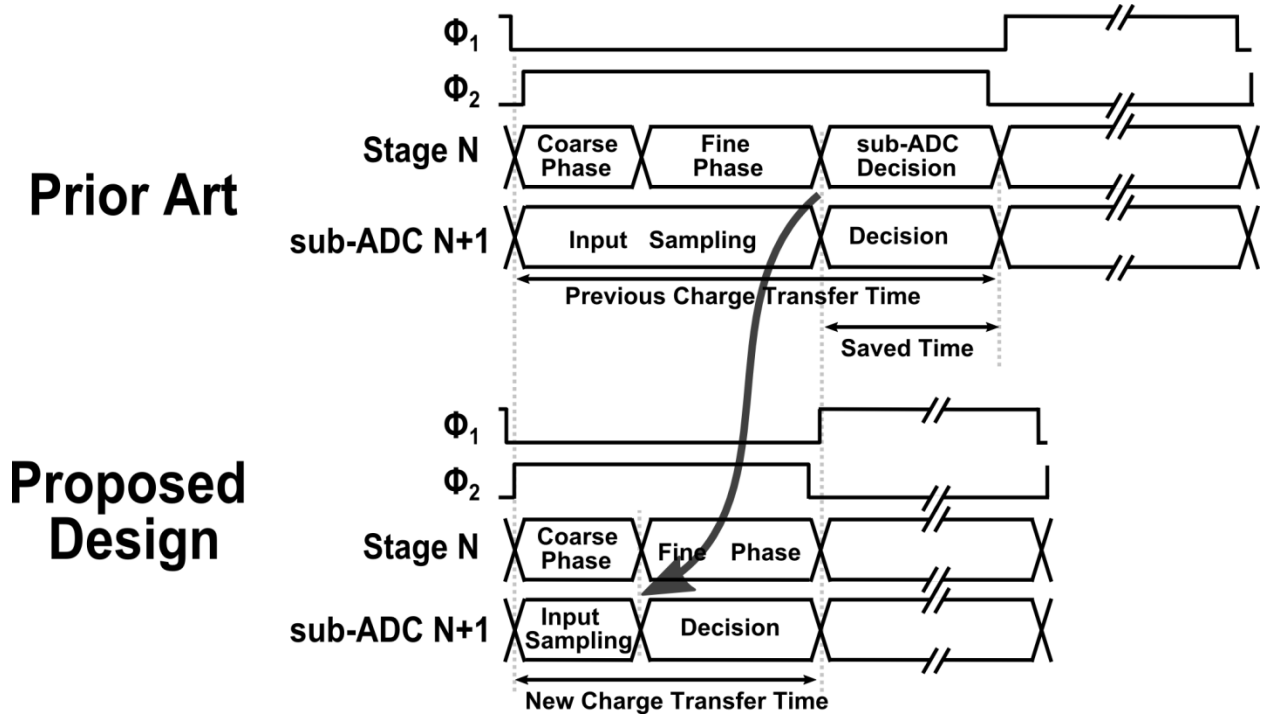


Figure 4-6: Timing diagram comparison with sub-ADC decision being made after either the fine phase or coarse phase.

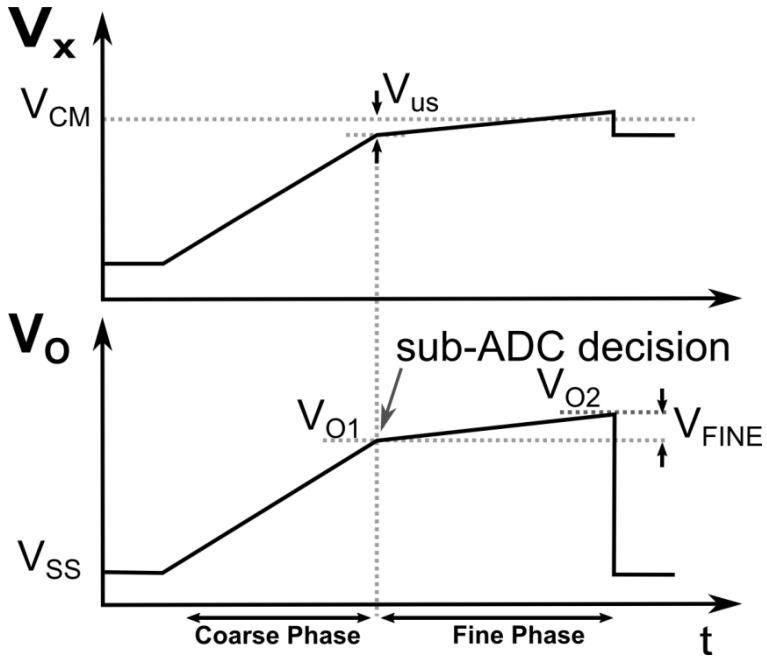


Figure 4-7: Waveforms of early sub-ADC decision.

Due to the high accuracy of the fine phase, this voltage difference is almost constant and thus appears as a fixed, systematic offset voltage which can be compensated. The voltage difference, V_{FINE}, between the coarse and fine phase is almost constant regardless of the output voltage residue.

Figure 4-7 illustrates waveforms for the residue output voltage and the ZCD input voltage for a single sample. V_{o1} is the output voltage at the end of the coarse ramp phase, and this is the voltage that is sampled for the early sub-ADC decision. V_{o2} is the output voltage at the end of the fine phase after the zero crossing decision that is sampled by the following pipeline stage. Since there is a voltage difference between V_{o1} and V_{o2}, the sub-ADC must be able to compensate in some way for the voltage difference between the coarse and fine phase output voltages. However, we have already noted in the previous section that in the dual ramp approach there is a nearly constant voltage difference between the coarse and fine phase output voltage. Thus, the voltage difference appears as a fixed systematic offset voltage on all sub-ADC comparators.

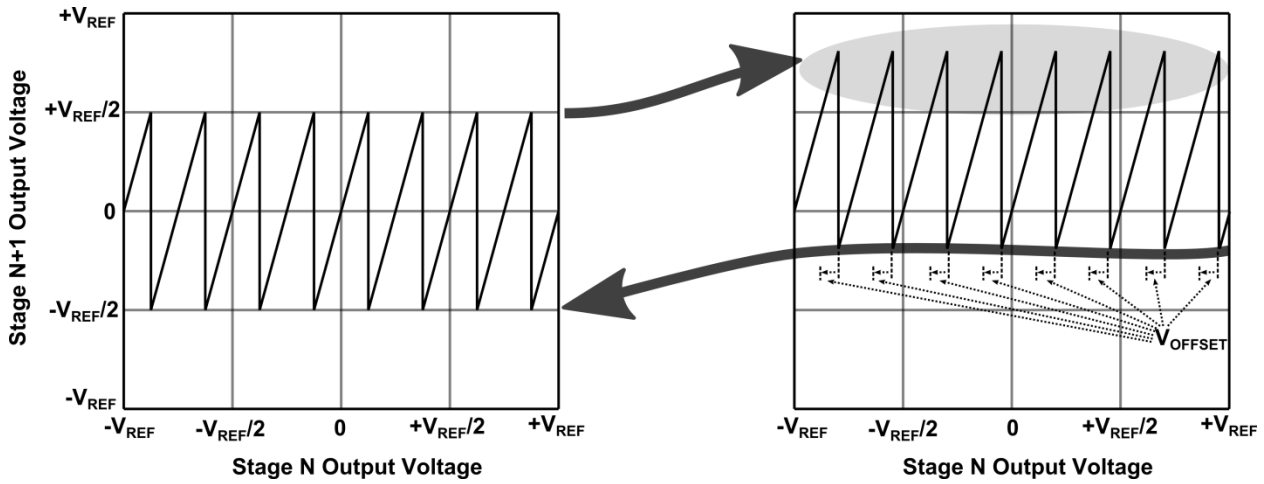
The variation of the offset is

$$\Delta V_{FINE} = \Delta \frac{dv_c}{dt_c} t_{ZCD,coarse} + \Delta \frac{dv_f}{dt_f} t_{ZCD,fine} \tag{4.17}$$

The constant portion of the offset becomes a systematic offset in the residue curve.

4.4 Residue Shift

Figure 4-8 (a) shows the nominal MDAC residue without offset in the sub-ADC decision. The nominal output residue range is from $-V_{REF}/2$ to $+V_{REF}/2$ with a stage gain of 4. However, because the sub-ADC decision is made immediately after the coarse decision phase, the output voltage seen by the sub-ADC is lower than the final output by a constant amount, V_{FINE}. This effectively corresponds to a systematic offset on all sub-ADC comparators which causes the residue to shift up as shown in Figure 4-8 (b). In the gray area of Figure 4-8 (b), the residue extends outside the nominal residue range. This cuts into the digital error correction range and degrades the available headroom of the coarse current source. To remove this overshoot in the residue voltage, a calibrated systematic offset voltage, V_{OFFSET}, is added to all sub-ADC comparator inputs. This approach keeps the MDAC residue within the nominal range while retaining the speed advantage of early sub-ADC decisions**.** The offset depends on the ramp rate and ZCD delay, necessitating calibration.



(a) (b)

Figure 4-8: Residue shift. (a) Nominal residue. (b) Residue with comparator offset.

4.5 Calibration of Residue Range

The systematic offset needs to be cancelled out when using the early sub-ADC decision scheme. The systematic offset depends on the ramp rate and ZCD delay. If the offset cancellation is incorrect, then the residue may sit out of the nominal residue range. This may force the fine phase current source into the linear region, which can degrade linearity. However, this out of nominal residue range can be easily corrected by a background calibration loop. Figure 4-9 shows three cases of residues that are too low, normal, and too high.

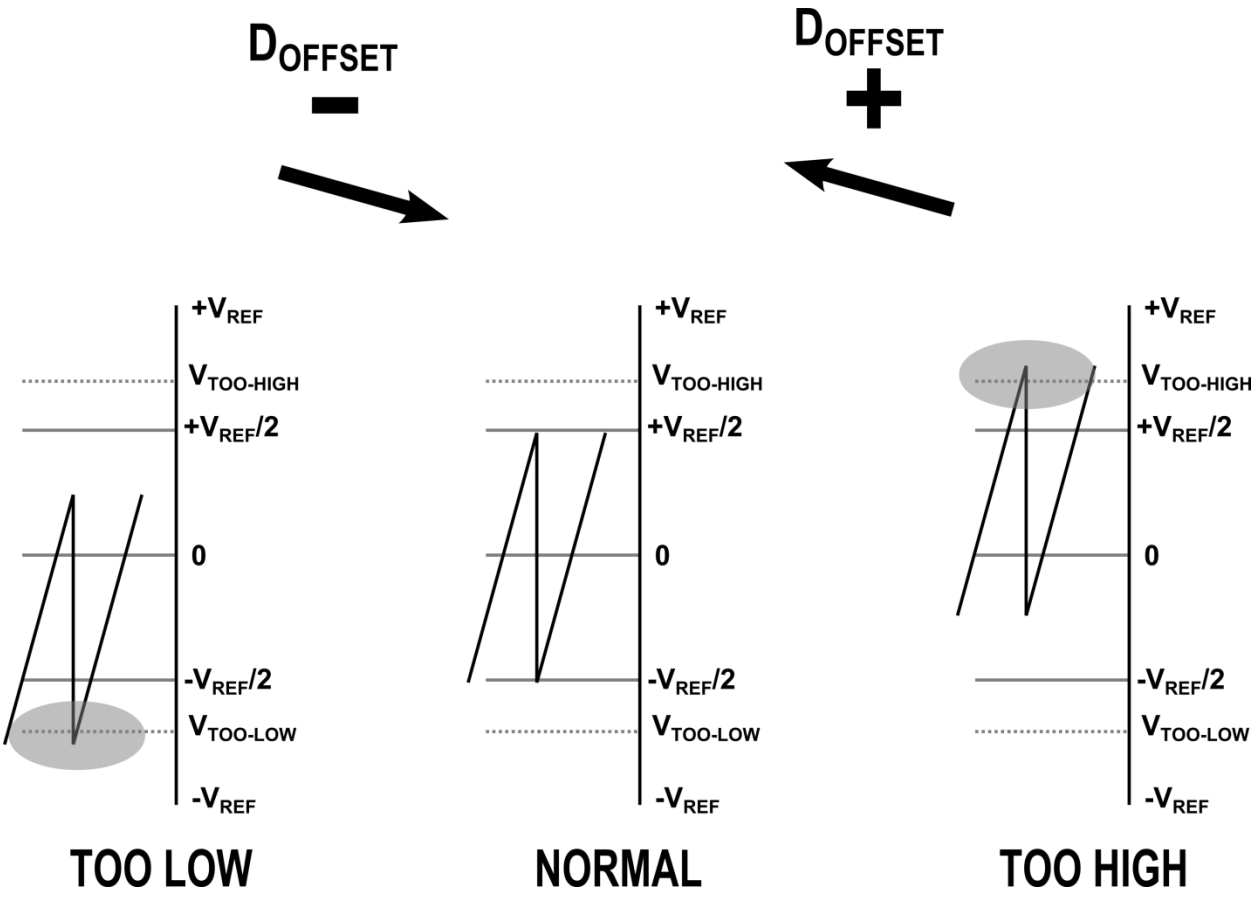


Figure 4-9: Diagram of residue calibration when the residue is too-low, normal, and too-high.

The condition of the residue being too low and too high can easily be detected by following a stage's comparators with reference voltages of $V_{TOO\text{-}LOW}$ and $V_{TOO\text{-}HIGH}$. Once this threshold voltage is detected, an accumulator changes its value based on positive or negative signal from the comparators. Then a digital code of D_{OFFSET} is fed back to the previous stage's reference resistor ladder, within the sub-ADC to change the systematic offset of the sub-ADC. This idea is illustrated in Figure 4-10. This calibration loop causes the output residue range to converge to the nominal range after several hundreds of sampling clock periods.

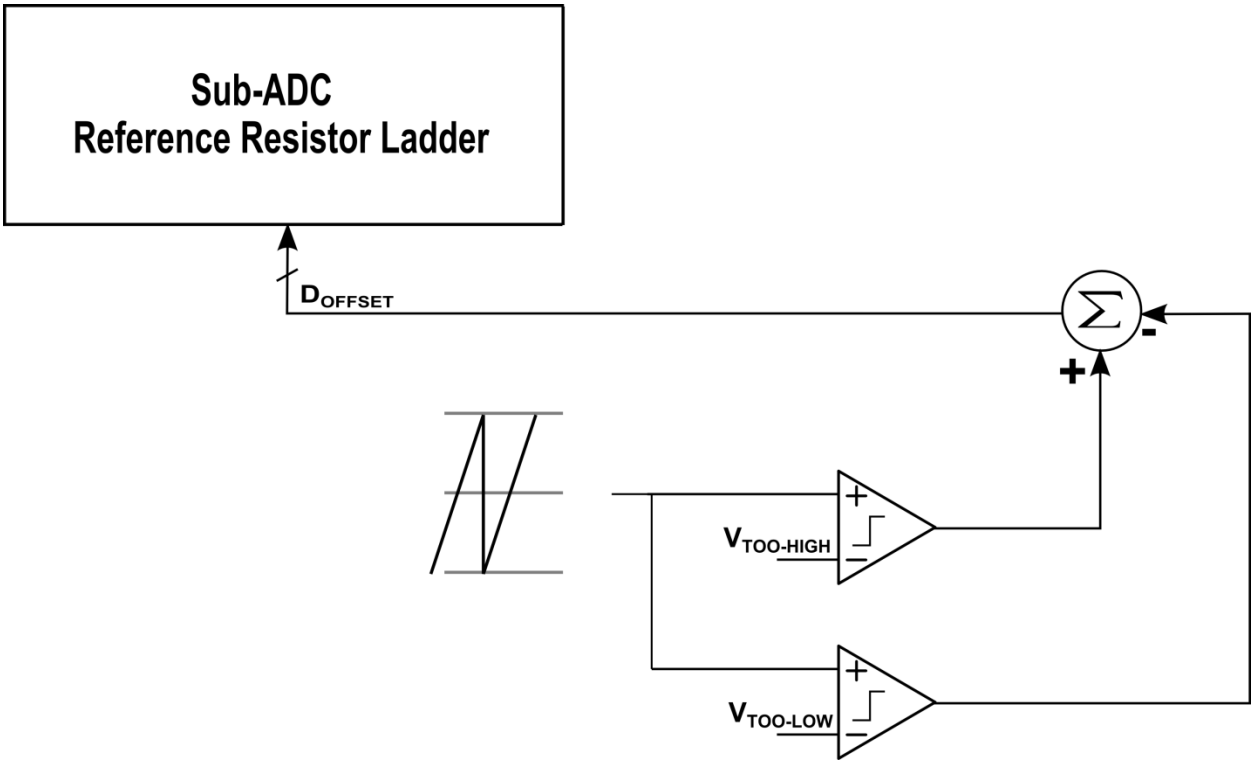


Figure 4-10: Block diagram of residue calibration.

4.6 Ramp Linearity Enhancement

4.6.1 Correlated Level Shifting (CLS) Technique

To reduce finite op-amp gain error and increase the op-amp's output swing, the correlated level shifting (CLS) technique was introduced in [15]; a block diagram of the circuit and waveforms for this scheme are shown in Figure 4-11.

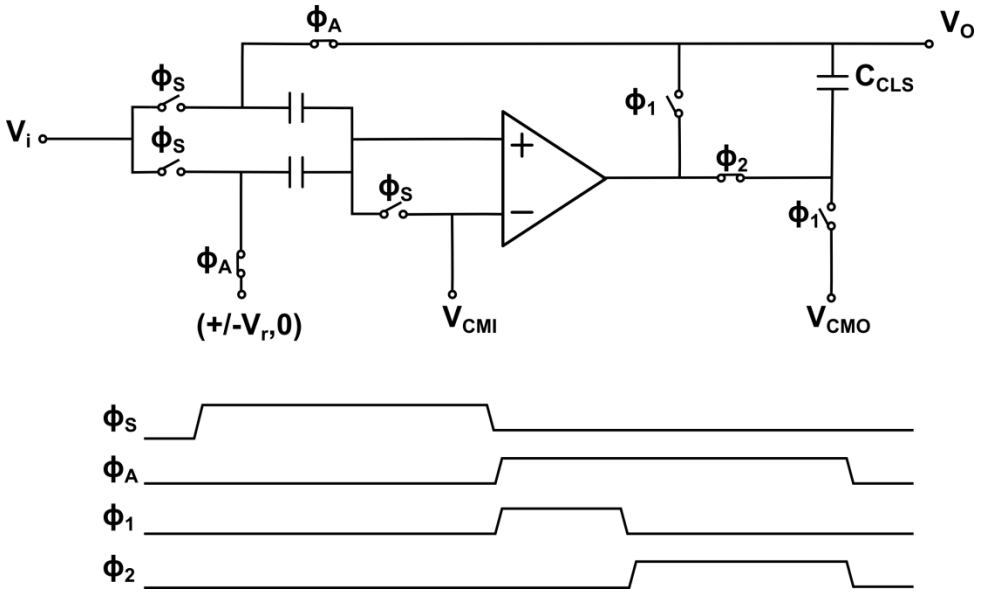


Figure 4-11: Correlated level shifting technique.

After sampling the input (ϕ_s), this switched capacitor circuit enters into an amplification phase (ϕ_A). CLS occurs during this amplification phase in two steps: estimation (ϕ_1) and level shifting (ϕ_2). In ϕ_1 the op-amp is connected directly to the output so that the level shifting capacitor samples an estimate of the correct output voltage with respect to the op-amp output common mode V_{CMO}. In ϕ_2, C_{CLS} is connected between V_o and the op-amp output, which level shifts the op-amp output to V_{CMO}. The op-amp only processes the error of the initial estimate and requires only small output swing because it only corrects this error. So the effective gain is

increased by the gain of the op-amp's estimation phase. The split-CLS technique of separating the op-amp into ZCBC for the estimation phase and a specific op-amp with high gain but reduced output swing for the level shifting phase was introduced to reduce the power consumption [16]. It still uses linear settling with feedback, but ZCBCs are inherently open-loop so there are no constraints with respect to feedback stability.

A similar CLS technique was proposed in ZCBC's [14], [21], [24]. Unlike the CLS in op-amp based circuits where settling must be interrupted to sample the coarse output voltage, this technique exploits the natural break in timing between the coarse and the fine phases. The coarse output voltage is sampled when the ZCD trips at the end of the coarse phase. Thus, there is no speed penalty for the CLS in ZCBC's.

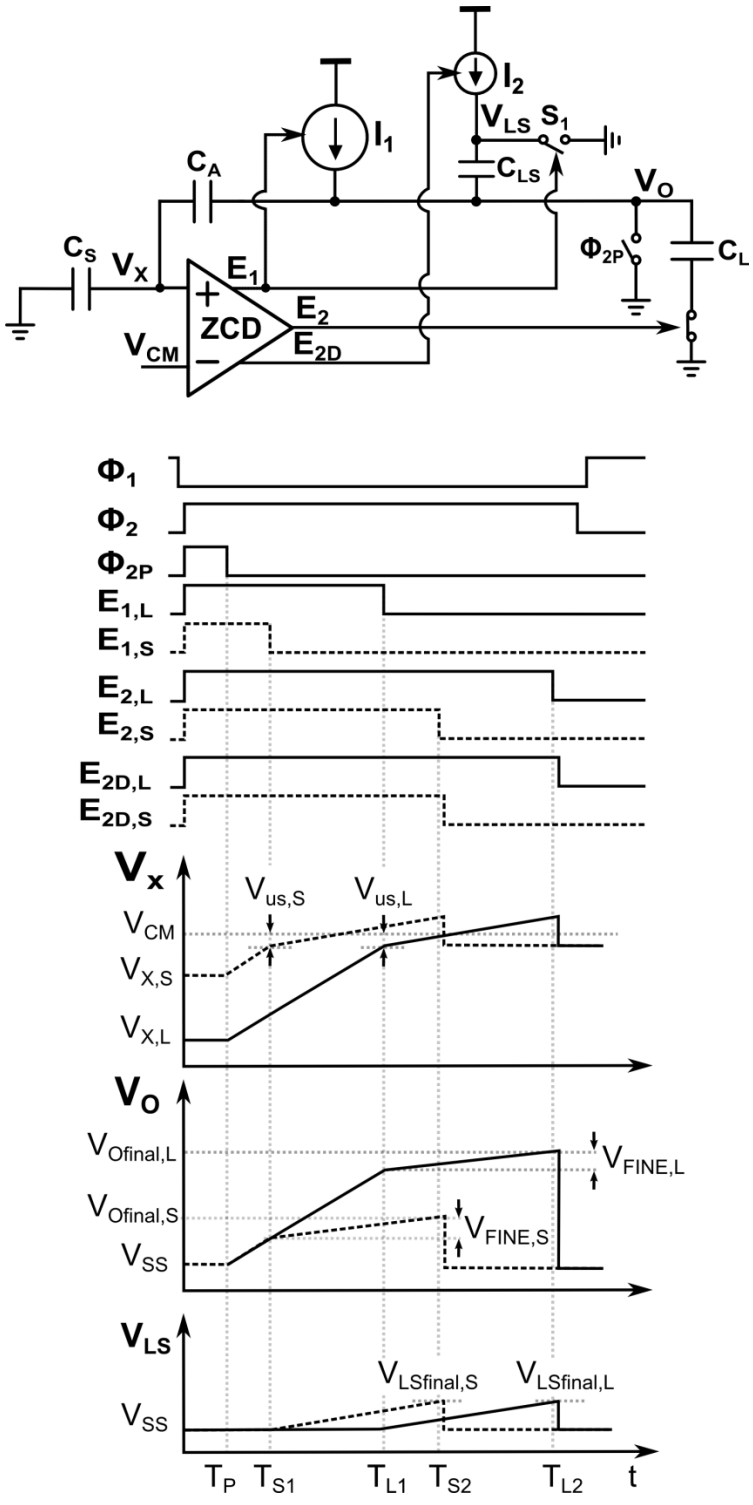


Figure 4-12: Simplified conceptual schematic of ZCBC with series charging capacitor for fine phase current source and timing diagram with a small residue (dotted line) and a large residue (solid line).

4.6.2 CLS with ZCBC

Figure 4-12 shows a simplified ZCBC schematic in the charge transfer phase with the level shifting capacitor C_{LS}, the coarse current source I_1, the fine current source I_2, and switches for the fine phase current source. The two bottom-most plots in Figure 4-12 show timing diagrams for the clock signals and waveforms illustrating two extreme cases of output residue voltages, one small and one large. The dotted line waveforms represent a small output residue and are denoted with a 'S' subscript, while a solid line is used for the large output residue waveforms that have an 'L' subscript.

It is clear that the differential input voltages to the ZCD (V_X) initially depend on the output residue voltage during the preset phase Φ_{2P}. However, at the end of the coarse phase (on the falling edge of E_1) both the small and large residue ZCD input waveforms transition from a coarse ramp to a fine ramp at approximately the same undershoot voltage, $V_{us,S}$ and $V_{us,L}$, respectively. The ZCD input voltage is related to the output voltage by the capacitive divider formed by C_A and C_S, at the end of the coarse ramp. Also, the output voltages $V_{O,S}$ and $V_{O,L}$ undershoot the final values ($V_{Ofinal,S}$ and $V_{Ofinal,L}$) by relatively small and nearly constant amount, shown as $V_{FINE,S}$ and $V_{FINE,L}$. Both waveforms, $V_{O,S}$ and $V_{O,L}$, then ramp in the fine phase, cross zero, and the E_2 signals end the charge transfer.

If the fine current source were applied to the output voltage directly, the current source would need to meet the linearity requirements over the entire output residue range, which is quite challenging. By using the CLS technique to connect the fine current source to the output voltage through a series capacitor, the current source output waveforms have a significantly reduced voltage range, as shown in the plot of V_{LS} at the very bottom of Figure 4-12. In this case, the maximum output range of the current source is limited to $V_{LSfinal}$, which is a fraction of the

overall residue range. In addition to the reduced range seen by the current source that makes high output resistance straightforward to implement, the variation of output voltage at the current source drain is also drastically reduced.

This concept is further illustrated in Figure 4-13 for a PMOS cascode fine ramp current source. Without CLS, the variation in the voltage at the current source output is shown as ΔV_{Ofinal}. With CLS, the voltage trajectory is nearly constant, resulting in near-constant overshoot that is limited by the precision of the coarse phase ($\Delta V_{LSfinal}$). By way of explanation, after the coarse phase, the incomplete settling coupled with the coarse current source's output resistance, result in slightly different undershoot voltages $V_{us,S}$ and $V_{us,L}$ at the ZCD input. These different undershoot voltages change the amount of voltage provided by the fine ramp V_{FINE}, which results in slightly different final voltages $V_{LSfinal,S}$ and $V_{LSfinal,L}$ at the zero-crossing instant.

Although this figure exaggerates the non-linearity for purposes of illustration, simulations indicate a linearity improvement of approximately 30dB by using a fine current source with CLS compared to the variation of a current source without level shifting. CLS therefore allows the same current source to be operated in a way that is much less sensitive to the data-dependent output residue voltage.

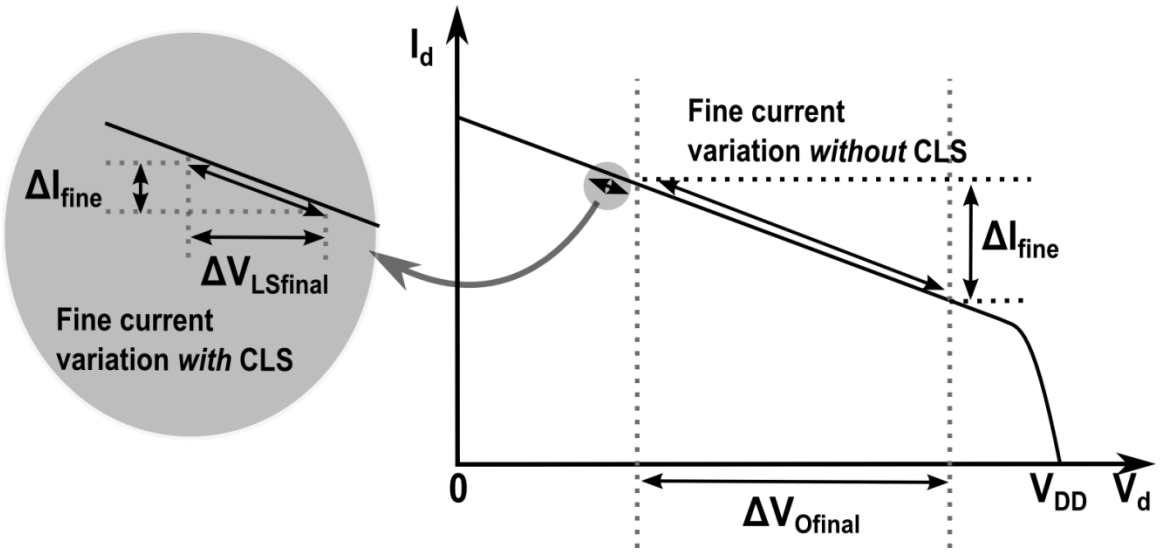


Figure 4-13: Effect of level shifting capacitor for the fine phase current source.

Note that there is a capacitive voltage divider between the fine current source output V_{LS} and the output V_{OUT} of corresponding stage. The voltage division ratio is proportional to C_{LS} for small values of C_{LS}, and the ratio approaches unity for a very large C_{LS}. While a small value of C_{LS} has less capacitive loading of the coarse ramp, the fine current source output range is increased and the fine ramp linearity is accordingly degraded. In this design, the size of C_{LS} was selected through simulation to achieve good fine current source linearity by maintaining a modest range for V_{LS} while also balancing the impact of the increased capacitance during the coarse ramp.

4.7 Summary

Limiting constraints on ramps for single phase and dual phase architectures were reviewed in this chapter. Dual ramp architecture not only reduces the ramp rate significantly and it also allows early sub-ADC decision for high speed operation. However, this early sub-ADC decision introduces systematic offset that must be resolved since it shifts output residue. Residue background calibration technique can remove the offset voltage between the output voltage of coarse phase and fine phase. To enhance ramp linearity with high speed operation, the CLS technique for fine current source dramatically improves the ramp linearity since CLS make the fine current source to be operated in a way that is much less sensitive to MDAC output residue voltage.

5 Implementation of a ZCBC Pipelined ADC

The previous chapters discussed several difficulties in using ZCBCs for high speed and high resolution along with several new techniques for surmounting these issues. These techniques are implemented and verified in a 12 b 200 MS/s pipelined ADC. In this design, a unidirectional dual ramp is adopted primarily because the fine current source can be turned on much earlier than in the bidirectional dual ramp [17]. This shortens the coarse phase duration, giving the fine current more time to settle before a zero-crossing event without consuming additional power. In addition, this strategy reduces transient disturbances during the transition from the coarse to fine phase current ramps, ultimately enabling a shorter fine phase. Finally, a unidirectional ramp relaxes the output range requirements for the coarse ramp current source.

5.1 Architecture

A top level block diagram of the ADC is depicted in Figure 5-1. The ADC consists of 4 stages and a final 4 bit flash. There is no sample-and-hold to reduce the power consumption. The first stage is composed of a 3.2b sub-ADC (8 comparators) and an MDAC with gain of 4. The second and third stages are scaled down by a factor of 2 from the first stage and second stage, respectively. The fourth stage is identical to the third stage. The standard redundancy for over range protection is used to relax offset constraints in both the sub-ADC comparators and the residue amplification, and to fold the residue within $V_{REF}/2$ to $-V_{REF}/2$. The reference buffer, bias circuits, and digital error correction circuits are all implemented on chip.

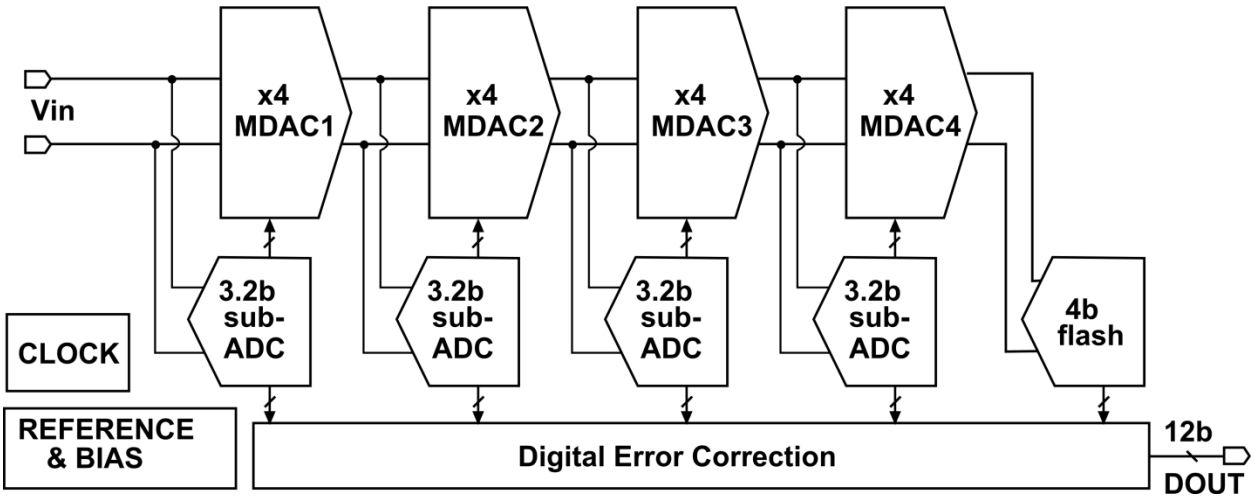


Figure 5-1: Proposed pipelined ADC architecture.

5.2 Frontend Sampling Circuits

The sample-and-hold amplifier (SHA) in the front-end of typical pipeline ADCs provides a constant DC signal to the pipeline stages once it samples. It therefore relaxes the path matching requirements between the signal going to the residue amplifier and the bit decision sub-ADC of the first stage. On the other hand, SHAs consume a lot of power because they must have sufficient bandwidth and accuracy. An ADC without an SHA is very power efficient and also less noisy [26]. There are constraints to adopting a SHA-less architecture, however. The sampled signal on the first MDAC and sub-ADC must match within the correction range of the first stage. The correction range is limited by the number of bits in the first stage.

Assume the analog input signal is a sine wave given by,

$$V_{in} = A\,sin(2\pi f_{in} t) \tag{5.1}$$

So it has a maximum slope given by

$$\left.\frac{dV}{dt}\right|_{max} = 2\pi f_{in} A \tag{5.2}$$

A mismatch time skew results in the voltage error as follows:

$$V_{error} = A2\pi f_{in}\Delta\tau \tag{5.3}$$

where $\Delta\tau$ is skew on the time constant. Timing skew affects mismatch more as the input frequency increases. If two signal paths have skew then it degrades SNR at high frequencies as well. Any mismatch between the two paths will cut the over-range protection of the pipeline stage.

In this ADC, two signal paths were carefully laid out and verified with the simulation. To get better linearity performance while sampling the input voltage, bootstrap techniques were used. The bootstrap switches reduce on resistance with the same size transistors and maintains the same V_{GS} with different input voltage as shown [27] by the V_G waveform in Figure 5-2.

$$V_G = V_{in} + \frac{C_b}{C_b + C_p} V_{DD} \tag{5.4}$$

where C_p is the total parasitic capacitance connected to the top plate of C_b. The gates of sampling switches on MDAC1 and bit decision comparators are all gate boosted. The sizes of the NMOS are chosen to minimize difference in the time constant of NMOS and sampling capacitors.

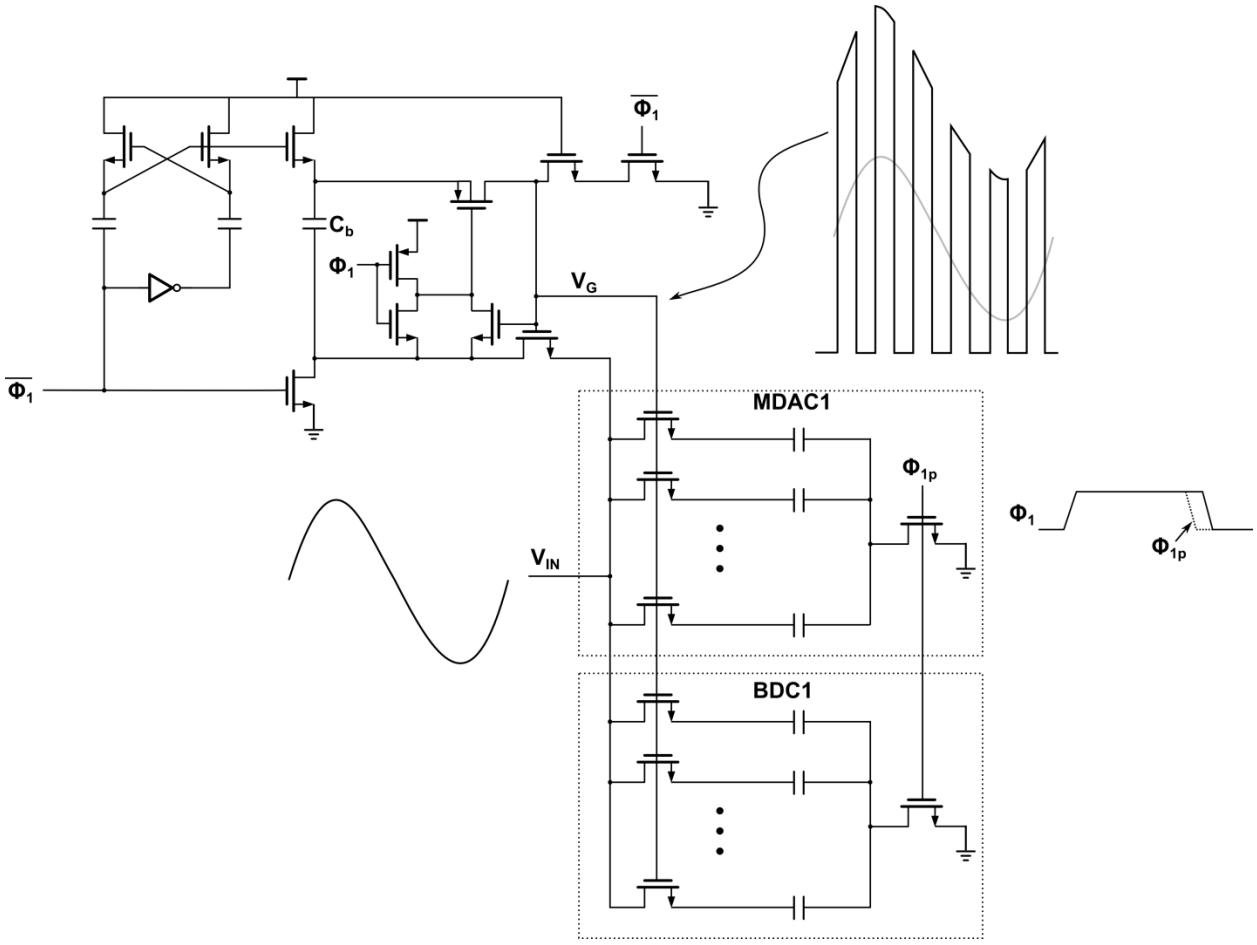


Figure 5-2: Frontend sampling circuits.

5.3 ZCBC pipeline stage

A simplified schematic of a ZCBC 3.2bit/stage pipelined ADC is shown in Figure 5-3. Each stage has switched-capacitor circuits with a sub-ADC, reference presampling capacitors $C_{R\pm}$, a ZCD, coarse and fine current sources, level shifting capacitors $C_{LS\pm}$, sampling capacitors $C_{S\pm}$ and amplification capacitors $C_{A\pm}$. Stage N is in the charge transfer phase and stage N+1 is in the sampling phase in Figure 5-3. The grey lines delineate the blocks that are disabled in these phases. A corresponding timing diagram is shown in Figure 5-4. The input voltage and reference voltage are sampled on $C_{S\pm}$ and $C_{A\pm}$ during the sampling phase (Φ_1). In the charge transfer phase (Φ_2), this charge is then subsequently added or subtracted based on the sub-ADC's output using switches SW.

With the proposed reference precharge architecture there is approximately a factor of 1.8 penalty in noise gain compared to a conventional architecture. To compensate for this increased noise, additional power is spent to reduce the input referred noise contribution of the ZCD.

Not shown are systematic calibration signals from stage N+1's sub-ADC to stage N's sub-ADC. The first stage's sampling capacitor is selected to make the thermal noise much less than the quantization noise. The signal-to-noise-ratio (SNR) for a given sampling capacitor value with quantization noise is

$$SNR = 10log\left(\frac{\frac{V_{FS}^2}{2}}{\frac{\Delta^2}{12}+\frac{kT}{C}}\right) \tag{5.5}$$

where Δ is the quantization step and V_{FS} is the full scale of the reference voltage.

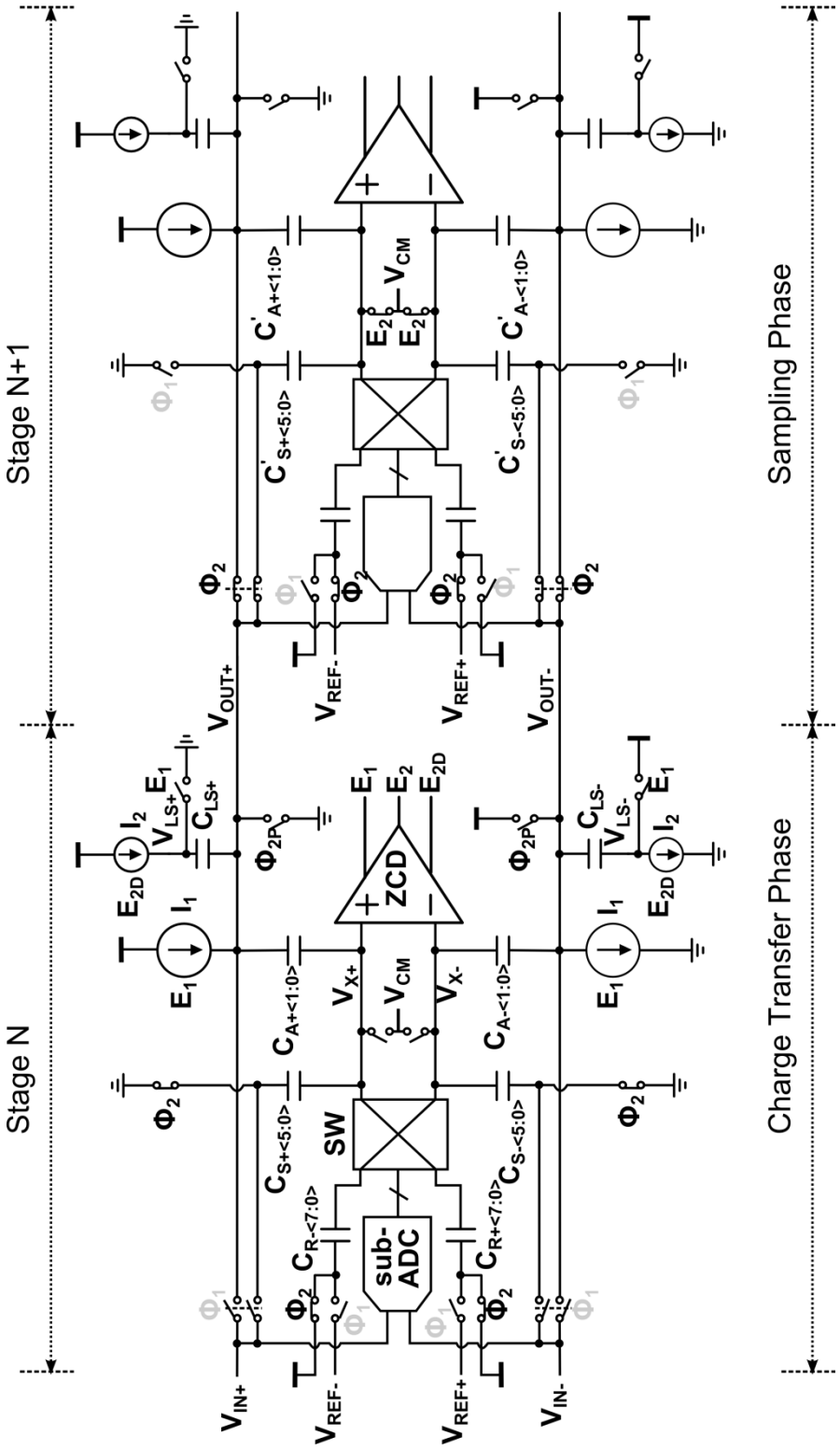


Figure 5-3: Simplified schematic of the ZCBC pipeline stages.

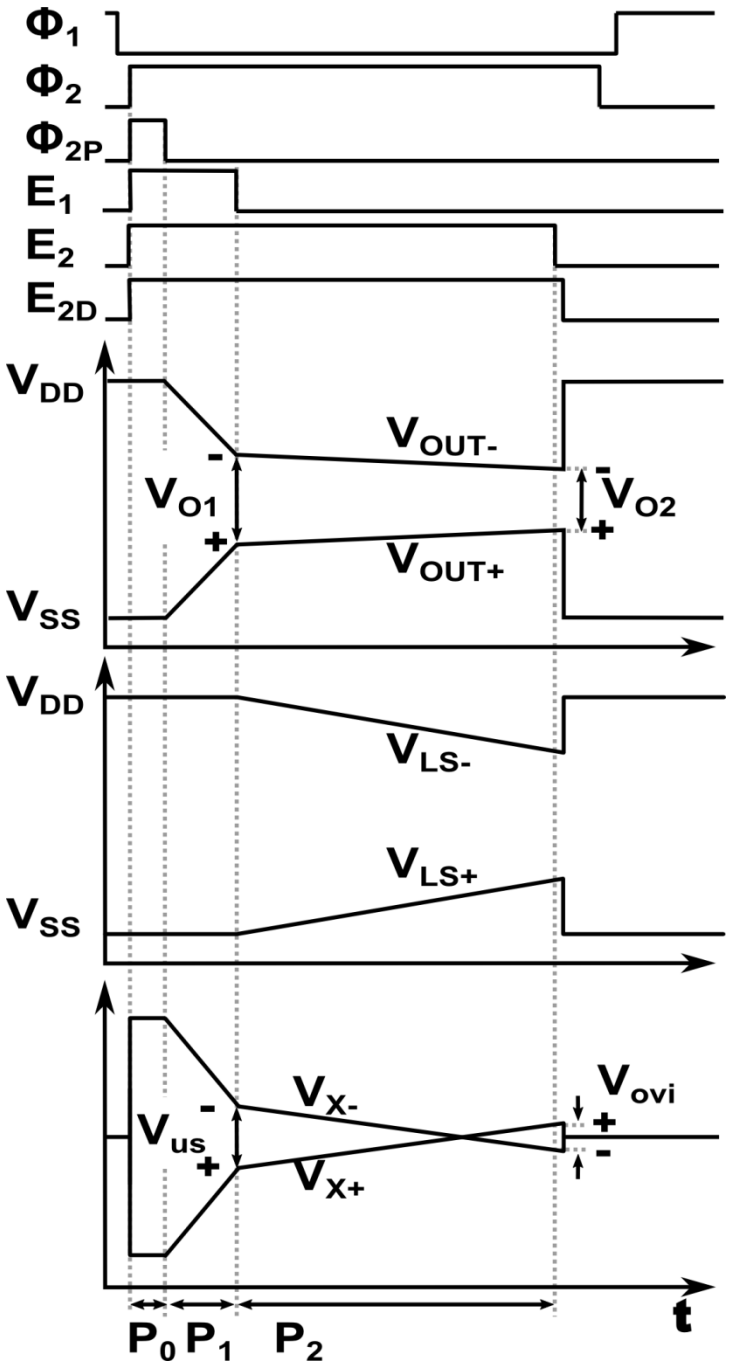


Figure 5-4: Timing diagram of the ZCBC stage.

The operations of ZCBC charge transfer in the preset, coarse, and fine phases are illustrated with the simplified schematics and timing diagrams in the following two figures. Grey arrows show the direction of current flow. In the preset phase (P_0) shown in Figure 5-5, a short preset signal Φ_{2P} sets V_{OUT+} to V_{SS} and V_{OUT-} to V_{DD} in order to ensure that the differential input to the ZCD starts from a negative voltage at the start of the coarse phase (P_1). At the beginning of the preset phase, E_1 and E_{2D} also turn on to reduce transient effects in the transition from the coarse phase to the fine phase.

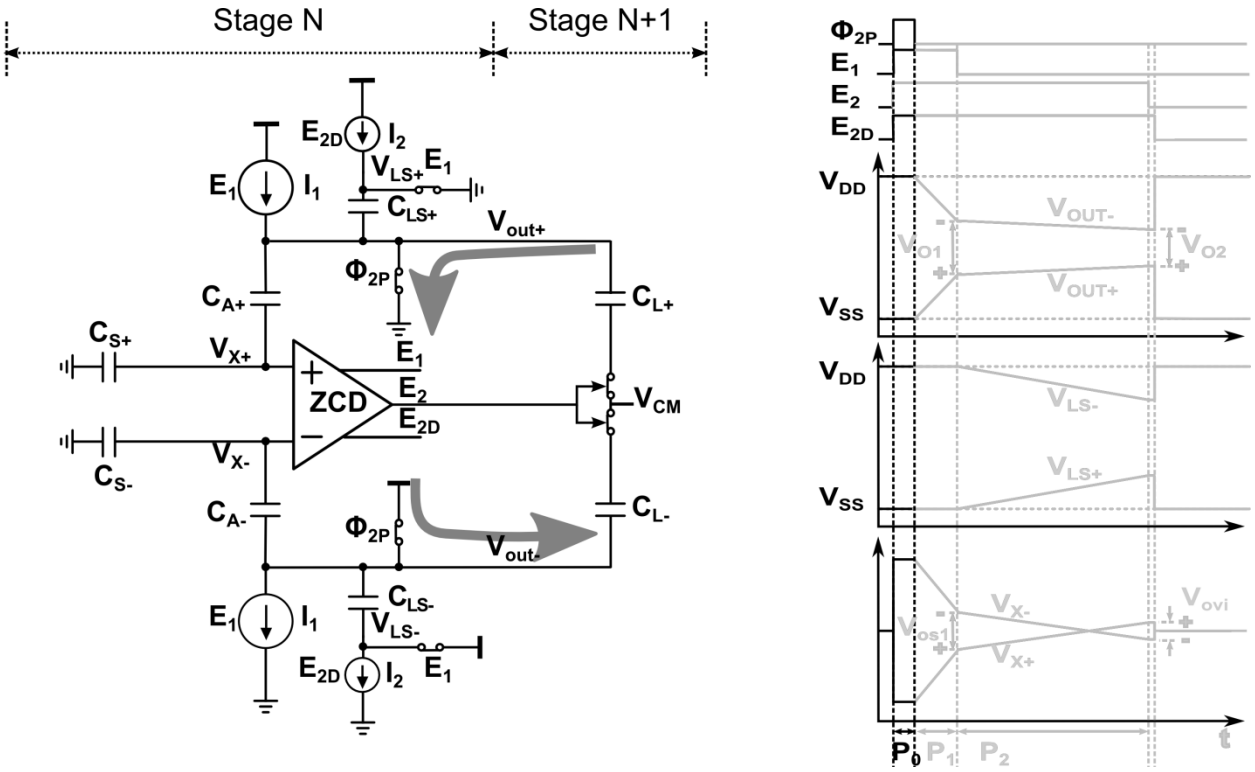


Figure 5-5: Preset phase.

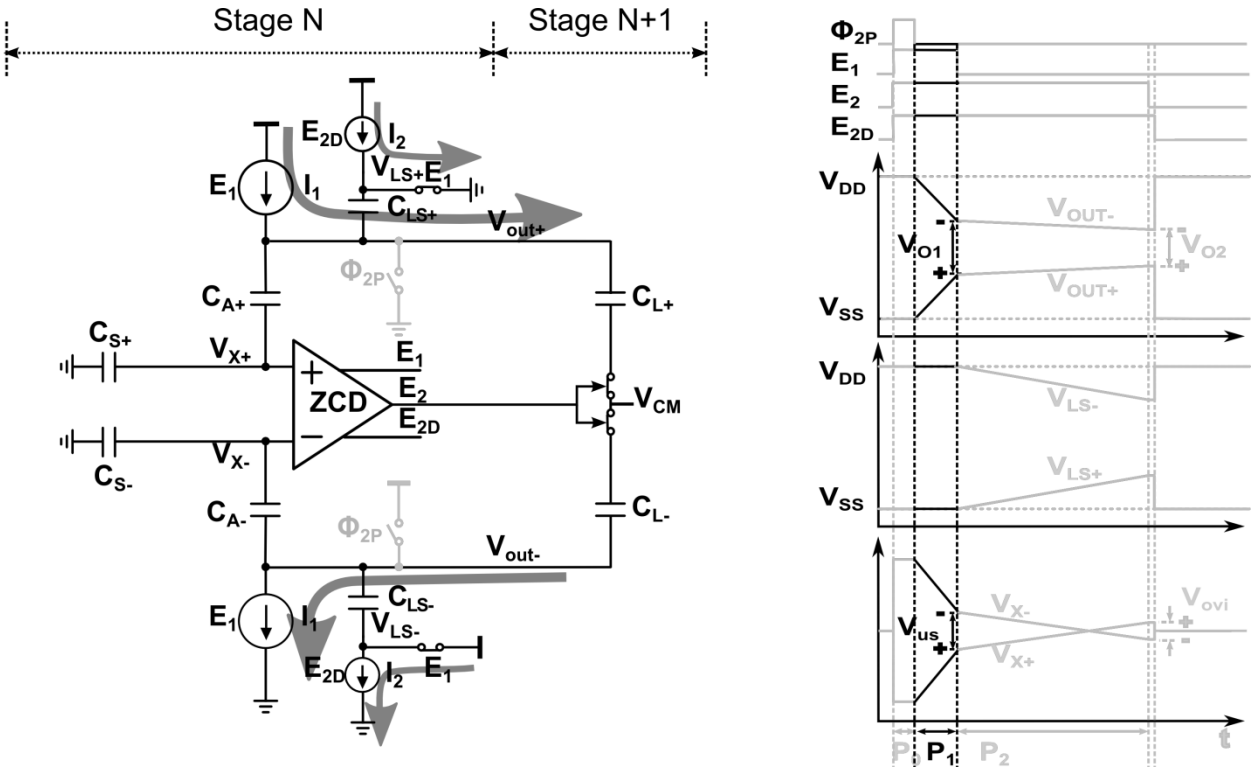


Figure 5-6: Coarse phase.

After Φ_{2P} turns off, the coarse phase begins as shown in Figure 5-6. E_1 controls the coarse phase and coarse current I_1 charges V_{OUT+} and discharges V_{OUT-} at a fast rate until V_{x+} and V_{x-} cross the offset voltage V_{us}. At this point, the next stage's sub-ADC strobes the output voltage V_{O1} and begins to make a decision. In this coarse phase the fine current sources I_2 are already turned on to reduce transient effects from the transition of the coarse phase to fine phase. The level shifting capacitors are also set (V_{LS+} to V_{SS} and V_{LS-} to V_{DD}) by E_1 until the coarse phase ends to improve the fine phase ramp linearity.

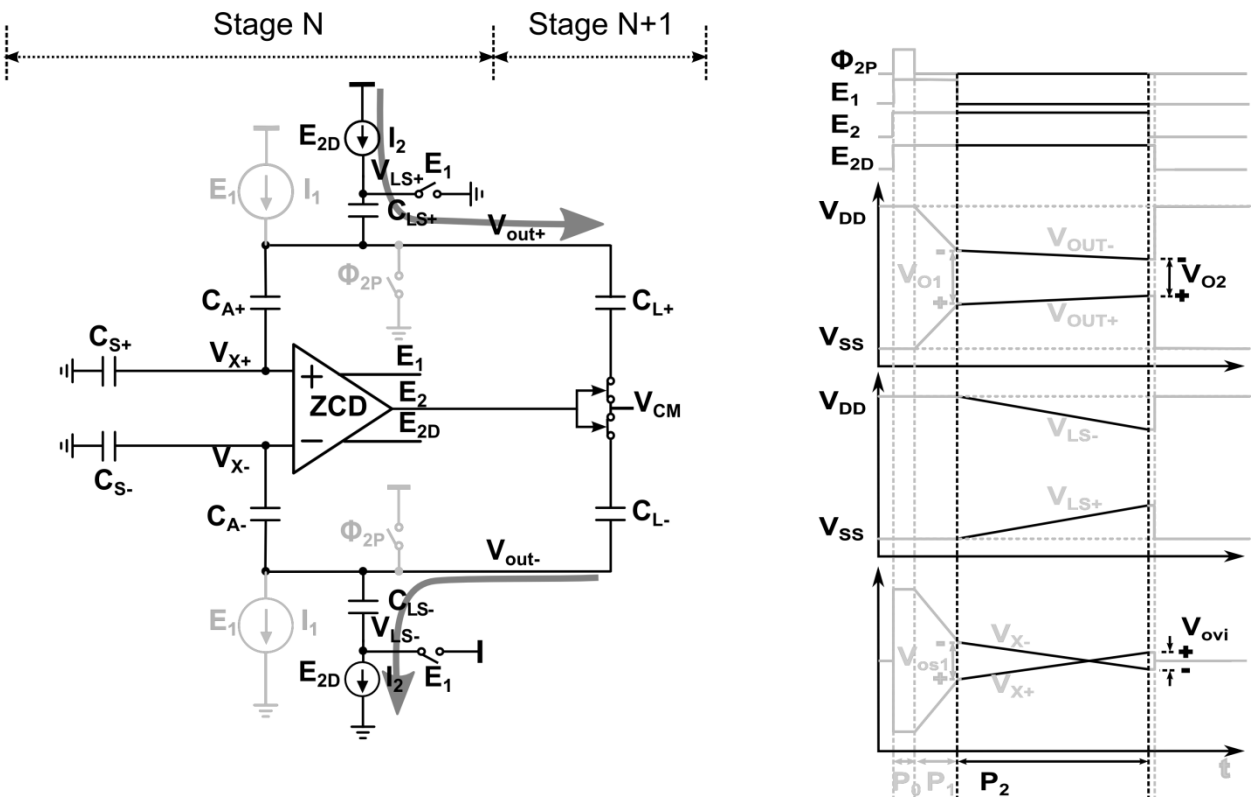


Figure 5-7: Fine phase.

After the coarse phase, the fine phase starts as shown in Figure 5-7. E_1 disconnects V_{LS+} from V_{SS} and V_{LS-} from V_{DD} so the fine phase (P_2) current I_2 through level shifting capacitor $C_{LS\pm}$ begins to charge V_{OUT+} and discharges V_{OUT-} at a slow rate. When V_{x+} crosses V_{x-}, the sampling signal E_2 falls to open the sampling switches. The output voltage V_{O2} is accurately sampled on the next stage capacitors $C`_{S\pm}$ and $C`_{A\pm}$ at that instant. Because the ZCD has a finite delay, I_2 turns off shortly after V_{x+} crosses V_{x-}, so this delay combined with the ramp rate causes a relatively constant overshoot (V_{OV2}). The current source with level shifting capacitor greatly reduces variation of this overshoot and its associated nonlinearities. Figure 5-8 shows the trajectories of simulated waveforms at the stage output, level shifting node, and input voltage of

the ZCD within a half clock cycle. After the fine phase, both V_{LS+} and V_{LS-} are pulled up to V_{DD} to prevent $C_{LS}\pm$ from being floating during the next sampling phase.

The initial voltage in the preset phase is defined by the sampled input voltage and bit decision result. Because the input voltage is sampled on both $C_{S\pm}$ and $C_{A\pm}$, then C_{A-} is connected to V_{DD} and C_{A+} is connected to V_{SS}, V_{x-} is always above V_{CM} and V_{x+} is always below V_{CM} in the preset phase, allowing for a unidirectional ramp.

In the coarse phase, the output ramps at a fast rate until the coarse detector makes its decision. The duration of P_1 depends on the initial voltage $\Delta V_x=V_{x+}-V_{x-}$. If ΔV_x is close to V_{os1}, it finishes in a short time. On the other hand if ΔV_x is large then it takes a longer time to finish the coarse ramp. Once the coarse detector senses $\Delta V_x=V_{os1}$ the ZCBC enters the fine phase. The variation of the fine phase duration time is nearly constant because the offset variation after the coarse phase is very small. The fine current source sees almost the same drain voltage regardless of output voltages. V_{LS+} and V_{LS-} voltages are almost constant after the fine phase ramp.

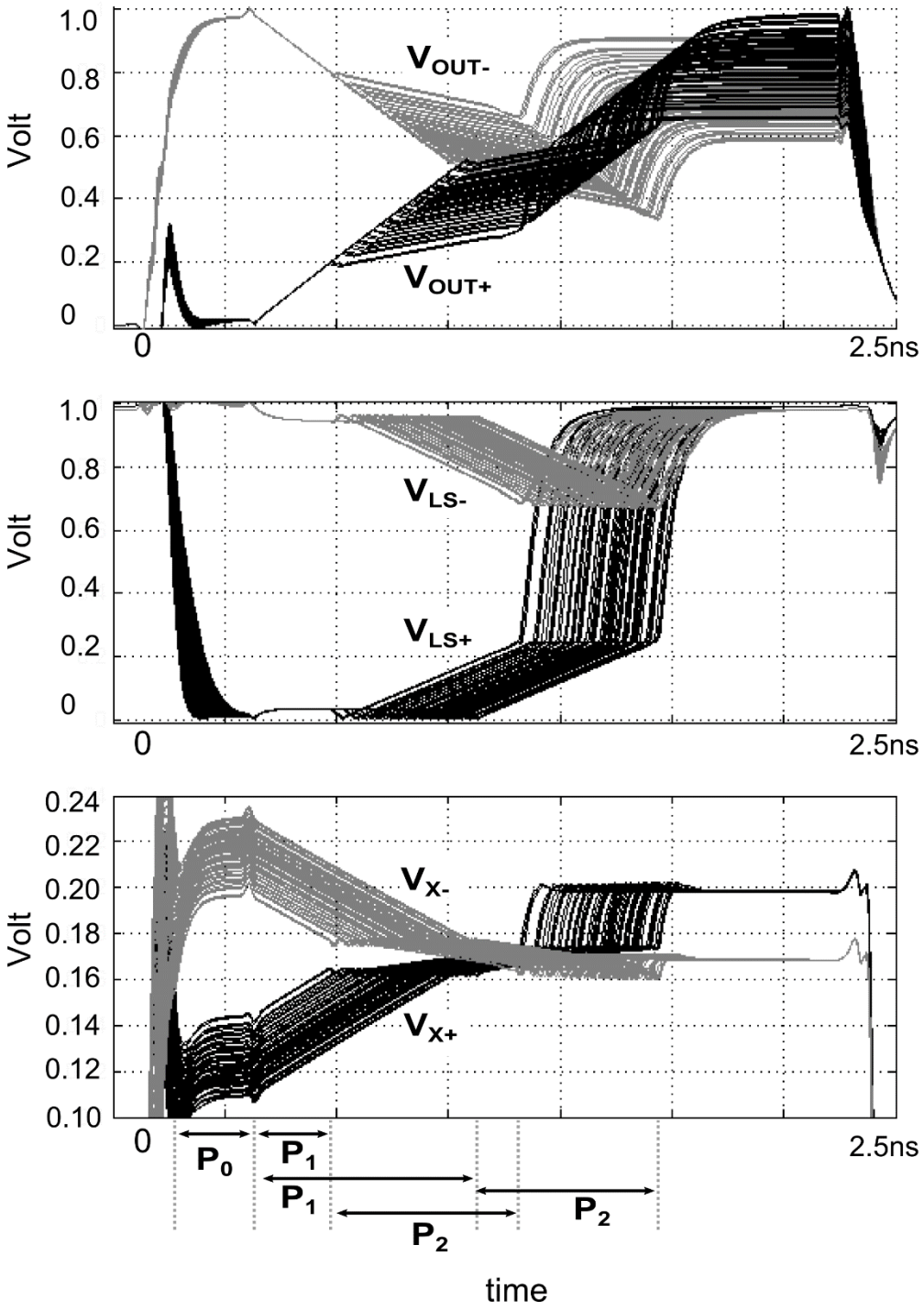


Figure 5-8: Superposition of simulated waveforms of the ZCBC stage within a half clock cycle.

5.4 Reference Precharge

Reference voltages ringing during switching events are a key challenge for high speed ADCs. This ringing, which is often attributed to parasitic package inductances, must be settled within half a LSB level of ADC's reference voltage in a half clock period. To allow more time for the reference voltage to settle, a precharge is added to the reference sampling capacitors $C_{R\pm}$ and the charges added or subtracted based on the sub-ADC's decision via switches SW. This procedure is shown in Figure 5-3. A drawback of using this reference precharge architecture is a noise gain penalty of a factor of 1.8 approximately compared to the case without precharging capacitors. To compensate for this increased noise, additional power consumption must be spent in the ZCD to reduce its input referred noise. A similar reference precharging architecture with reduced noise gain penalty was recently reported in [22].

5.5 Fine Current Source with Level shifting Capacitor

The current source and the associated switches are shown in Figure 5-9. M_{PC1-2} are the coarse current source and M_{PF1-2} are cascoded for the fine current source. Because of the fast ramp requirement during the coarse phase, the coarse charging current is very large so a gate boosting circuit is used to turn on and off M_S. This boosted V_G voltage reduces M_S's on-resistance with a reduced size.

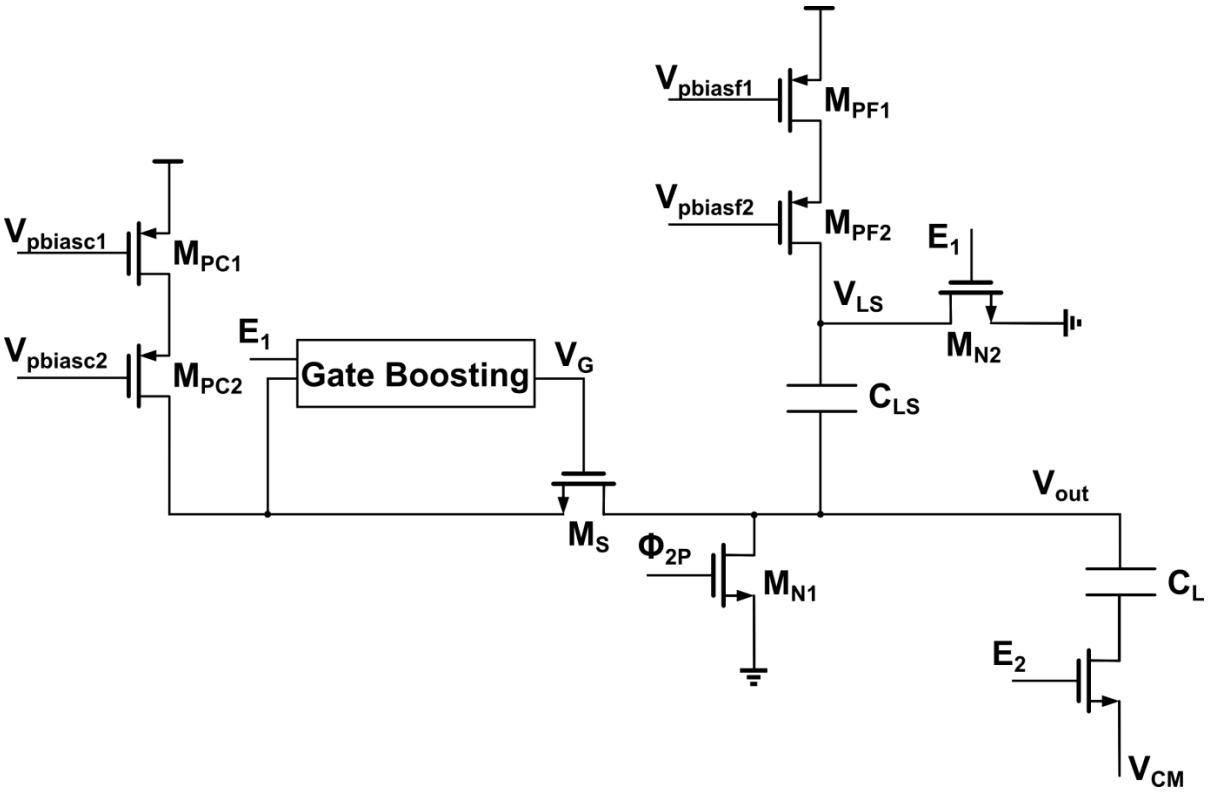


Figure 5-9: Schematic of current sources for coarse and fine phases.

5.6 Sub-ADC with Residue Range Calibration

As discussed in section 4-3, a sub-ADC decision is made right after the coarse phase instead of after fine phase. Figure 5-10 shows simulated waveforms for both small and large residue voltages at each stage's positive output. It shows almost constant offset voltage V_{FINE} between the coarse and the fine phases.

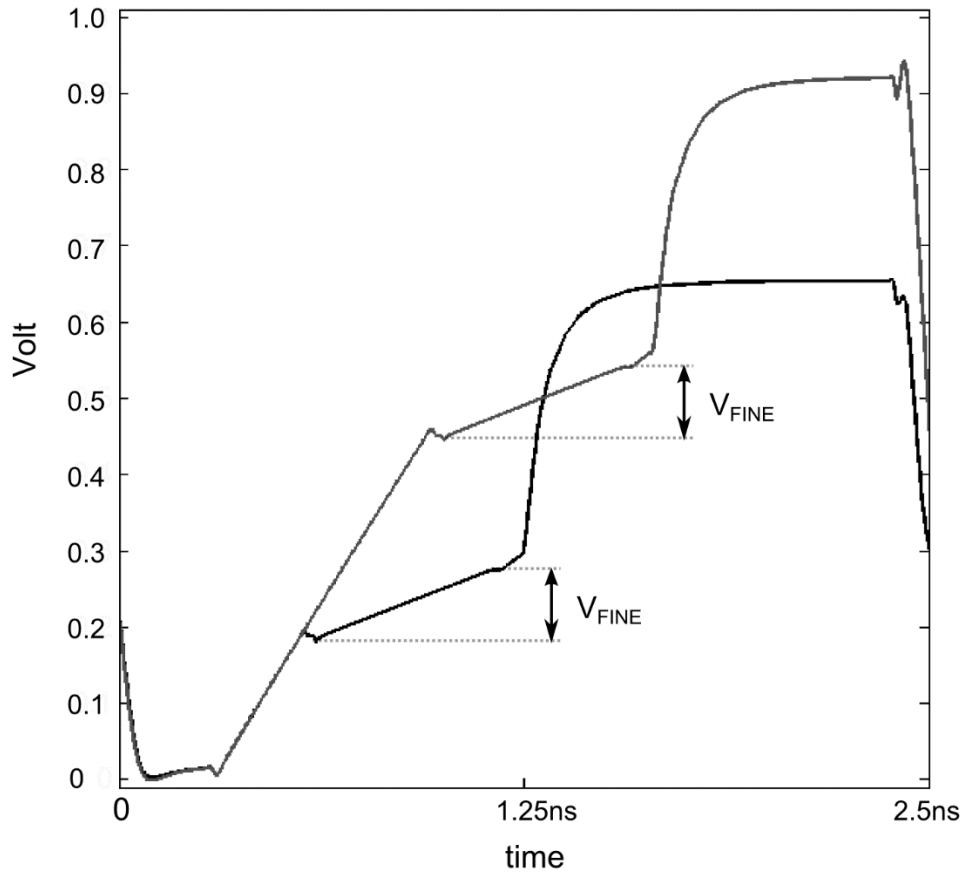


Figure 5-10: Comparison of simulated output waveforms of small and large residues at V_{OUT+}.

The sub-ADC used in all four gain stages consists of two reference resistor ladders and eight switched-capacitor comparators to realize a nine level (3.2bit) flash sub-ADC. For each sub-ADC in Stages 2-4 that follow a ZCBC, there are two additional comparators to detect residue-too-high and residue-too-low conditions for residue background calibration.

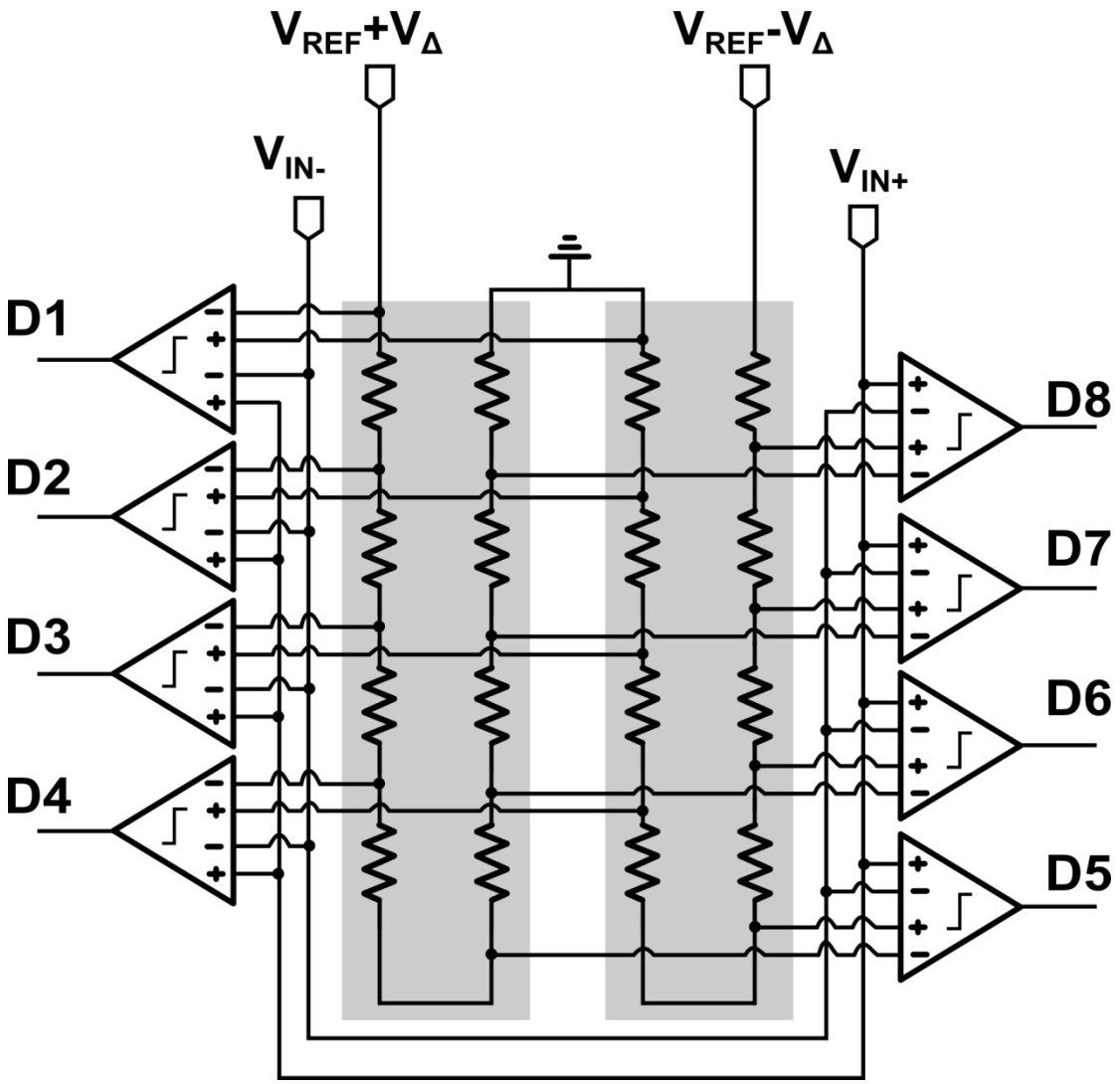


Figure 5-11: Schematic of sub-ADC.

In a traditional sub-ADC without an offset voltage, bipolar threshold voltages can be generated from a single resistor ladder. However, in this case the threshold voltages for each polarity are equal in magnitude. Here, we require a constant and systematic offset voltage V_{OFFSET} to compensate for the early sub-ADC decision. Figure 5-11 then shows the reference

ladder modifications that generate the differential threshold voltages of the sub-ADC comparators including the V_{OFFSET} term.

In Figure 5-11, two reference voltages (V_{REF}-V_{Δ}, V_{REF}+V_{Δ}) are applied to two parallel resistor ladders. The positive terminals for the threshold voltages are tapped from the first ladder at fractional values of (V_{REF}-V_{Δ})*{7/8, 6/8, 5/8, etc.}, and the negative terminals for the threshold voltages are tapped from the second ladder at fractional values of (V_{REF}+V_{Δ})*{1/8, 2/8, 3/8, etc.}. In this way, the full V_{Δ} is seen in each of the 8 differential threshold voltages such that the differential reference voltage of the i^{th} comparator ($i \in \{1,2,\ldots 8\}$) is given by:

$$\left(V_{REF} - V_{\Delta}\right)\frac{i-1}{8} - \left(V_{REF} + V_{\Delta}\right)\frac{9-i}{8} = (V_{REF})\frac{2i-10}{8} - V_{\Delta} \tag{5.6}$$

For example, the 8th comparator threshold is

$$\left(V_{REF} - V_{\Delta}\right)\frac{7}{8} - \left(V_{REF} + V_{\Delta}\right)\frac{1}{8} = (V_{REF})\frac{6}{8} - V_{\Delta} \tag{5.7}$$

When compared to the nominal threshold voltage for a traditional 9-level sub-ADC of 7/8V_{REF}, we find that V_{OFFSET} = V_{Δ} + V_{REF}/8. The choice to include an offset of V_{REF}/8 in all the thresholds was made to relax headroom issues on the lower supply voltage and to bring the resistor ladders closer to differential operation.

Figure 5-12 shows the schematic of the offset reference voltage generation circuit (ORVGC). It consists of a 2-stage op amp and a current steering DAC ($M_{10\text{-}12}$, $M'_{10\text{-}12}$) added to the output stage. ORVGC forces currents, I_S+I_C, on V_{O+}, and I_S-I_C on V_{O-} where I_S=I_1-I_0=I_2+I_3-I_0.

D_{OFFSET} code controls $I_{C.}$ The average voltage (V_{RCM}) of the top side of the two resistor ladders is feedback to the inverting input op-amp and changes $I_{1\text{-}3}$. Thus, V_{RCM} becomes V_{REF} with this common mode feedback and these different output currents from ORVGC generate $V_{REF} + V_{\Delta}$ on V_{O+}, $V_{REF} - V_{\Delta}$ on V_{O-} through R_{CM}, where $V_{\Delta} = I_{RCM}R_{CM}$. Thus, new reference voltages are generated on top of the resistor ladders and those are provided to all comparators in the sub-ADC with shifted reference voltages.

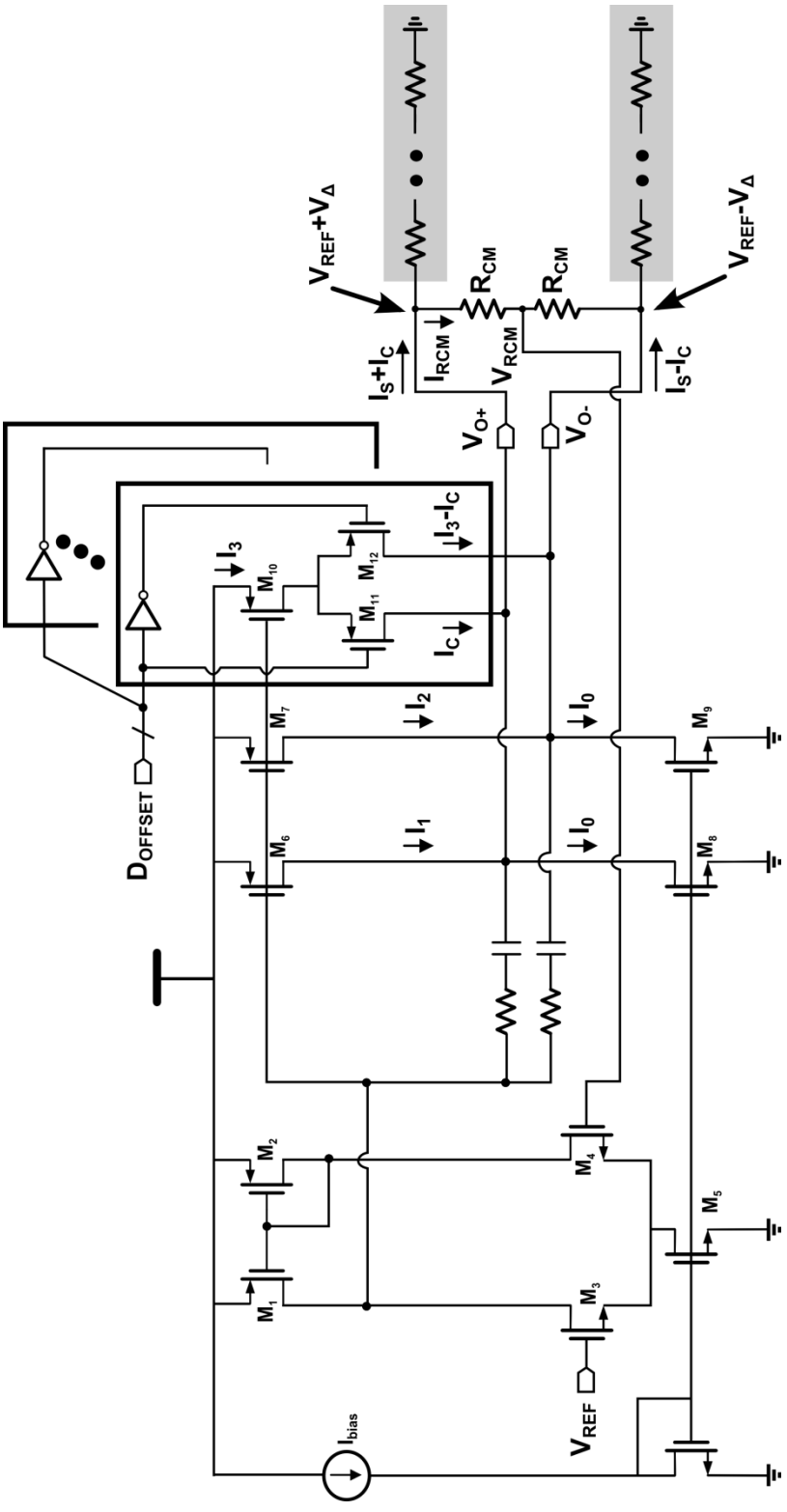


Figure 5-12: Schematic of offset generation block.

5.7 Residue Range Background Calibration

As discussed in the section 4-5, residue overshoot is calibrated with a background residue range calibration. A residue voltage of stage N which is either too low, or too high, is detected using the comparators of the N+1 stage with reference voltages of $V_{TOO\text{-}LOW}$, and $V_{TOO\text{-}HIGH}$, which are generated from a resistor ladder in the sub-ADC; shown in Figure 5-13. Whenever these threshold voltages are exceeded, an accumulator is incremented or decremented. The accumulator output D_{OFFSET} is fed back to the reference generation block in the stage N sub-ADC, to shift the reference voltages of the sub-ADC by a systematic offset. This background calibration causes the output residue range to converge to the desired nominal range after several hundreds of sampling clock periods.

Figure 5-14 shows the simulated residue voltages resulting from the background residue calibration. This simulation was performed by sweeping the temperature from -40 C˚ to 125 C˚ and varying the power supply voltage from 0.9 V to 1.1 V. In this simulation, the ADC is initiated at 0.5 μs at which time calibration begins. Figure 5- 14 shows the residue range converging in around 1.0 μs, which is approximately 200 cycles of sampling clock period. The output residue converges well within the nominal residue range as calibration runs in the background. A similar residue background calibration was recently proposed in [45]. Note that the calibration values are stored in digital registers and therefore can be held indefinitely regardless of the input signal statistics or activity.

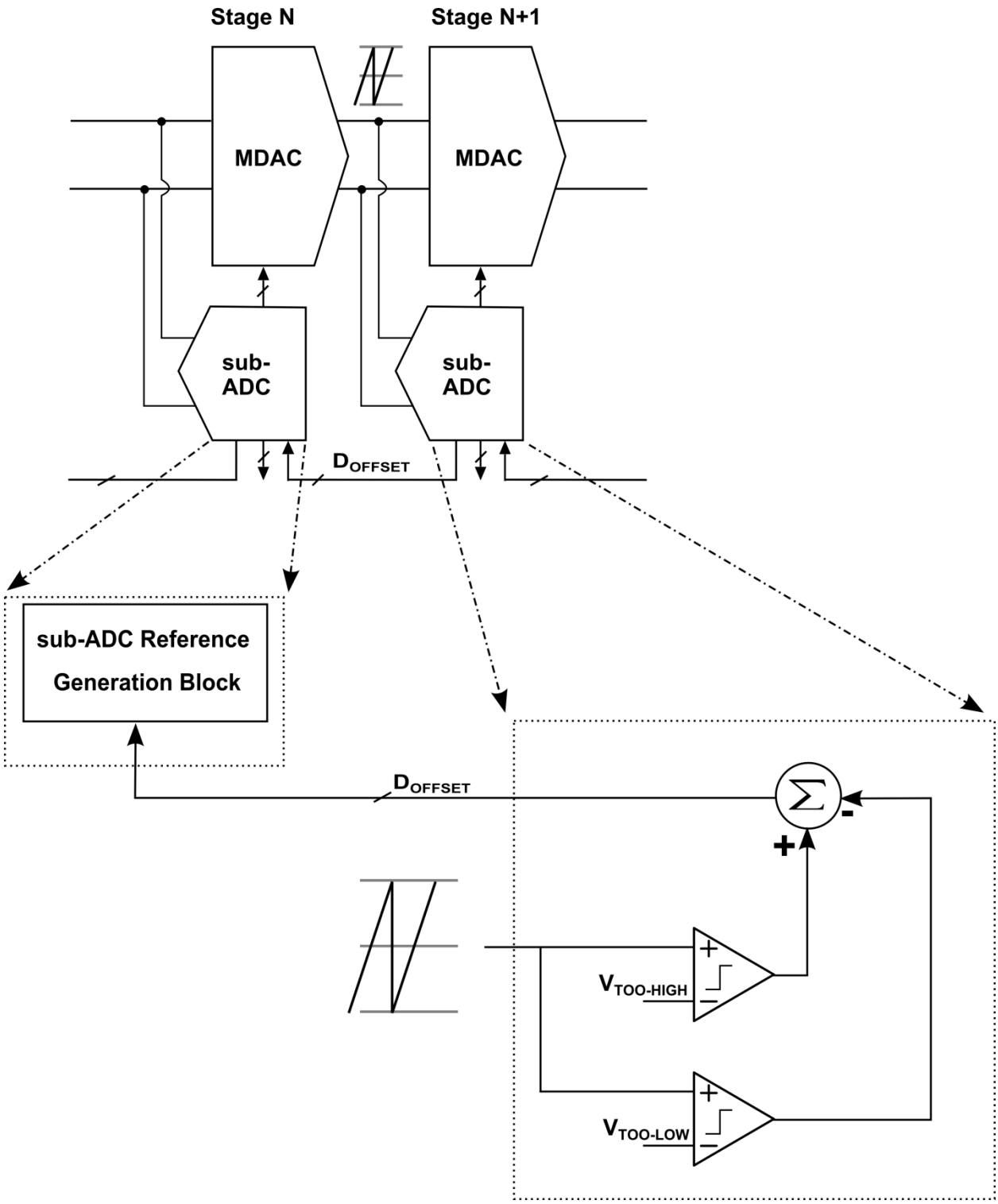


Figure 5-13: Calibration for residue range.

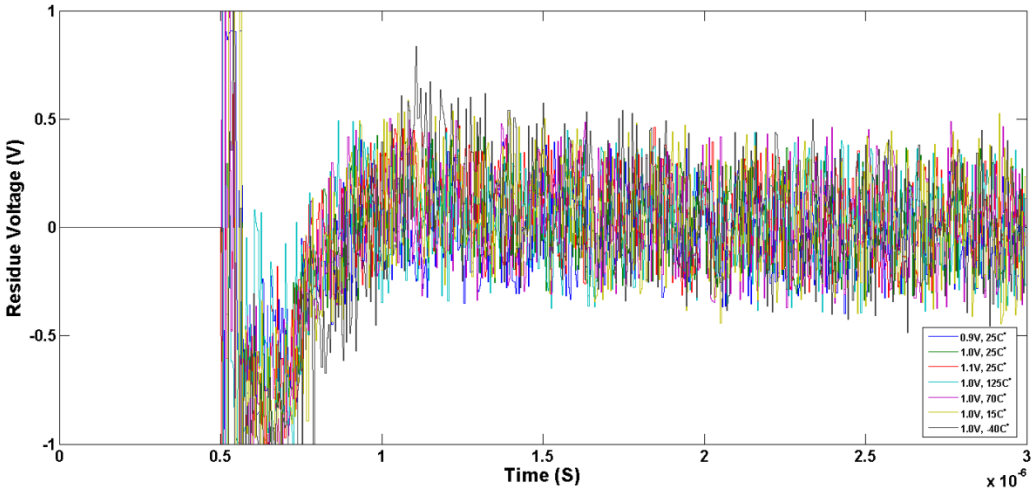
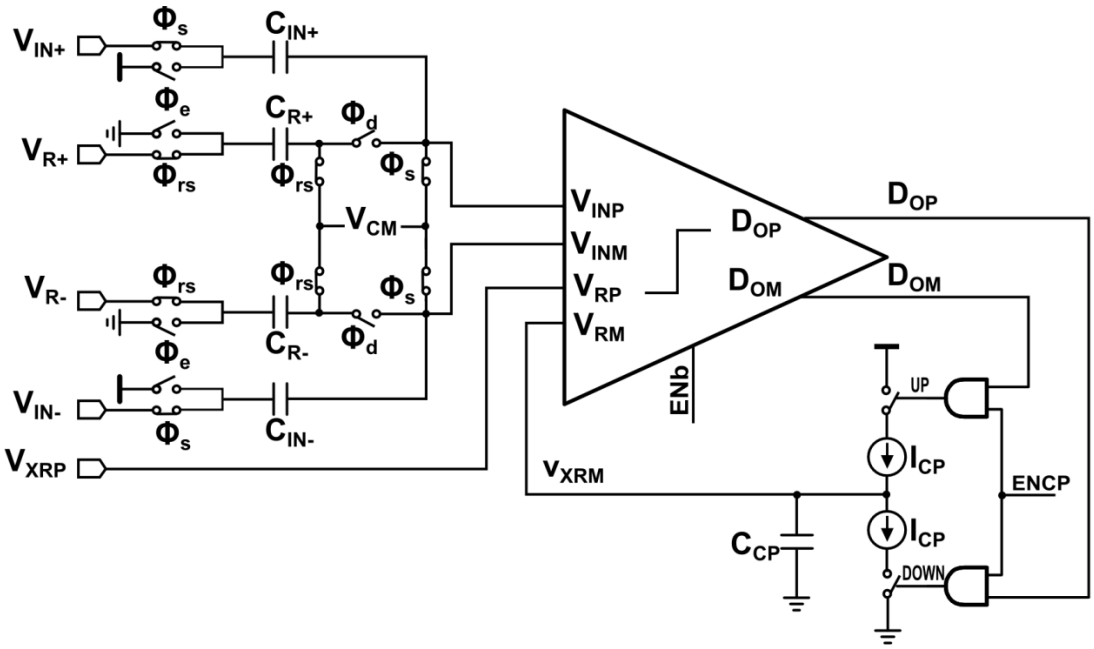


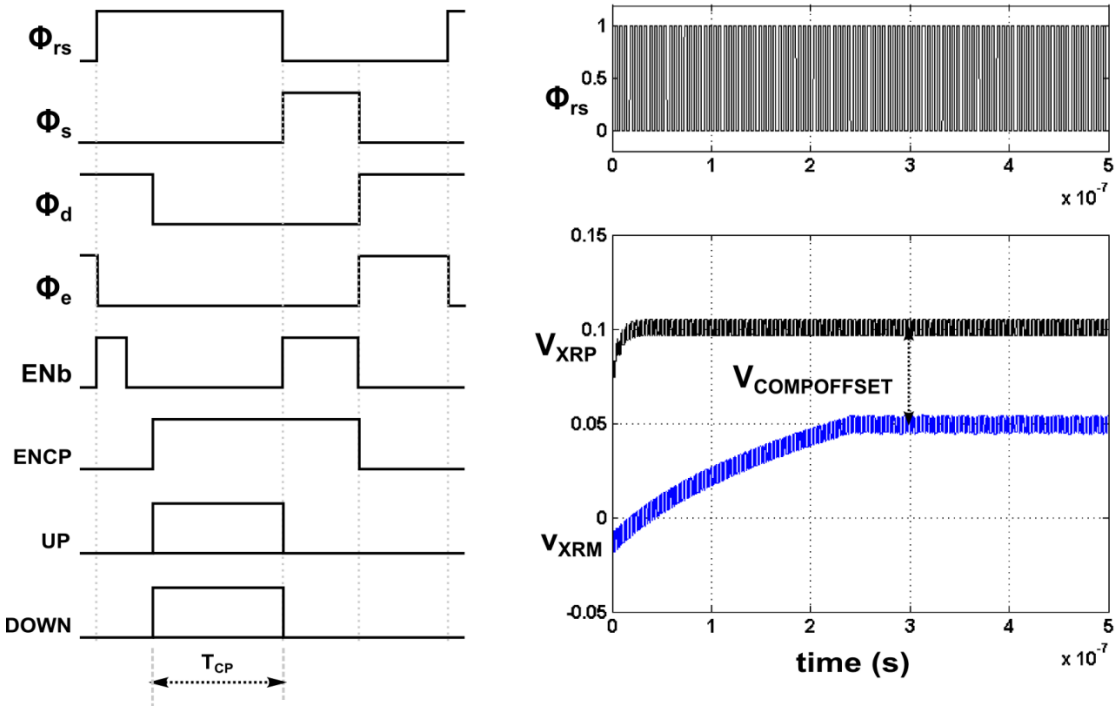
Figure 5-14: Simulated residue voltages of residue range background calibration with temperature swept from -40 C° to 125 C° and the power supply swept from 0.9 V to 1.1V with 10 MHz sinusoidal full swing input.

5.8 Sub-ADC Comparator

The offset of the comparator degrades the noise floor and DNL, especially in the final flash stage. To reduce this offset voltage, large devices can be used but this approach is not suitable for high speed operation due to the large parasitic capacitance. Another way to reduce offset is to use offset calibration with digital control by adding extra capacitance at the comparator outputs [28]. However, this also decreases the speed and the many digital registers per comparator occupy considerable silicon area. A self-calibrating technique [29] is introduced that does not impair speed but does require a special calibration mode. In this design, a discrete-time charge-pump based background calibration technique is used to adjust the comparator's offset every cycle. The comparator offset voltage calibration circuit is shown in Figure 5-15 with the corresponding timing diagram. It consists of a comparator with four inputs, two input sampling capacitors $C_{IN\pm}$, two reference precharge capacitors $C_{R\pm}$, a low pass filter capacitor C_{CP} for the charge pump, I_{CP} for the charge pump current, and enable switches.



(a)



(b) (c)

Figure 5-15: Comparator schematic with a corresponding timing diagram. (a) Schematic of comparator. (b) Timing diagram. (c) Simulated comparator offset calibration with 50mV forced offset voltage.

At the beginning of the reference sampling, ϕ_d goes high for a short time to short the input of the comparator for offset calibration. If the comparator has a positive offset voltage then the comparator output will be high. Likewise, if the comparator has a negative offset voltage then the comparator output will be low. The result of this comparison is used to update the offset calibration every clock cycle. Figure 5-14 (c) shows the simulated waveforms of the comparator offset calibration, where V_{XRP} and V_{XRM} converge to a $V_{COMPOFFSET}$ value of 50mV. This 50 mV corrects for a forced differential offset voltage of the opposite magnitude at the comparator input in the simulation. A calibration voltage V_{XRM} is applied to the inverting input of the auxiliary differential pair (V_{RM} in Figure 5-16). With the main input shorted, the voltage V_{XRM} is incremented by the charge pump if the comparator output is "1" and decremented if the comparator output is "0". After a several clock cycles, the voltage V_{XRM} converges to a value that cancels the comparator offset. The current I_{CP} in the charge pump is designed such that the voltage ripple on V_{RM} after convergence is much less than the sub-ADC's LSB.

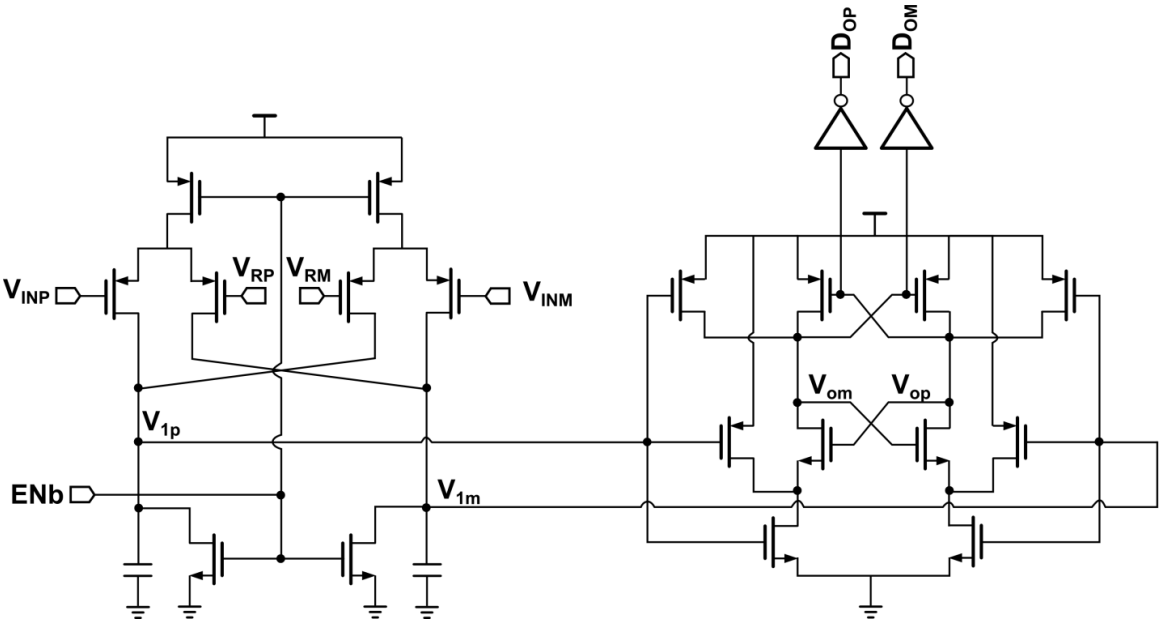


Figure 5-16: Schematic of dynamic comparator.

The sub-ADC comparator needs to be fast enough so as to have a minimal impact on the charge transfer phase time available to the MDAC. For fast operation, a two stage dynamic comparator is implemented as shown in Figure 5-16. The comparator consists of two input devices for the comparator input and two input devices for offset calibration. V_{1p} and V_{1m} nodes are discharged to V_{SS} during a reset and the second stage is also reset to $V_{DD,}$ at this time. When ENb goes low, the comparator enters the comparison phase which is controlled by two input pairs, then both V_{1p} and V_{1m} rise with different ramp rates depending on the difference of the input voltages. V_{1p} and V_{1m} rise up to V_{DD} because the pull down path is high impedance. Thus, the second stage regenerates very fast since the input pair has a full swing V_{GS} without a series enable switch on the source.

5.9 Zero-Crossing Detector

The ZCD senses the crossing of V_{x+} - V_{x-} in both the coarse phase and fine phase. At the end of the fine phase, the ZCD toggles E_2 which turns off the sampling switch in the following stage, thereby completing the charge transfer. Figure 5-16 shows a schematic of the ZCD. It is composed of a main pre-amplifier (M_{S1-2}, M_{P1-2}, M_{1-2}, M_{L1-L4}), a coarse threshold detector (M_{C1-2}, M_{CL1-2}), a fine threshold detector (M_{F1-2}, M_{FL1-2}), and simple digital logic to create the appropriate timing signals. PMOS input pairs are chosen in the preamplifier to accommodate a low input common-mode level.

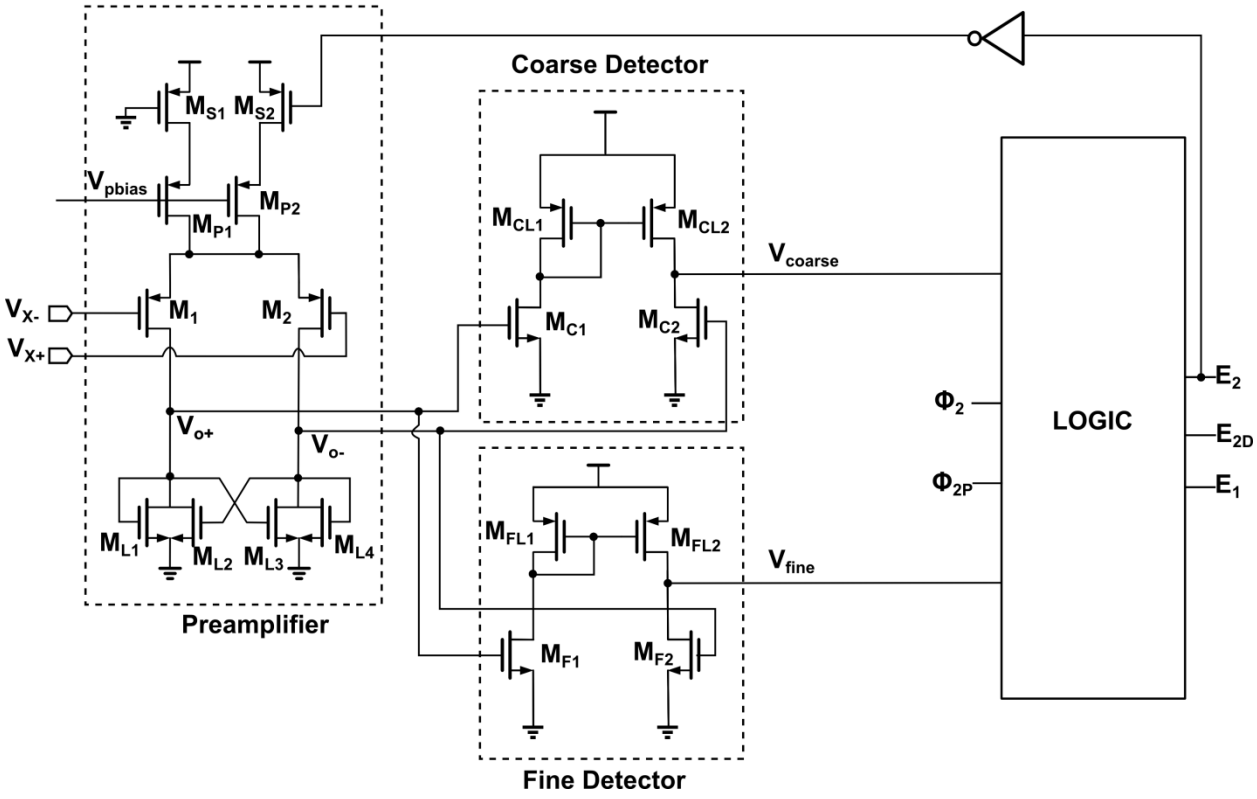


Figure 5-17: Schematic of zero-crossing detector.

To generate an undershoot voltage in the coarse phase to enable a uni-directional two-phase operation, an intentional offset is introduced between M_{CL1} and M_{CL2}. The coarse phase offset is set to ensure the coarse phase sufficiently undershoots regardless of process, voltage, and temperature corners. The noise of the ZCD is mainly determined by the preamplifier because the noise associated with the coarse and fine detectors are reduced by the preamplifier open-loop gain.

Due to the dynamic operation of the core ZCBC, the power consumption is proportional to the sampling rate [12], with the exception of the bias circuitry which consumes a small amount of static power. In the preamplifier, M_{S1} provides a small amount of bias current for a faster turn-on transient, while the larger M_{S2} only turns on during the coarse and fine phases. As soon as E_2 goes low, M_{S2} is turned off to save power. To reduce the power consumption at lower sampling frequencies, the ramp currents I_1 and I_2, as well as the ZCD bias current are designed to scale with the sampling clock frequency and track the primary current generated from a master bias control circuit.

5.10 Noise Contribution

Flicker and thermal noise from resistors and transistors are generated during the ZCBC ADC's operation. The current sources, switches, and ZCD all add noise to the system but the ZCD is the dominant noise source among them [41] - [42]. In a pipelined ADC, all noise can be calculated as input referred noise. To achieve the target signal to noise ratio, the sum of the noise power must be lower than the ratio given by

$$SNR = 10log(\frac{P_{signal}}{P_{noise}}) \tag{5.8}$$

This RMS signal power of a sinusoidal input is

$$V_{in,rms} = \frac{V_{p-p}}{2\sqrt{2}} \tag{5.9}$$

where $V_{p\text{-}p}$ is the peak-to-peak amplitude of the sinusoidal input.

The RMS quantization noise is

$$V_{q,rms} = \frac{1LSB}{\sqrt{12}} \tag{5.10}$$

The sampled RMS noise on a capacitor is

$$V_{sampling,rms} = \sqrt{\frac{kT}{C}} \tag{5.11}$$

The input referred noise of a ZCD is

$$V_{ZCD,rms} = \sqrt{\frac{\overline{V_{o,ZCD}^2}}{A_{ZCD}^2}} \tag{5.12}$$

where A_{ZCD} is the gain of the preamplifier and $V_{o,ZCD}^2$ is the integrated output noise power. This noise contribution is multiplied by the noise gain and then divided by the signal gain for the input referred noise in a pipelined ADC.

The ZCD input-referred noise contribution in the pipelined ADC stages is

$$P_{n,in} = \left(\frac{A_{NG}}{A_{sig}}\right)^2 P_{n,ZCD1} + \left(\frac{A_{NG}}{A_{sig}{}^2}\right)^2 P_{n,ZCD2} + \left(\frac{A_{NG}}{A_{sig}{}^3}\right)^2 P_{n,ZCD3} + \left(\frac{A_{NG}}{A_{sig}{}^4}\right)^2 P_{n,ZCD4} \tag{5.13}$$

where A_{NG} is the noise gain, A_{sig} is the signal gain, and $P_{n,ZCD1-4}$ is the input referred ZCD noise power of each stage.

Each stage's noise is scaled by a factor of $\frac{1}{A_{sig}{}^2}$, so the input referred noise of the 2nd through 4th stages is relatively small compared to the 1st stage.

6 Low Power Techniques with Dynamic Biasing ZCD

In a zero-crossing based ADCs, the ZCD consumes a large portion of the overall power in the pipelined ADC since noise contribution of ZCD is the most significant. To lower ZCD noise, some power must be spent to reduce noise level. In this chapter, we will describe a way to reduce ZCD power consumption further while keeping similar noise performance. Dynamic ZCDs that consume current only during the switching time to reduce power consumption have been published [10], [16]. However, the published dynamic ZCDs were not fully differential so accuracy and noise immunity were limited. In this chapter, we propose a fully differential dynamic biasing ZCD.

6.1 Dynamic Biasing on ZCD

The basic idea of a dynamic zero-crossing detector (DZCD) is to change the bias current dynamically depending on the input voltage. Low noise is only needed when the ZCD makes its final decision. Other portions of the charge transfer phase can be relaxed. For example, the coarse phase does not need low noise because the noise contribution is mainly related to fine decision. So, we can start with a small current in the coarse phase and gradually increase the bias current as the two input voltages get closer as shown in Figure 6-1. When the current reaches the maximum current, we can get a very fast fine decision. Once the zero crossing point is reached the bias current can be totally turned off.

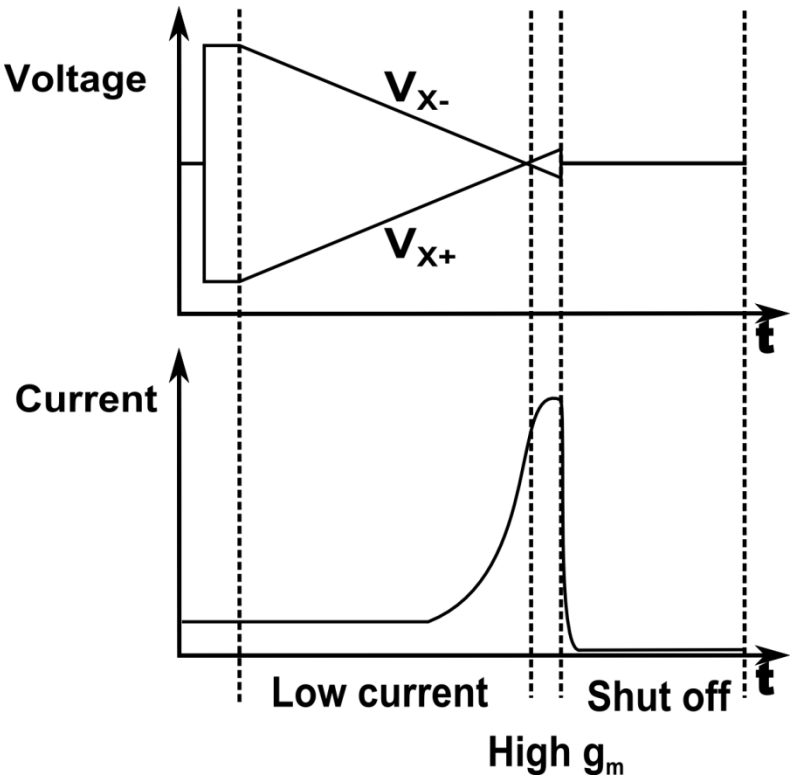


Figure 6-1: Current profile of dynamic ZCD.

6.2 Single Ended DZCD

The first single ended dynamic ZCD was reviewed in section 3-2. This design is very power efficient but ZCD's noise is very high due to the nature of the single ended architecture. The resolution was therefore limited to only 8bit. This dynamic ZCD consists of a NMOS and a PMOS transistor as shown in Figure 6-2. The preset pulse pushes the virtual ground node voltage V_x down to turn off the NMOS. Simultaneously, $\overline{\Phi_1}$ turns on M_2 to pre-charge the voltage V_p high and turn on the sampling switch in the next stage. When $\overline{\Phi_1}$ drops, node V_p is left floating high to keep the sampling switch on, and the output voltage begins to ramp. As V_x ramps up it

will give the NMOS sufficient gate drive at some point to start pulling down the floating V_p node. When V_p is pulled down sufficiently to turn off the sampling switch, the voltage on the load capacitor is sampled and the charge transfer is complete. One significant limitation of this ZCD relates to the inherently single-ended topology which does not have a natural differential extension. Thus, depending on the amount of power supply and substrate noise present in a particular system, this architecture is not suitable for high resolution applications [10].

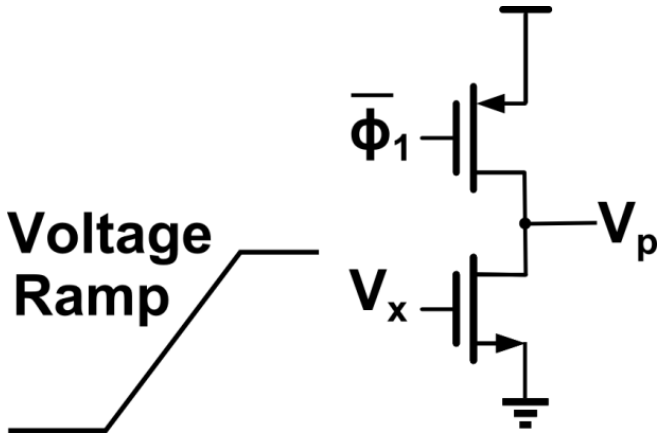


Figure 6-2: Dynamic inverter as a ZCD.

6.3 Pseudo Differential DZCD

Figure 6-3 shows a differential DZCD that was used in the split CLS technique. It consists of a reference current, coupling capacitor to the gate of the tail current source, and preamplifier stage. The ZCD in a differential ZCBC system is statically biased while the current sources ramp the output. However, if the power consumption of the ZCD is redistributed to concentrate the use of current around the detection instant, then power efficiency can be optimized and the static power can be minimized. Figure 6-4 shows the operation of the dynamic ZCD. Initially during ϕ_{PC}, the tail transistor M_1's gate node is charged via switch M_3 to a static bias. On the falling edge of ϕ_{PC}, V_b is disconnected from this reference and left at a fixed but floating voltage. The inputs are still relatively far apart, and if the gain of the ZCD is sufficiently large, the outputs V_{o+} and V_{o-} are saturated at the maximum value of the ZCD's output swing. Node V_{o-} will remain close to V_{SS} in this saturated state.

At this point the voltage at V_{o-} will begin to rise and, via the feedback capacitor C_{FB}, the floating node V_b will also rise by some proportional amount, increasing the tail current by some proportional amount. Around the detection instant, the g_m of the ZCD is at a maximum. Once the ZCD decision is registered by the dynamic latch at the output of V_{o+}, switch M_2 connects V_b to V_{ss} and shuts off the ZCD. The floating gate of M_1 makes the dynamic ZCD sensitive to external transient variations [16].

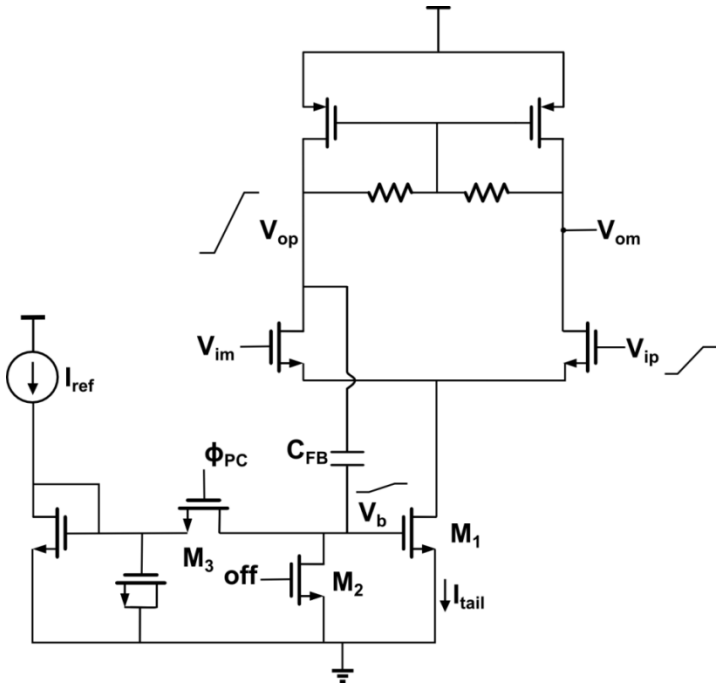


Figure 6-3: Pseudo Differential dynamic ZCD.

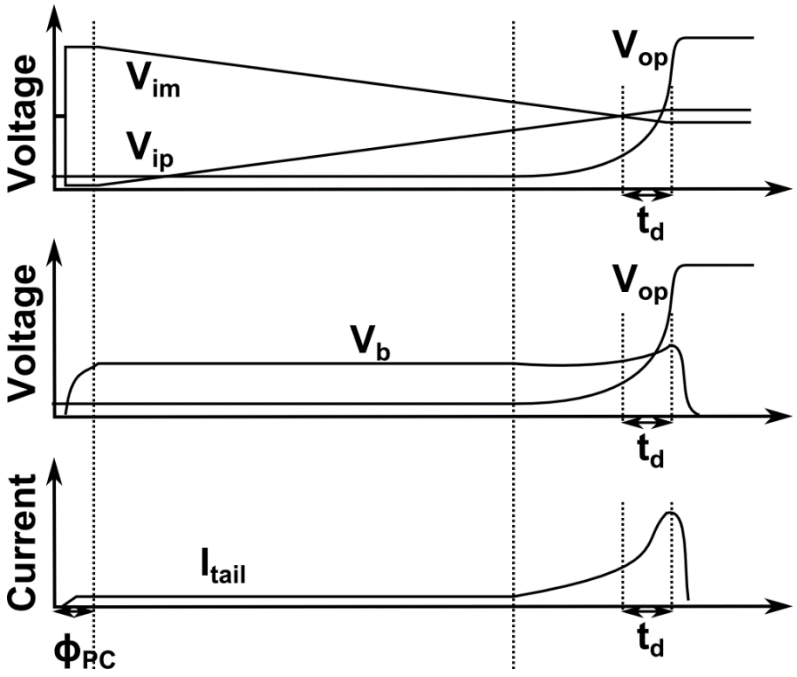


Figure 6-4: Waveforms of pseudo differential dynamic ZCD.

6.4 Proposed Differential DZCD

In order to change the bias current dynamically, a dynamic biasing block controls the tail current source of the preamplifier as shown in Figure 6-5. DZCD consists of a dynamic biasing block, preamplifier, coarse detector, and fine detector. Separate signal paths are optimized with each specific requirement. The dynamic biasing block does not need to have low noise. The current is relaxed and its size is not big but it must be very fast to immediately respond to changes in the input waveforms. The coarse detector implemented for the ADCs described in this dissertation, uses a differential to single converter.

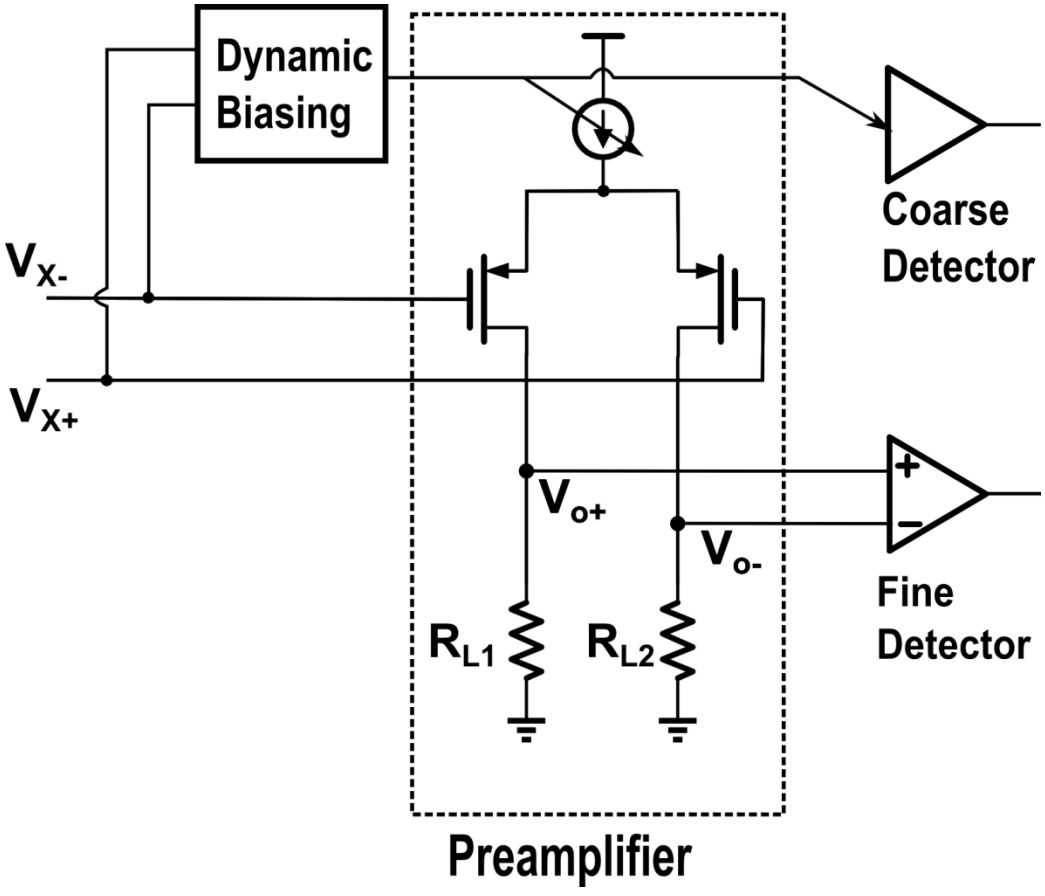


Figure 6-5: Block diagram of dynamic ZCD.

6.5 ZCD Time Domain Response

6.5.1 Dynamic Biasing ZCD

A DZCD changes bias current depending on the amplitude of the differential input voltage. Defining transconductance of the dynamic biasing block as G_{md} then the bias current with ramp input is

$$I_d = RtG_{md} \tag{6.1}$$

where R is the input ramp rate, t is time.

A preamplifier's transconductance in strong inversion is

$$G_m = \sqrt{2\beta I_d} = \sqrt{2\beta RtG_{md}} \tag{6.2}$$

Where β is $\mu C_{ox}\frac{W}{L}$.

Because the preamplifier works as an integrator for large signals, the integrated voltage with ramp input is

$$\begin{aligned} V_o &= \frac{1}{C_p}\int_0^t I_d dt \\ &= \frac{1}{C_p}\int_0^t V_R G_m dt = \frac{1}{C_p}\int_0^t V_R\sqrt{2\beta RtG_{md}}dt \\ &= \frac{1}{C_p}\int_0^t Rt\sqrt{2\beta RtG_{md}}dt = \frac{\sqrt{2\beta G_{md}}}{C_p}\int_0^t (Rt)^{\frac{3}{2}}dt \\ &= \frac{\sqrt{2\beta R^3 G_{md}}}{C_p}\frac{2t^{\frac{5}{2}}}{5} = \frac{\sqrt{8\beta R^3 G_{md}t^5}}{5C_p} \end{aligned} \tag{6.3}$$

where V_R is input ramp voltage.

If the zero crossing detector's trip voltage is V_{trip}, then the ZCD delay is

$$t_d = \sqrt[5]{\frac{\left(5C_pV_{trip}\right)^2}{8\beta R^3 G_{md}}} \tag{6.4}$$

The overshoot voltage is the product of the input ramp rate R and the comparator delay t_d and is given by

$$V_{ov} = Rt_d = R\sqrt[5]{\frac{\left(5C_pV_{trip}\right)^2}{8\beta R^3 G_{md}}} = \sqrt[5]{\frac{\left(5C_pV_{trip}R\right)^2}{8\beta G_{md}}} = \sqrt[5]{\frac{\left(5C_pV_{trip}\frac{I_O}{C_t}\right)^2}{8\beta G_{md}}} \tag{6.5}$$

Current variation and parasitic nonlinear capacitance variation changes the ramp rate and this also changes the ZCD delay. The overshoot variation is

$$\begin{aligned}\Delta V_{ov} &= \frac{\partial V_{ov}}{\partial i}\Delta i + \frac{\partial V_{ov}}{\partial C_t}\Delta C_t \\ &= \sqrt[5]{\frac{\left(5C_pV_{trip}\frac{1}{C_t}\right)^2}{8\beta G_{md}}}\frac{2}{5}i^{-\frac{3}{5}}\Delta i + \sqrt[5]{\frac{\left(5C_pV_{trip}i\right)^2}{8\beta G_{md}}}\left(-\frac{2}{5}{C_t}^{-\frac{7}{5}}\right)\Delta C_t\end{aligned} \tag{6.6}$$

Because of this sensitivity, performance can be degraded if the current is data dependent at the zero crossing instant.

6.5.2 Constant Bias ZCD

If the bias current is constant then it can be analyzed in steady state.

The ramp input is

$$x(t) = \begin{cases} Rt, & 0 < t < \infty \\ 0, & x \geq 0 \end{cases} \tag{6.7}$$

$$X(s) = \mathcal{L}[x(t)] = R\int_0^\infty te^{-st}\,dt \tag{6.8}$$

$$X(s) = \frac{R}{s^2} \tag{6.9}$$

where *R* is the slope of the input ramp. *x(t)* shows a linear ramp input voltage with constant slope of *R*. *X(s)* is the Laplace transform of *x(t)*.

Assuming the dynamics of the zero-crossing detector is a single pole response, then the response is

$$H(s) = \frac{A}{\left(1+\frac{s}{\omega_0}\right)} \tag{6.10}$$

where *A* is DC gain and ω_0 is a pole location.

Thus, the output is

$$Y(s) = X(s)H(s)$$

$$\begin{aligned} &= \frac{R}{s^2} \cdot \frac{A}{\left(1+\frac{s}{\omega_0}\right)} \\ &= \frac{k_1}{s^2} + \frac{k_2}{s} + \frac{k_3}{\left(1+\frac{s}{\omega_0}\right)} \end{aligned} \tag{6.11}$$

$$RA = k_1 + s\left(\frac{k_1}{\omega_0} + k_2\right) + s^2\left(\frac{k_2}{\omega_0} + k_3\right) \tag{6.12}$$

$$k_1 = RA$$
$$k_2 = -\frac{RA}{\omega_0}$$
$$k_3 = \frac{RA}{{\omega_0}^2}$$
$$Y(s) = \frac{RA}{s^2} + \frac{-\frac{RA}{\omega_0}}{s} + \frac{\frac{RA}{{\omega_0}^2}}{\left(1 + \frac{s}{\omega_0}\right)}$$
$$= \frac{RA}{s^2} + \frac{-\frac{RA}{\omega_0}}{s} + \frac{\frac{RA}{\omega_0}}{(\omega_0 + s)} \tag{6.13}$$

Then, we take the inverse Laplace transform to get the time domain response

$$y(t) = RAtu(t) - \frac{RA}{\omega_0}u(t) + \frac{RA}{\omega_0}e^{-\omega_0 t}u(t) = RA\left(t - \frac{1}{\omega_0} + \frac{1}{\omega_0}e^{-\omega_0 t}\right)u(t) \tag{6.14}$$

Here, ω_0 is a function of current and g_m. If the trip voltage is V_{trip}, then the time when the input crosses this trip voltage is given by

$$T_1 = \frac{V_{trip}}{R} \tag{6.15}$$

The time T_2 when the output crosses the trip voltage is

$$V_{trip} = RA\left(T_2 - \frac{1}{\omega_0} + \frac{1}{\omega_0}e^{-\omega_0 T_2}\right) \tag{6.16}$$

$$\frac{V_{trip}}{RA} = \left(T_2 - \frac{1}{\omega_0} + \frac{1}{\omega_0}e^{-\omega_0 T_2}\right) \tag{6.17}$$

The delay of the zero-crossing detector is $t_d = T_2 - T_1$ and can be found by solving equation 6.15 and 6.17.

6.6 DZCD Implementation

Figure 6-6 shows the schematic of the DZCD implementation. It consists of a dynamic biasing block, preamplifier, coarse detector, fine detector, and a combinational logic that generates proper signals for the current sources and following stage's sampling switch. The dynamic bias block is also the input of the coarse detector.

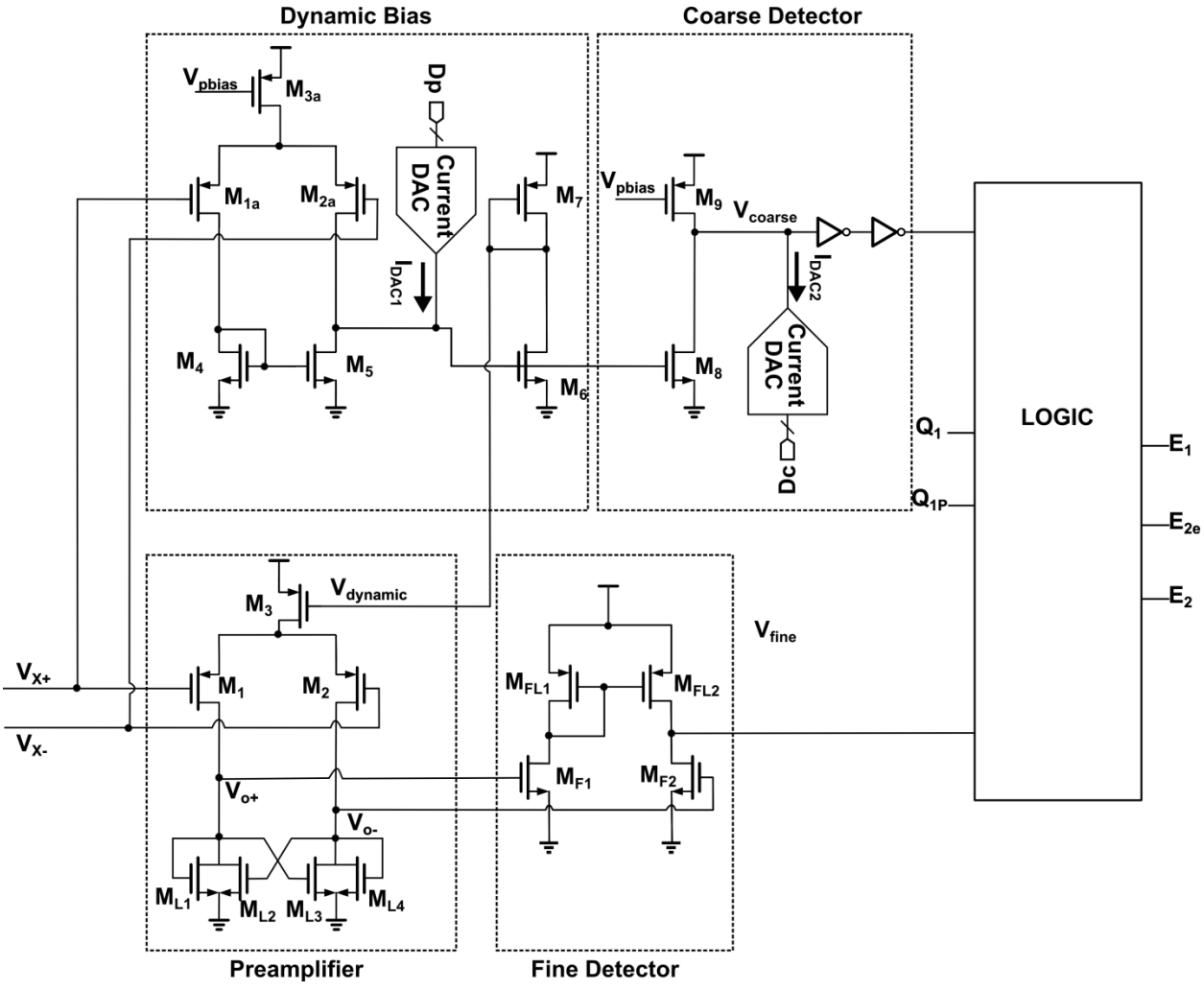


Figure 6-6: Schematic of dynamic ZCD.

6.6.1 Dynamic Biasing Circuit

The dynamic biasing circuit generates bias voltages for the preamplifier of the ZCD which depend on the input ramp. When the differential voltage is smaller, the DZCD needs to generate a bigger tail current for the preamplifier. Figure 6-7 shows the dynamic biasing circuit and preamplifier. The dynamic biasing circuit consists of a differential amplifier $M_{1a,2a,4,5}$, current DAC I_{DAC1} and common source amplifier with diode connected PMOS load M_7.

The tail current in the preamplifier is

$$I_{d5} = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_5\left(V_{gs5} - V_{th}\right)^2(1 + \lambda V_{ds5}) = \frac{I_{d3a}}{2} + I_{d2a} + I_{DAC1} \tag{6.18}$$

$$I_{d4} = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_4\left(V_{gs4} - V_{th}\right)^2\left(1 + \lambda V_{gs4}\right) = \frac{I_{d3a}}{2} - I_{d2a} \tag{6.19}$$

If we ignore channel length modulation on I_{D4} to simplify this equation,

$$V_{gs4} = \sqrt{\frac{\frac{I_{d3a}}{2} - I_{d2a}}{\frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_4}} + V_{th} \tag{6.20}$$

$$V_{gs6} = V_{ds5} = \left(\frac{\frac{I_{d3a}}{2} + I_{d2a} + I_{DAC1}}{\frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_5\left(V_{gs5} - V_{th}\right)^2} - 1\right)\frac{1}{\lambda} \tag{6.21}$$

$$V_{gs5} = V_{gs4} = \sqrt{\frac{\frac{I_{d3a}}{2} - I_{d2a}}{\frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_4}} + V_{th} \tag{6.22}$$

$$I_{d6} = I_{d7} = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_6\left(V_{gs6} - V_{th}\right)^2$$

$$= \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_6\left(\left(\frac{\frac{I_{d3a}}{2}+I_{d2a}+I_{DAC1}}{\frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_5\left(V_{gs5}-V_{th}\right)^2} - 1\right)\frac{1}{\lambda} - V_{th}\right)^2 \quad \textbf{(6.23)}$$

$$I_{tail} = I_{d3} = I_{d7}\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_7} = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_6\left(\left(\frac{\frac{I_{d3a}}{2}+I_{d2a}+I_{DAC1}}{\frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_5\frac{\frac{I_{d3a}}{2}-I_{d2a}}{\frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_4}} - 1\right)\frac{1}{\lambda} - V_{th}\right)^2\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_7} \quad (6.24)$$

If we make M_4 equal to M_5 then,

$$I_{tail} = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_6\left(\left(\frac{\frac{I_{d3a}}{2}+I_{d2a}+I_{DAC1}}{\frac{I_{d3a}}{2}-I_{d2a}} - 1\right)\frac{1}{\lambda} - V_{th}\right)^2\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_7} \quad (6.25)$$

Note that I_{d2a} approaches $\frac{I_{d3a}}{2}$ when V_{x-} approaches V_{x+}, which means the denominator becomes closer to zero. Thus, I_{tail} increases rapidly when ZCD inputs get closer to the zero-crossing. This can be intuitively understood as follows. As V_{x+} - V_{x-} get closer to zero, M_{2a} adds more current on M_5's drain so V_{gs} of M_6 increases and then current of M_6 is mirrored to M_3 with the ratio of M_3 over M_7.

Figure 6-8 shows simulated current profile on I_{d3} and $V_{dynamic}$ with V_{x+} and V_{x-}. The tail current of preamplifier rapidly increases as ZCD approaches zero-crossing. I_{DAC1} current controls the initial biasing voltage on $V_{dynamic}$ and magnitude of I_{d3} as shown in Figure 6-9. The nature of this dynamic biasing changes g_m, noise, and bandwidth. Because I_{tail} is very small initially, the preamplifier starts in weak inversion, then it enters into strong inversion.

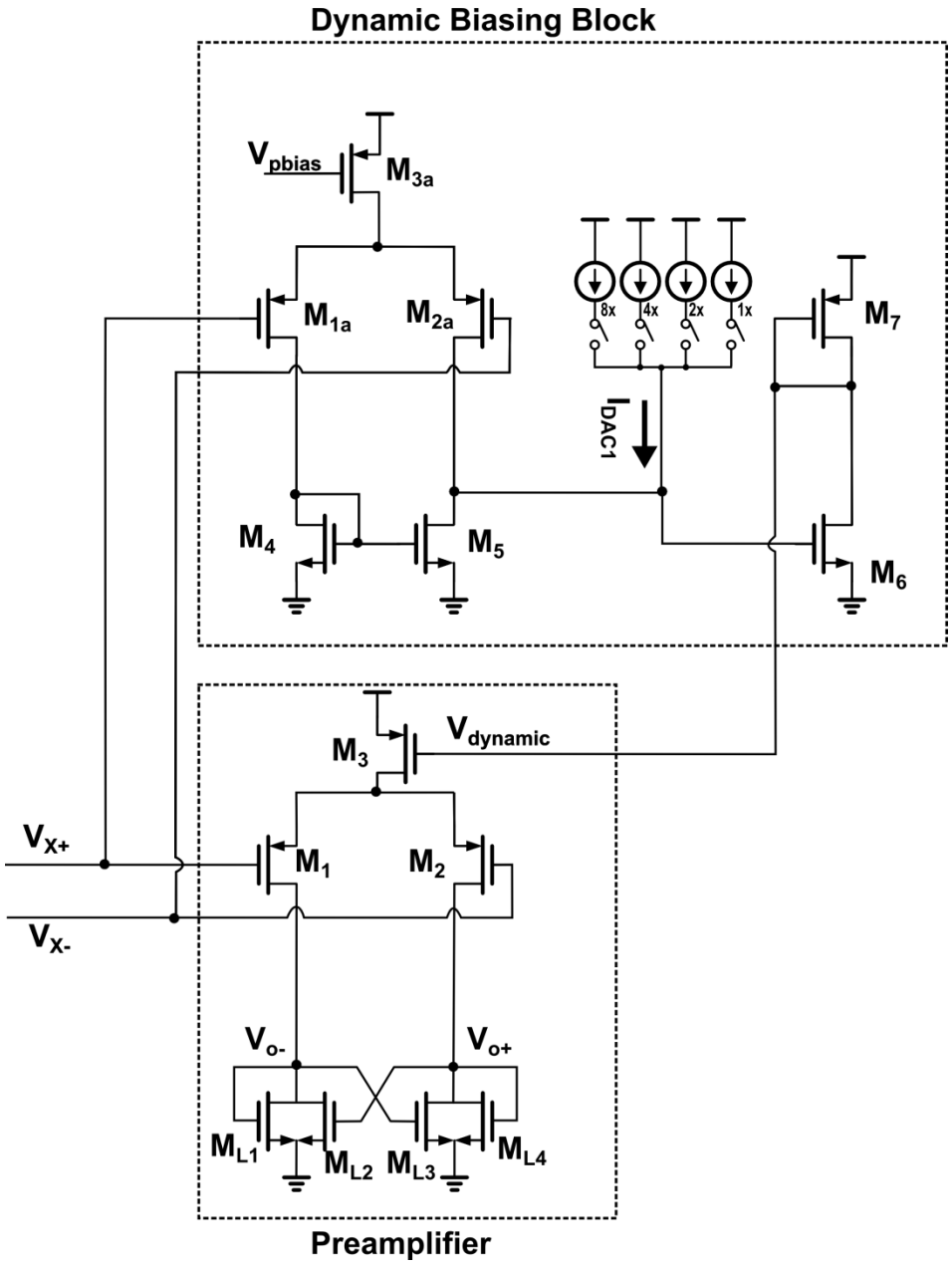


Figure 6-7: Schematic of dynamic biasing block and preamplifier.

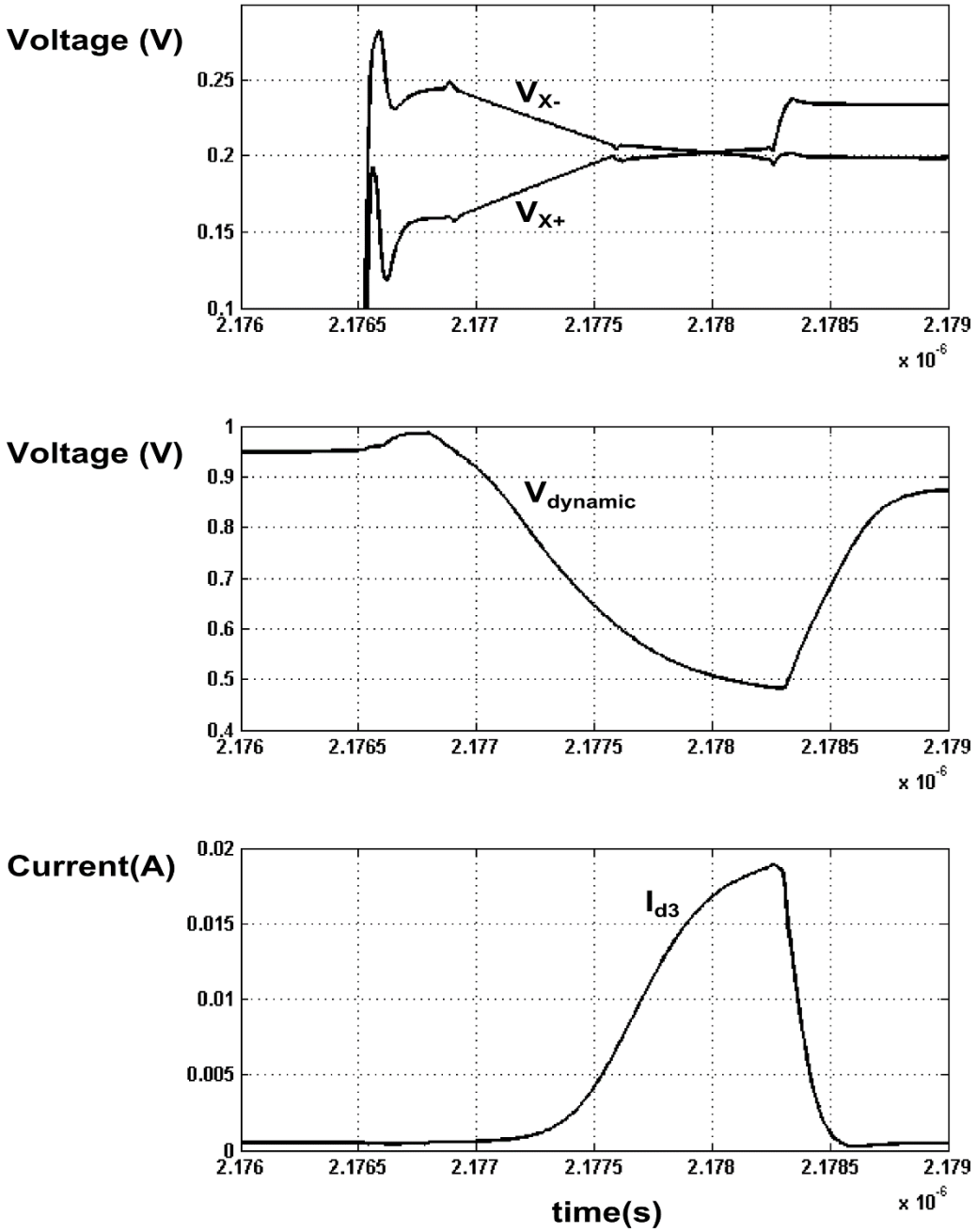


Figure 6-8: Dynamic biasing waveforms.

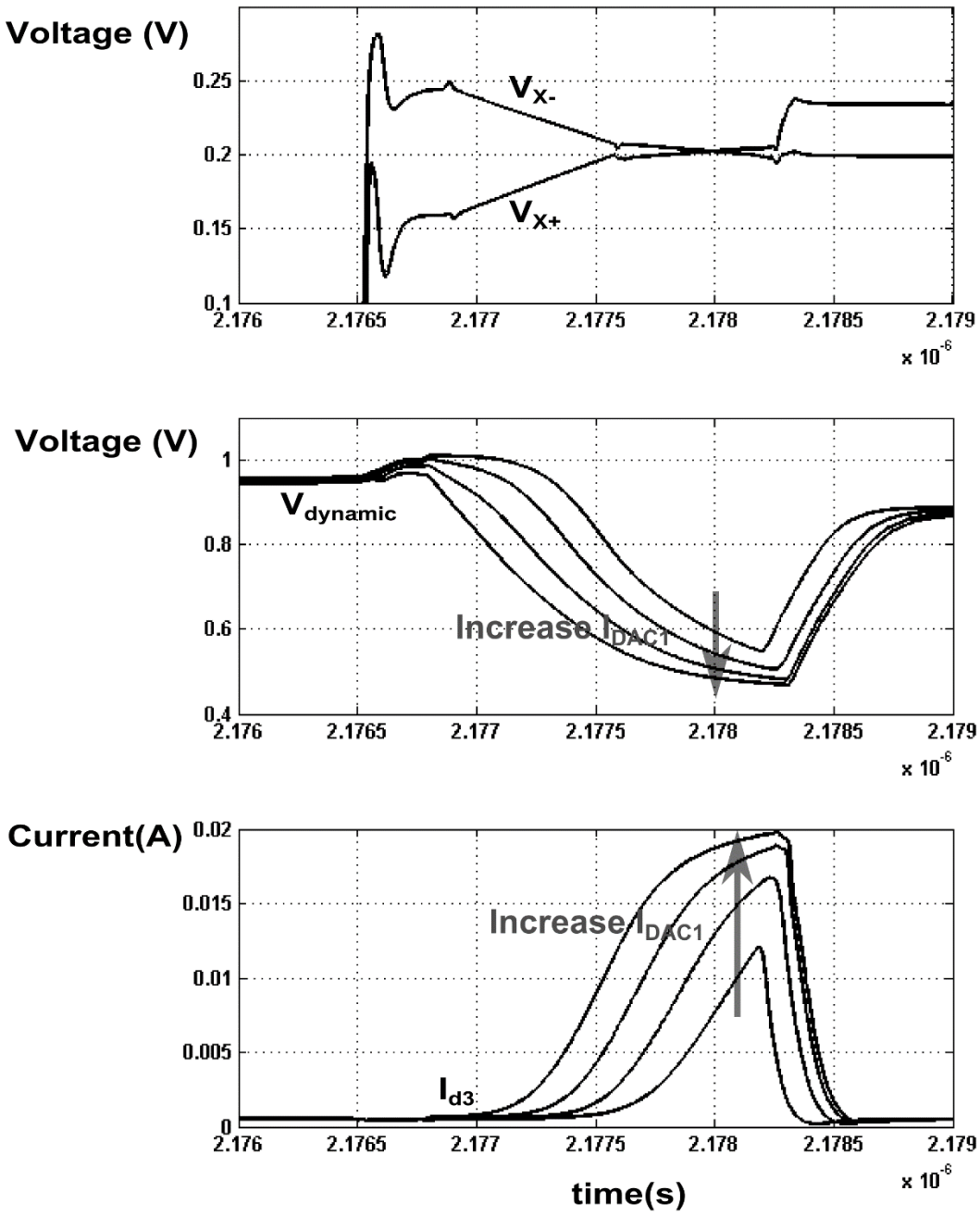


Figure 6-9: Dynamic biasing waveforms with I_{DAC1} swept.

6.6.2 Coarse Detector

For the coarse phase, a single ended inverter is used for the fast coarse decision as shown in Figure 6-10. The trip point is controlled by a current DAC. I_{DAC2} changes the logic threshold of the inverter.

$$I_{d8} = I_{d9} - I_{DAC2} \tag{6.26}$$

When the inverter makes a transition, all of the MOS transistors are in a saturation region. So the transfer function of the inverter is

$$I_{d8} = \frac{1}{2}\mu C_{ox}\frac{W_{m8}}{L_{m8}}(V_{in} - V_t)^2(1 + \lambda V_{coarse}) \tag{6.27}$$

With equation 6.26 and equation 6.27, V_{coarse} in Figure 6-10 is

$$V_{coarse} = \left(\frac{(I_{d9} - I_{DAC2})}{\frac{1}{2}\mu C_{ox}\frac{W_{m8}}{L_{m8}}(V_{in} - V_t)^2} - 1\right)\frac{1}{\lambda} \tag{6.28}$$

By changing I_{DAC2} the inverter's trip point can be easily changed. Figure 6-11 shows the simulated trip voltage variation as I_{DAC2} increases.

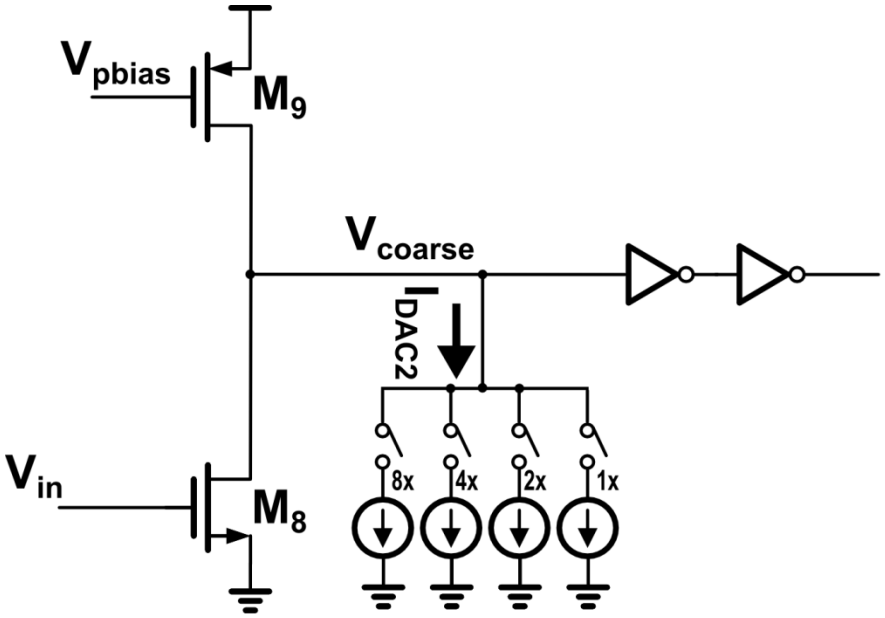


Figure 6-10: Schematic of coarse detector.

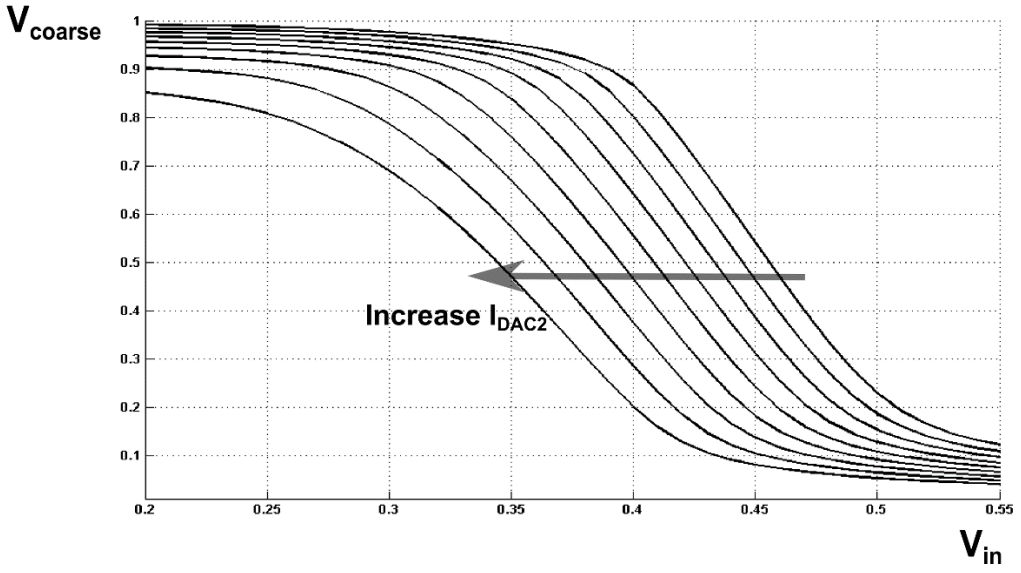


Figure 6-11: Waveform of coarse detector with I_{DAC2} swept.

6.6.3 Fine detector

Figure 6-12 shows the fine detector schematic with preamplifier which is similar to the constant bias ZCD discussed in chapter 5. $M_{F1,F2}$ are scaled to the size of $M_{L1,L4}$ to reduce power consumption since the second stage of ZCD noise contribution is smaller than the first stage. Assuming no channel length modulation the differential preamplifier gain is

$$A_v = g_{m1,m2} \frac{1}{g_{mL1,L4} - g_{mL2,L3}} \tag{6.29}$$

At the beginning of charge transfer, the preamplifier's tail current is very low so both of the input devices are in weak inversion. As the tail current source increases $M_{1,2}$ enter strong inversion where the g_m is described by,

$$g_{m1,m2} = \sqrt{2\mu C_{ox} \frac{W}{L} \frac{I_{d3}}{2}} \tag{6.30}$$

The bandwidth of these devices is

$$\omega_0 = \frac{g_{m1,2}}{C_p} \tag{6.31}$$

where C_p is the parasitic capacitance at the preamplifier's output.

Once the fine detector changes V_{fine}, this signal becomes the rail-to-rail swing of the digital signal followed by inverters which turn off the next stage's sampling switch.

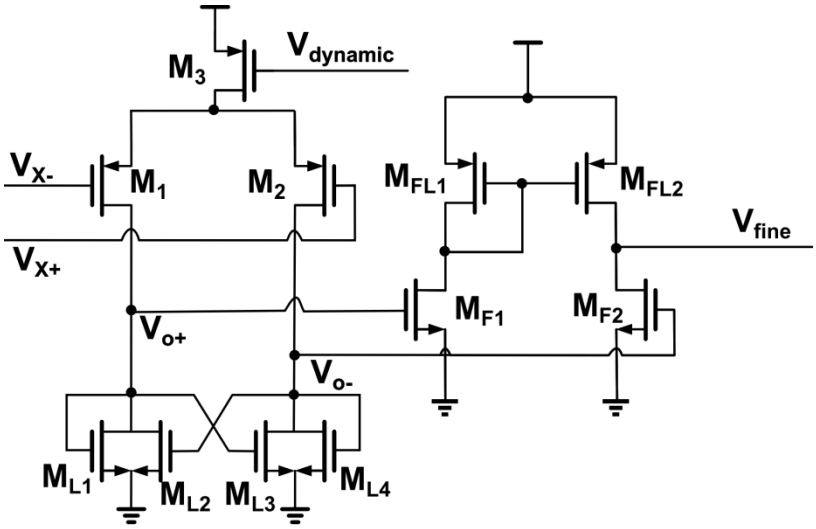


Figure 6-12: Schematic of fine detector with preamplifier.

6.7 DZCD Performance

The performance mainly depends on how good the DZCD delay variation is. This delay variation in turn depends on current variation. Any variation on the ZCD becomes a source of ADC nonlinearity. During the design process, the delay variation of the ZCD is evaluated with a Verilоga monitoring block. The dynamic biasing block and preamplifier's tail current source is optimized with this process. Having a maximum current at zero crossing is important in order to maximize power efficiency. If this current is too small then the g_m is not big enough for a given speed since g_m dominates bandwidth and noise performance of ZCD. If it is too big then the DZCD is not power efficient.

6.8 Noise Contribution

The tail current source contributes negligible noise if the differential input signal is zero, and the circuit is symmetric, in which case the noise in the tail current source divides equally between

input devices, producing only a common-mode noise voltage at the output [40]. The most significant source of noise for this circuit is the DZCD. Noise from the DZCD causes timing jitter which creates uncertainty when the sampling switch opens. Device $M_{1,2}$ of the DZCD in Figure 6-11 contributes most significantly to this source of noise. The input referred noise of the ZCD has been solved in [41, Eq. 5.20] and the result is

$$\sigma_v{}^2 = \frac{N}{4\tau}\left(\frac{1+e^{-\frac{T_c}{\tau}}}{1-e^{-\frac{T_c}{\tau}}}\right) = \frac{N}{4\tau}\coth\left(\frac{T_c}{2\tau}\right) \tag{6.32}$$

where N is the noise spectral density, T_c is the deterministic time when the input crosses zero, and τ is the time constant.

7 Experimental Prototypes and Measurement Results

The prototype ZCBC pipelined ADCs based on the above architectures were fabricated in a 55nm, six-metal, single-poly digital CMOS technology. This chapter discusses the test setup and measurement results of ZCBC pipelined ADCs, with both the constant bias ZCD and dynamic bias ZCD.

7.1 Die Photographs

Die photographs of the prototype constant bias and dynamic bias ZCD ADC are shown in Figures 7-1 and 7-2 respectively. The prototype's ADC cores are the same size, of 367µm x 767µm. Both of the ADCs have the same building blocks except for the ZCD.

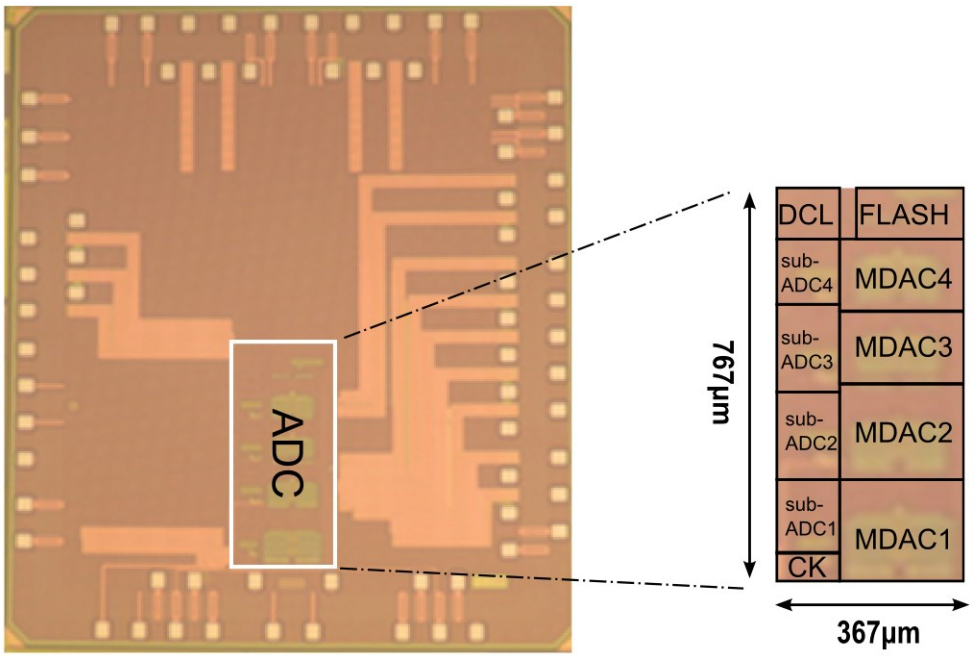


Figure 7-1: The die photo of ZCBC ADC with constant bias ZCD.

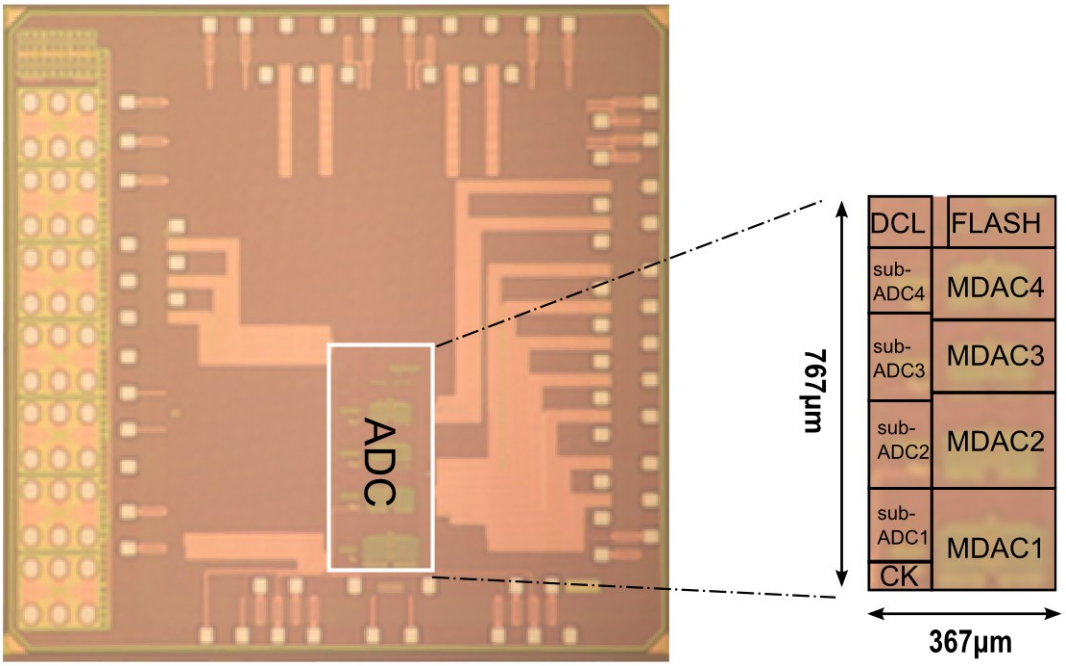


Figure 7-2: The die photo of ZCBC ADC with dynamic bias ZCD.

7.2 Test Environment

The ADC was tested by supplying a sinusoidal input source and clock signals while capturing the digital output data with a logic analyzer. The analog input is provided by an RF signal generator, bandpass filtered, and then converted from single ended to differential signal using an RF transformer whose secondary is terminated by 50 Ohms. To get better jitter performance and better clock duty cycle, 2 times larger clock frequency was supplied from an RF signal generator and then divided by 2 on chip.

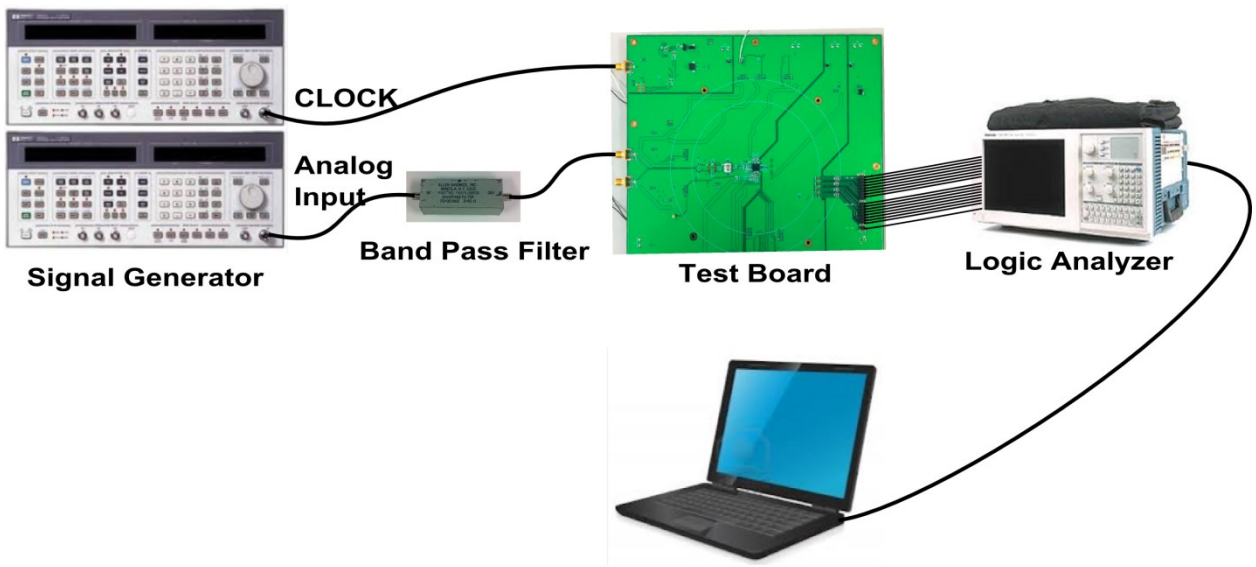


Figure 7-3: ADC test setup.

The clock signal is converted from single ended to differential with an RF transformer. The ADC output is captured with a logic analyzer and the dynamic and static performance was analyzed with MATLAB as shown if Figure 7-3. The ADC output was decimated by 16x to simplify the output setup. The chips were packaged in a QFN (quad flat no lead) 48 with an exposed paddle and soldered to the printed circuit boards. The two signal generators for signal input and clock were synchronized with a 10 MHz reference source.

7.3 Measured Results

A code density test was used to measure the differential nonlinearity (DNL) and integral nonlinearity (INL). The dynamic linearity of the ADC was characterized by applying a Fast Fourier transform (FFT) to the digital output codes with a single-tone input.

The Walden's figure of merit (FOM) is defined [43].

$$F = \frac{2^{SNRbits} f_{samp}}{P_{diss}} \tag{7.1}$$

$$SNRbits = \frac{SNR-1.76}{6.02} \tag{7.2}$$

where P_{diss} is power dissipation and f_{samp} is sampling frequency. Similar FOMs have been widely used in recent ADC's for comparison with effective number of bit (ENOB).

$$FOM_1 = \frac{P}{2^{ENOB} f_s} \tag{7.3}$$

$$FOM_2 = \frac{P}{2 f_{in} 2^{ENOB}} \tag{7.4}$$

$$ENOB = \frac{SNDR-1.76}{6.02} \tag{7.5}$$

where *SNDR* is signal-to-noise and distortion ratio, f_s is sampling frequency, and f_{in} is input frequency. In this measurement comparison, FOM_1 is used.

7.3.1 ADC With Constant Bias ZCD

Figure 7-4 shows the output spectrum when sampling a 10.1 MHz sinusoidal input at 200 MS/s. The measured peak SNDR reaches 64.6 dB, equivalent to 10.44 ENOB. Under the same condition, the peak spurious free dynamic range (SFDR) is 82.9 dBc. In Figure 7-5 and Figure 7-6, DNL and INL versus input code are plotted. The magnitude of the maximum DNL and INL are +0.24/-0.28 LSB and +1.36/-1.89 LSB, respectively. Table 7-1 summarizes measurements of the ADC with constant bias ZCD.

To achieve optimal power consumption vs. sampling frequency, the primary current generated from a master bias control circuit is designed to scale with the sampling clock frequency. Since the ramp currents I_1 and I_2 track the master bias current, at lower sampling rates the ramp rate is reduced to take advantage of the increased time available for the charge transfer. As the sampling rate is increased, the variation in time of the second phase zero crossings becomes a larger and larger fraction of the overall half clock period. Eventually, this leads to a higher percentage of zero-crossings failing to occur within the time provided by a half clock period, and the accuracy is significantly reduced as seen Figure 7-7. Conversely, at low sampling rate the SNDR is limited by the noise. Note the SNDR is almost flat up to 250 MS/s before degrading gradually. The SNDR is 62.9 dB at 250 MS/s. The power consumption is approximately proportional to the sampling frequency. The SNDR remains above 50 dB even at 300 MS/s sampling rate.

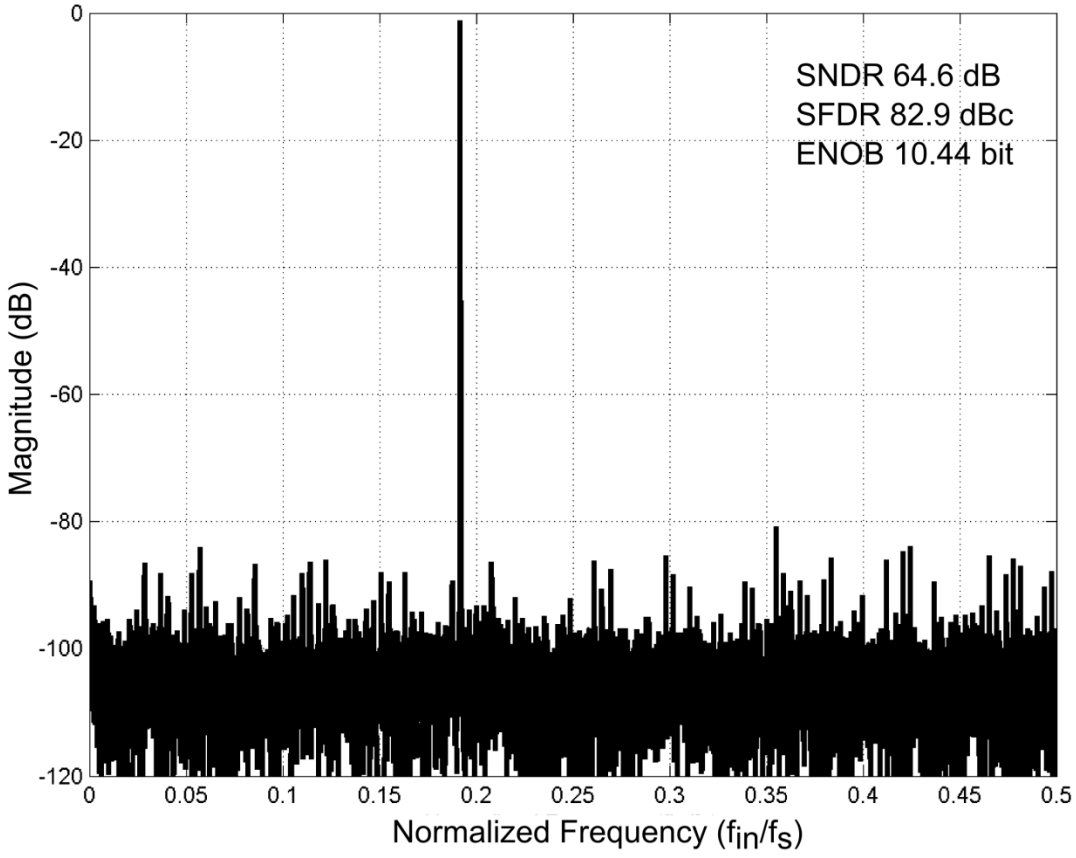


Figure 7-4: ADC digital output spectrum with a constant bias ZCD when sampling a 10.1 MHz sinusoidal input at 200 MS/s (output decimated by 16x).

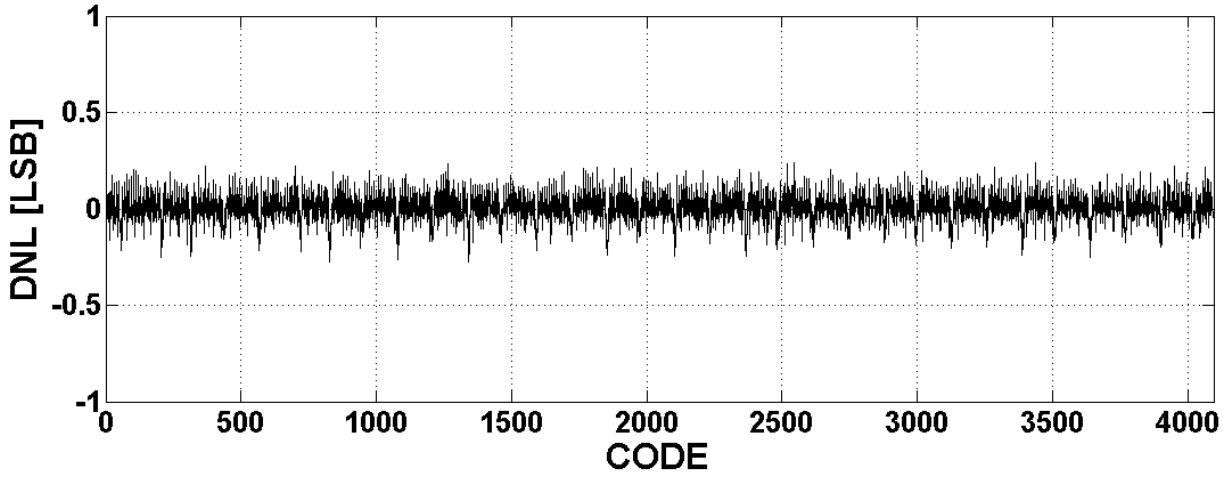


Figure 7-5: DNL of ADC with constant bias ZCD.

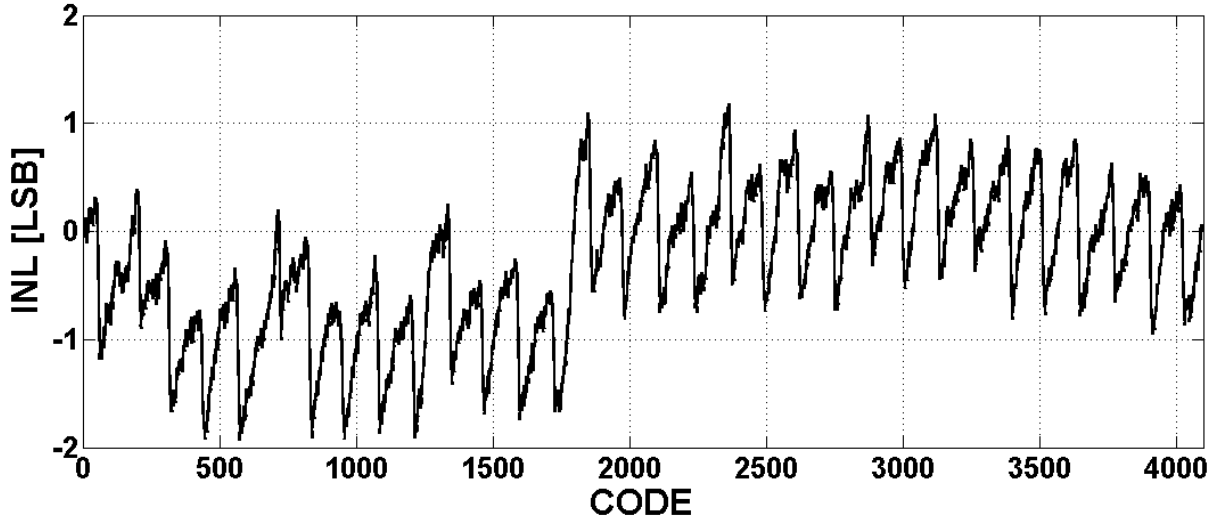


Figure 7-6: INL of ADC with constant bias ZCD.

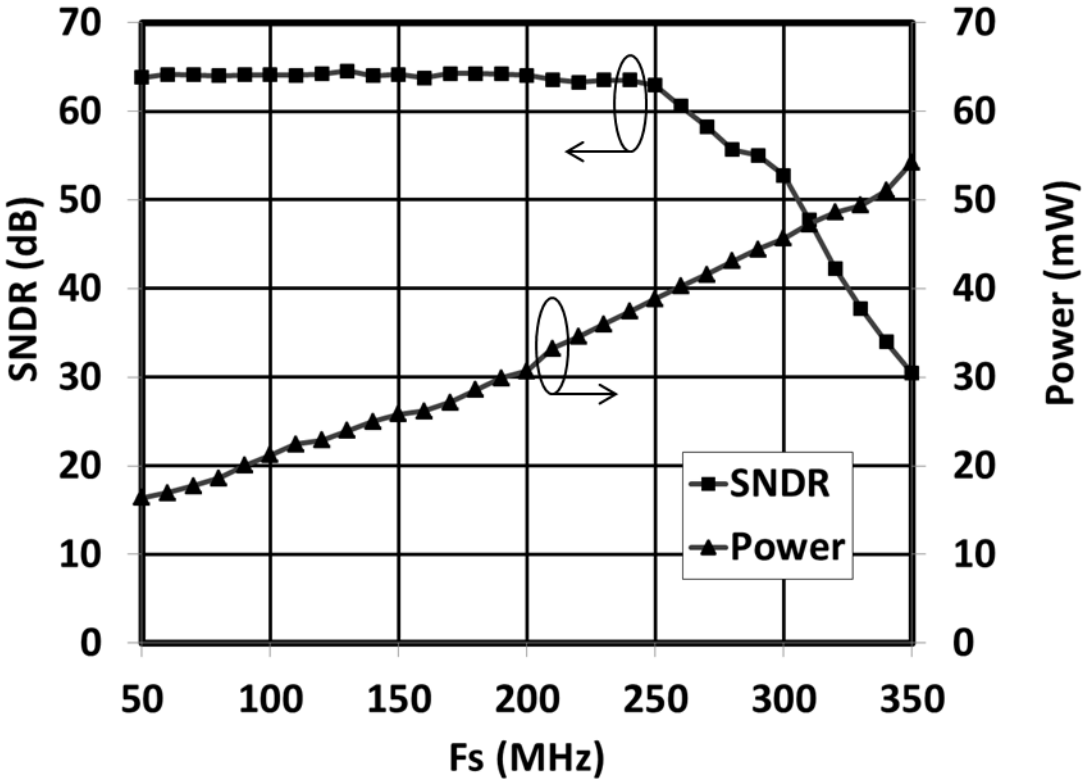


Figure 7-7: SNDR, Power versus sampling frequency with constant bias ZCD.

Table 7-1: Performance summary of ADC with constant bias ZCD

Technology	55nm CMOS 1-Poly 6-Metal
Supply voltage	1.1 V
Resolution	12 b
Conversion rate	200 MS/s
Input voltage Range	2 Vp-p (differential)
Die area	0.282 mm^2
Power consumption	30.7 mW
DNL	+0.24 / -0.28 LSB
INL	+1.36 / -1.89 LSB
SFDR	82.9 dBc (fin=10.1 MHz)
SNDR	64.6 dB (fin=10.1 MHz)
FOM	111 fJ/step (fin=10.1 MHz)

7.3.2 ADC With Dynamic Bias ZCD

Figure 7-7 shows the output spectrum when sampling a 15 MHz sinusoidal input at 200 MS/s. The measured peak SNDR reaches 61.2 dB, equivalent to 9.9 bit ENOB. Under the same condition, the peak SFDR is 78.7 dBc. Figure 7-8 shows DNL versus input code and the maximum/minimum DNL is +0.59/-0.39. Figure 7-9 shows INL versus input code and the maximum/minimum INL is +1.53/-2.19 LSB. Table 7-2 summarizes measurements of the ADC with dynamic bias ZCD. Figure 7-10 shows SNDR, SFDR versus sampling frequency. The SNDR gradually degrades as the sampling frequency increases.

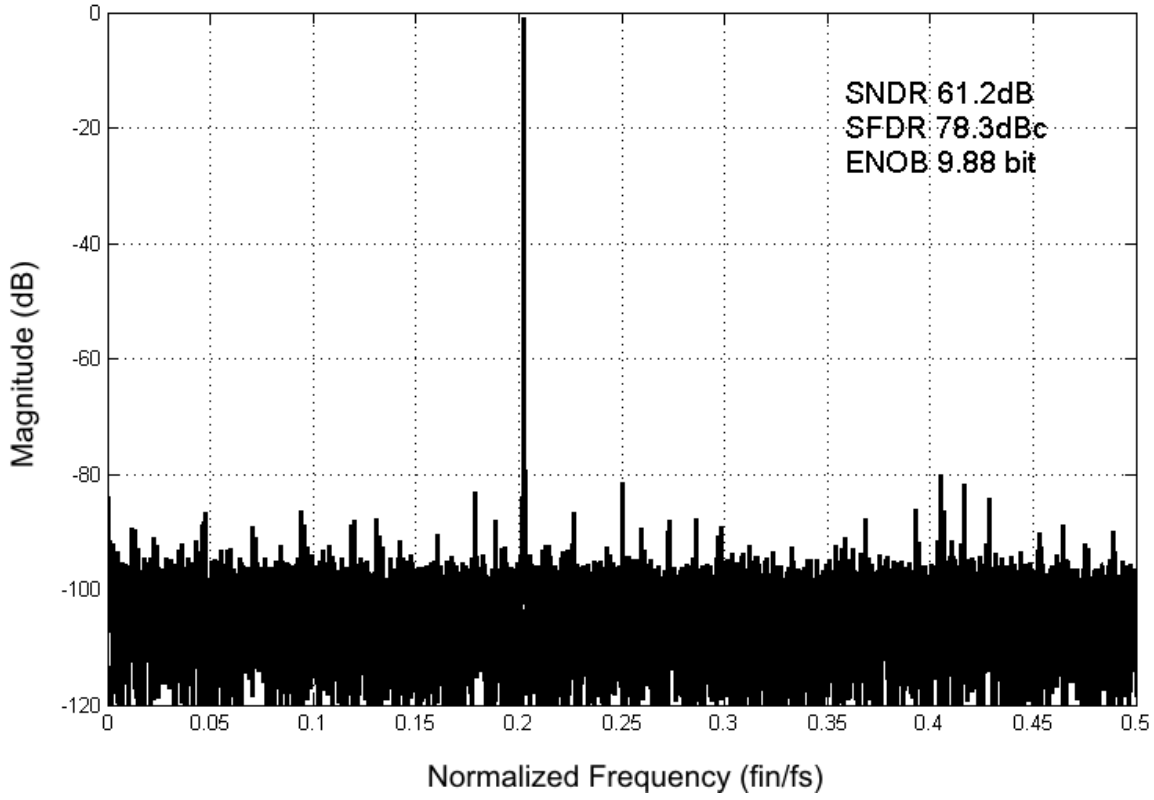


Figure 7-8: ADC digital output spectrum when sampling 15 MHz sinusoidal input at 200 MS/s with dynamic ZCD (output decimated by 16x).

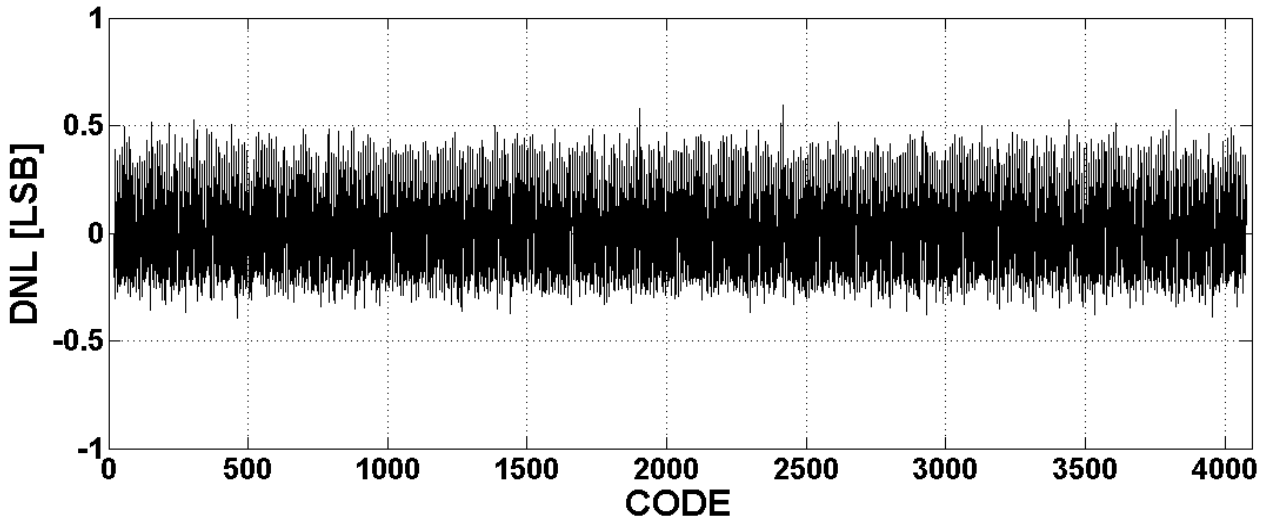


Figure 7-9: DNL of ADC with dynamic bias ZCD.

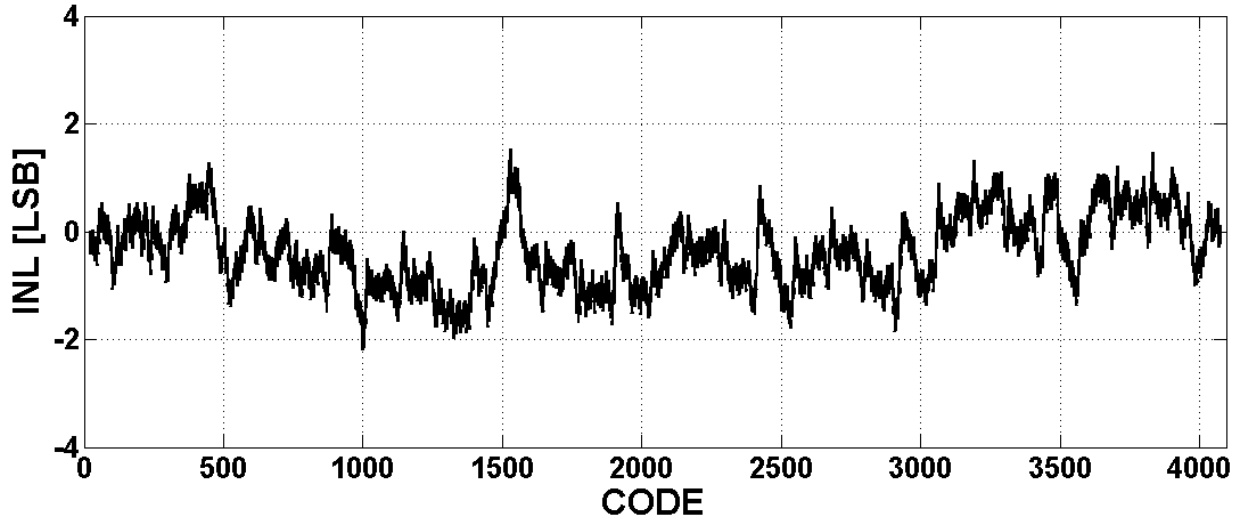


Figure 7-10: INL of ADC with dynamic bias ZCD.

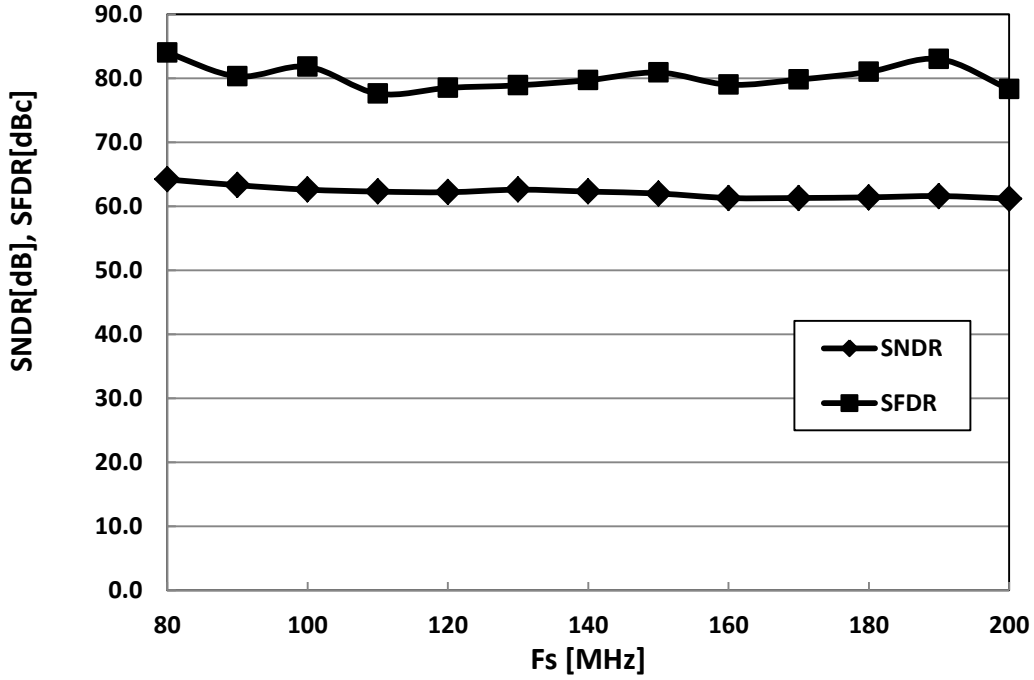


Figure 7-11: SNDR, SFDR versus sampling frequency with dynamic bias ZCD.

Table 7-2: Performance summary of ADC with dynamic bias ZCD

Technology	55nm CMOS 1-Poly 6-Metal
Supply voltage	1.1 V
Resolution	12 b
Conversion rate	200 MS/s
Input voltage Range	2 Vp-p (differential)
Die area	0.282 mm^2
Power consumption	27.1 mW
DNL	+0.59/-0.39 LSB
INL	+1.53/-2.19 LSB
SFDR	78.3 dBc (fin=15MHz)
SNDR	61.2 dB (fin=15MHz)
FOM	143 fJ/step (fin=15MHz)

7.4 Performance Comparison

Table 7-3 compares the performance with recent high speed and high resolution ADCs. Three high speed and high resolution ZCBC pipelined ADCs achieved lower FOM compared to other ADCs. The device described in [21] has big jumps in the DNL because of a larger than expected offset in the comparator. This problem is improved with comparator offset calibration in this work but with additional power consumption. The ADC with constant bias ZCD shows better performance on SNDR compared to the ADC with dynamic bias ZCD. The ADC with dynamic bias ZCD consumes less power but SNDR is worse than the ADC with constant bias ZCD. Thus, FOMs are very similar among them. The SNDR degradation on the ADC with dynamic bias ZCD is believed to occur because of the sensitivity of the dynamic current biasing block from package inductance induced ringing.

Table 7-3: Comparison with recent high speed high resolution ADCs.

Reference	Resolution	Conversion Rate[MS/s]	Technology	SNDR [dB]	SFDR [dBc]	Power [mW]	FOM [fJ/step]
ISSCC 2006[31]	14	100	130nm	66.0	-	224.0	1373.8
ISSCC 2008[33]	14	100	180nm	72.2	88.5	230.0	690.8
ISSCC 2009[34]	14	100	90nm	68.8	85.0	130.0	577.6
VLSI 2008[32]	14	100	90nm	70.0	80.0	250.0	967.4
VLSI 2010[13]	12	100	90nm	63.2	74	6.2	52.7
ISSCC 2009[3]	16	125	180nm	78.6	92.0	385.0	532.3
VLSI 2008[37]	13	250	180nm	65.9	77	140.0	347.4
JSSC 2009[38]	12	200	90nm	59.4	-	186	1220
VLSI 2013[44]	12	200	90nm	65	82	11.5*	39.6*
CICC 2012[21]	12	200	55nm	62.5	78.6	28.5**	114**
This work (Constant bias)	12	200	55nm	64.6	82.9	30.7**	111**
This work (Dynamic bias)	12	200	55nm	61.3	78.5	27.1**	143**

*: Reference buffer and digital calibration engine powers are excluded.

** : Reference buffer and all digital powers are included

7.5 Performance Benchmark

Figure 7-11 shows FOM comparisons of previously published high resolution ADCs that are 12 bit and higher resolutions. It shows very good FOM ADCs for low speed but high speed ADCs consume more power to achieve higher bandwidth amplifier performance, and faster settling. Among the 200 MS/s ADCs, the proposed ADC achieves the lowest FOM.

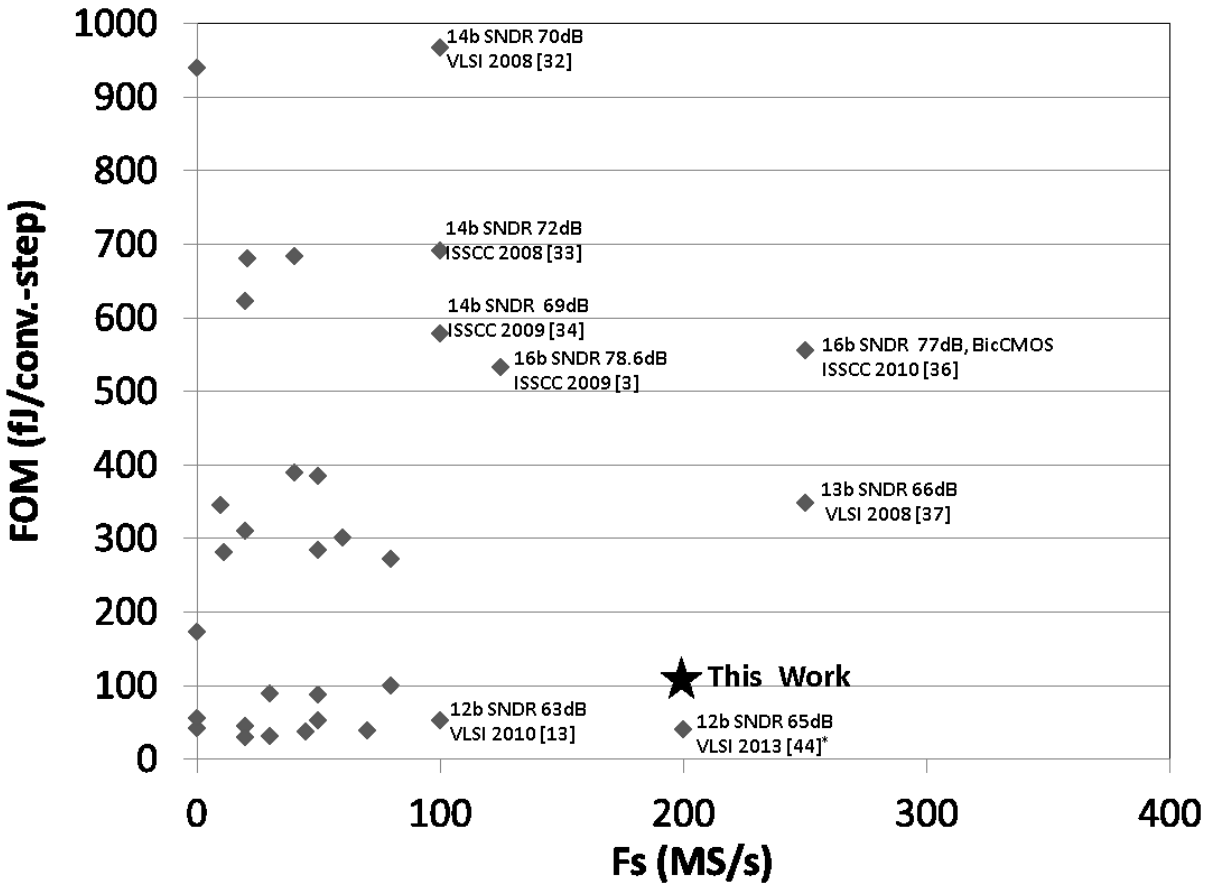


Figure 7-12: Comparison of this design (star) and previously published high resolution (12bit and above) ADCs (diamonds) [30].

7.6 Future Directions

While the zero-crossing circuits have shown the state-of-the-art performance in scaled technology, there are still many opportunities and some outstanding research directions to be explored. The following is a discussion of some of these areas.

First, the number of pipelined stages can be reduced if resolution per stage is increased. To increase resolution, the gain in each stage needs to be larger but this decreases feedback factor in switched capacitor circuits. This makes op-amp based circuit difficult to design. ZCBCs are well suited for amplification for large signal gain of a stage since ZCBCs are inherently open loop and no stability issue with reduced feedback factor.

Second, there is some optimal undershoot voltage and ramp rate for uni-directional dual ramp architecture at a given sampling rate since ZCD requires sufficient settling time before the second slow ramp crosses zero, and lower ramp rate improves accuracy.

Third, ZCBCs have a small amount of current flowing through reference switches during the charge transfer phase. The constant charging current is switched into the reference buffer based on the sub-ADC's decision, and this creates data dependent modulation on the reference voltages because of voltage drop across the switches. The reference precharging architecture with additional capacitors [22] can be used to relax this but these extra capacitors increase noise gain. Thus, the feedback factor reduction leads to more stringent noise requirements for ZCD.

Finally, there have been many publications on ADCs made by combining different architectures. ZCBCs with these architectures can improve performance and power efficiency. For example, two-step zero-crossing based ADC with back-end SAR architecture was recently reported in [47] for 15 bit resolution with state-of-art performance. This ADC adopted high

signal gain for the first and second stages. Also reference current compensation scheme and background control circuit for undershoot voltage in the coarse phase are proposed with ZCBCs.

8 Conclusions

In this dissertation, accuracy and speed of a ZCBC pipelined ADC was improved with the proposed design techniques. A low power high speed high resolution zero-crossing based pipelined ADC was presented. The first approach discussed in this dissertation focused on high resolution and high speed with ZCBC. The ADC exploits a sub-ADC decision after the coarse phase to maximize charge transfer time. A level shifting capacitor for the fine phase current source is also adopted for higher accuracy by increasing the effective output resistance of the fine current source. The systematic offset voltage between coarse and fine phases of the early sub-ADC decision was calibrated by residue range calibration using extra comparators within the following stage's sub-ADC. Random offsets in the sub-ADC comparators are removed with background offset calibration using a charge-pump circuit.

This work represents the highest speed 12-bit ZCBC ADC to date. With the ramp rate and bias current designed to track the sampling rate, the ADC remains functional at frequencies well over the maximum design frequency and the performance degrades gracefully up to 350 MS/s. The circuit demonstrates that ZCBC's provide broad sampling rate tunability with the power consumption approximately proportional to the sampling rate. Dynamic biasing ZCDs reduces the current consumption dramatically, however the performance was degraded a little bit due to sensitivity of the preamplifier current variation and noise from the substrate, power supply, and coupling from the parasitic package inductance. This 12 bit ZCBC pipelined ADCs have achieved the lowest figure of merit among ADCs with no off chip components (off-chip reference buffers, calibration circuits, etc.) as compared to other ADCs with sampling rates of 200 MS/s and higher.

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