SA 18.3: A 1.9GHz Wide-Band IF Double Conversion CMOS Integrated Receiver for Cordless Telephone Applications

Jacques C. Rudell, Jia-Jiunn Ou, Thomas B. Cho[1], George Chien, Francesco Brianti[2], Jeffrey A. Weldon, Paul R. Gray

Dept. of Electrical Engineering and Computer Sciences, UC Berkeley, CA/[1]San Francisco Telecom / Level One Communications/[2]SGS Thomson, San Jose, CA

A number of recent efforts have concntrated on highly-integrated radio receivers using a low-cost silicon process such as CMOS [1, 2]This prototype monolithic CMOS receiver combines RF and baseband functionality by taking the carrier signal at the LNA input and producing a 10b digital baseband waveform. A wide-band intermediate frequency double conversion (WBIFDC) architecture eliminates the need for external narrow-band IF filters.

The experimental chip includes an LNA, an image-rejection mixer, and two baseband signal-processing paths, each of which includes a 2nd-order Sallen and Key anti-alias filter, an 8th-order switched-capacitor filter and a 10b pipelined ADC. The receiver meets the specifications of the digitally enhanced cordless telephone (DECT) standard. The device achieves -90dBm receiver reference sensitivity, -7dBm input IP3, with 198mW overall power dissipation from a 3.3V supply. The design is in 0.6μm double-poly, triple-metal TSMC CMOS process.

The wide-band IF double conversion architecture modulates all of the RF spectrum passing through the RF filter directly to baseband in its entirety, where channel selection is done by low-pass signal processing as in the case of direct conversion (Figure 1). No band-pass filtering is performed at the IF frequency. In contrast to direct conversion, translation takes place in two steps, using two oscillators and two sets of mixers. This provides two principal advantages over direct conversion systems: no oscillator operates at the RF input frequency, and the tuning of the receiver uses the second low-frequency LO. Because the first LO is fixed, easier trade-offs may be obtained with regard to LO phase noise. As in the case of direct conversion, channel selection can be performed at baseband, where digitally-programmable filter implementations can potentially enable more multi-standard capable receiver features.

To reduce the effects of high-frequency coupling, the entire analog RF and baseband signal paths are fully differential. The ADC output drivers are realized with a differential source coupled buffers that reduce digital substrate coupling effects into the analog section of the chip.

The low f_T and gm/Id ratio of CMOS devices limit performance of traditional broadband LNA designs. A tuned narrow-band technique passively enhances voltage gain of the LNA and performs impedance matching [3]. This approach relaxes the conventional trade-off between noise figure and power dissipation and allows linearity to be traded for noise figure. The LNA is implemented as a single-stage differential common source amplifier with on-chip spiral inductors (Figure 2). The LNA input network utilizes bondwire inductor L1 and spiral inductor L2 to enhance the Q of the input network and perform impedance matching. Spiral inductor L3 tunes the output node while improving both the gain and the image rejection of the receiver.

Similar to conventional heterodyne systems, the wide-band IF double-conversion architecture (WBIFDC) requires image rejection. In the DECT standard, approximately 80dB rejection is required in the image-band. The image rejection is accomplished through combination of a front-end external RFfilter, a tuned LNA, and a new image-rejection technique achieved by the double-conversion configuration. This scheme utilizes both the in-phase and quadrature-phase of the local oscillators to realize a broadband image reject function. A complex modulation from RF to IF is performed (Figure 1). The IF signals are mixed to baseband where in-phase and quadrature channels are generated from both of the I&Q IF channels. By properly combining these four baseband signal paths, the correct phase can be obtained for constructive interference of signals above the first local oscillator frequency, while to first-order any RF signals below LO1 are cancelled. Passive components used in conventional image-rejection mixers are eliminated from the signal path. The magnitude of image rejection is limited by gain matching of the mixer paths and by LO deviation from quadrature. To mitigate effects of low-frequency noise at baseband and dc components resulting from self mixing from IF to baseband, two offset cancellation current DACs are used at the image-rejection mixer output.

The individual mixer units are realized with a doubly-balanced CMOS active mixer (Figure 3). The cascode devices M3 and M4 improve isolation between the mixer LO and IF/RF input terminals. Current sources M11 and M12, along with a common-mode feedback loop comprised of M13, M14, and M15, set the output common-mode voltage. Two triode region pMOS devices, M9 and M10, determine both the loading and gain of the mixer cell. The conversion gain is adjustable from 0dB to 10dB by modulating the current through diode-connected device M16.

In the receiver, 55dB overall image rejection is obtained using externally supplied LOs with an on-chip phase shifting network adjusted for quadrature. Loss of the balun is estimated to be 2dB in the image-band while 8dB of rejection is contributed by the LNA, leaving approximately 45dB of image rejection coming from the mixer portion of the receiver.

Aggressive dynamic range requirements are placed on the baseband circuits because the IF filter is removed in the WBIFDC radio architecture. After a mix from IF to baseband, a 2nd-order Sallen and Key filter performs anti-aliasing before subsequent sampling into an 8th-order switched-capacitor filter meeting the bandwidth requirements for a single DECT channel (700kHz BW). In addition to providing channel filtering, the gain is variable from 6dB to 48dB in 6dB increments. The baseband channel filter output is then sampled by a 10b pipelined 10MHz ADC. Capacitor scaling techniques optimize the filter and ADC for noise and power [4].

The prototype is packaged using a chip-on-board technology The backside of the chip is attached directly to the board using a conductive epoxy with bondwires running from chip pads directly to landing zones on the board. Single-ended-to-differential conversion is achieved using an external balun placed in front of the LNA and LO input ports. Experimental results are shown in Tables 1 and 2. A -90dBm receiver reference sensitivity is obtained by measuring the ADC output signal-to-noise ratio. 10dB of SNR is assumed to meet the DECT BER requirement of 10^{-3}. The 3rd-order intermodulation intercept is -7dBm referred to the LNA input (Figure 4).

Acknowledgments:

Support provided by ARPA, California MICRO program, NSF, Rockwell International, GEC Plessey, Xerox, Harris, Philips, and National Semiconductor. Fabrication donated by TSMC and Level One Communications. The authors thank T. Weigandt, R. Meyer, R. Brodersen, and B. Boser for advice and support.

References: See page 476.

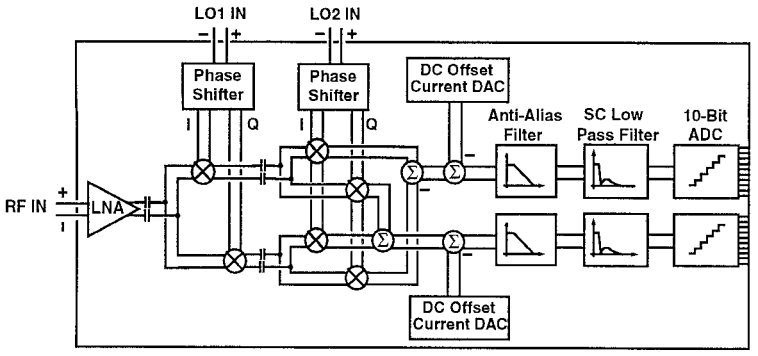

Figure 1: Wide-band IF double conversion receiver architecture.

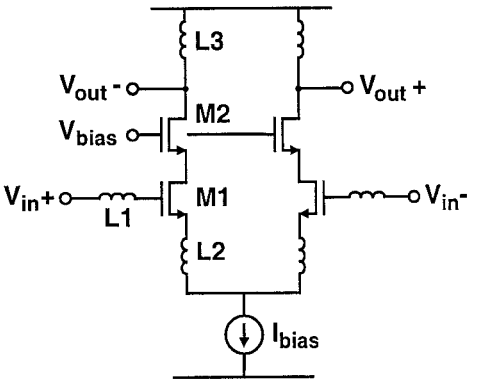

Figure 2: Narrow-band inductively tuned LNA.

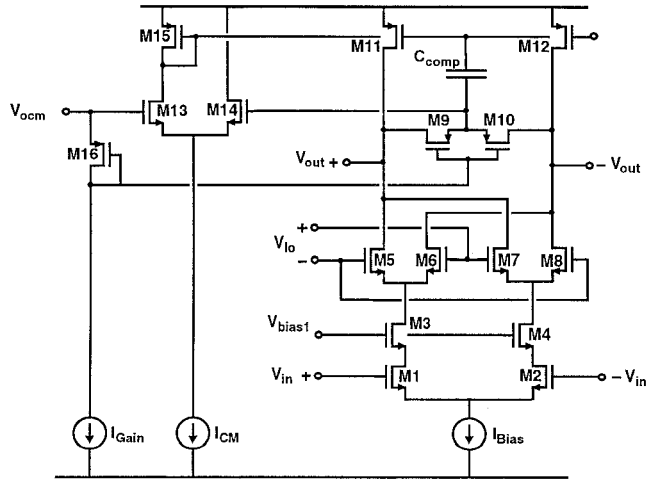

Figure 3: Variable gain active mixer with common-mode feedback.

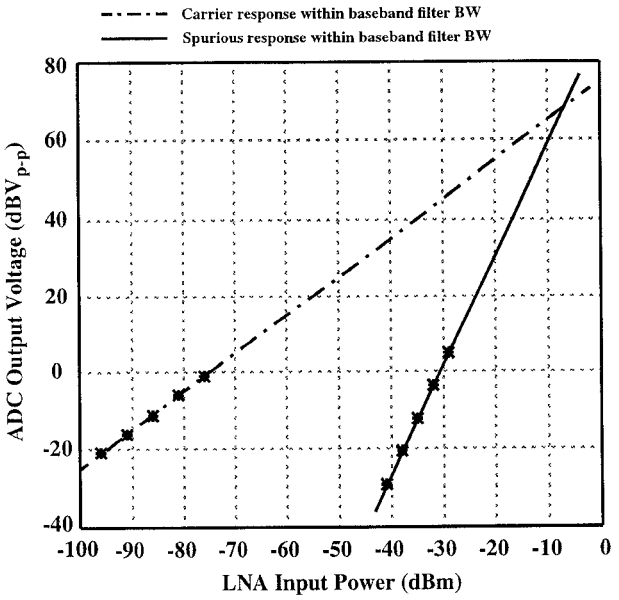

Figure 4: Receiver two-tone (spaced 2 & 4 DECT channels from carrier) test for 3rd-order intermodulation.

Figure 5: See page 476.

Sensitivity	-90dBm*
Input IP3	-7dBm**
Receiver image rejection	55dB
Pob3dB (max. gain setting)	-33dBm***
P-1dB (min. gain setting)	-24dBm
Max. receiver gain	78dB
Min. receiver gain	26dB
Supply voltage	3.3V
LO1	1.7GHz
LO2	182 - 197MHz
Carrier frequency	1.882 - 1.897GHz
Active chip area (including bias)	15mm²

* -83dBm sensitivity required for DECT.
** -27dBm input referred IP3 required for DECT.
*** Blocker 1 DECT channel from carrier.

Table 1: Receiver performance features.

LNA	41 mW
RF to IF mixers	17 mW
IF to baseband mixers	34 mW
Baseband filters	66 mW
ADCs	40 mW
Total chip	198 mW

Table 2: Receiver power dissipation.

(Continued from page 305)

References:

[1] Rofougaran, A., et al., "A 1GHz CMOS RF Front-End IC for a Direct-Conversion Wireless Receiver," IEEE J. of Solid-State Circuits, pp. 880-889, July 1996.

[2] Crols, J., M. Steyaert, "A Single-Chip 900 MHz CMOS Receiver Front-End with a High Performance Low-IF Topology," IEEE J. of Solid-State Circuits, pp.1483-1492, Dec.,1995.

[3] Shaeffer, D., T. Lee, "A 1.5V, 1.5GHz CMOS Low Noise Amplifier," Symp. on VLSI Circuits Digest of Technical Papers, pp. 32-33, June, 1996.

[4] Cho, T., et al., "A Power-Optimized CMOS Baseband Channel Filter and ADC for Cordless Applications," Symp. on VLSI Circuits Digest of Technical Papers, pp.64-65, June, 1996.

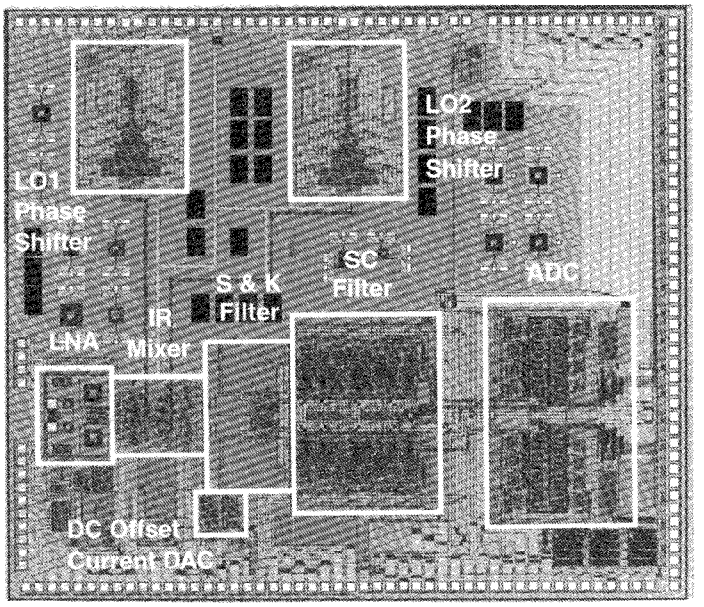

Figure 5: Receiver chip micrograph.

SA 18.5: A 2.7V DECT RF Transceiver with Integrated VCO

(Continued from page 309)

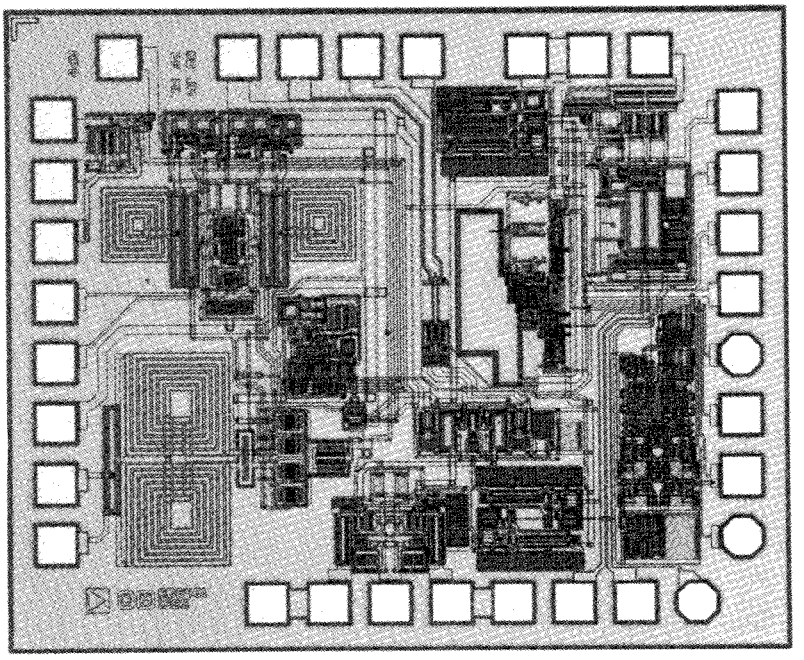

Figure 5: Chip micrograph.