

Introduction to the Special Issue on the 2005 IEEE International Solid-State Circuits Conference

THIS issue of the JOURNAL OF SOLID-STATE CIRCUITS is a selection of papers from the 2005 IEEE International Solid State Circuits Conference. It presents outstanding papers from the Analog, Wireless, Wireline, and Imaging Sessions.

I. ANALOG

The selection of innovative analog papers spans a wide range of applications and bandwidth, literally from DC to the gigahertz range. The papers are presented roughly in order of speed. Many classic circuit blocks are taking advantage of new developments in advancing technologies or producing surprising solutions as voltage scaling challenges the circuit designer.

The paper by Ahuja *et al.* presents a technology that has seen a number of research papers over the years now applied in its most basic form—the application of the floating gate device as a voltage reference, something that may have a significant impact on future IC designs.

The paper by Chatterjee *et al.* takes supply voltage levels to the extreme of 0.5 V and examines the techniques required to build continuous-time filters under these constraints. It shows interesting solutions both on the system and circuit level.

The paper by Gaalaas *et al.* implements a class-D amplifier by embedding the output stage in a delta-sigma loop. The most critical idea in this circuit is the reduction of the output switching frequency by introducing hysteresis in the output comparator. Thus, both the noise shaping from the delta-sigma and a switching frequency low enough to maintain good efficiency can be obtained.

The next paper, by Nguyen *et al.*, also deals with audio data conversion, here a delta-sigma ADC. The key implementation idea here is the use of both continuous-time and discrete-time circuits to yield a power-efficient modulator.

The paper by Ahn *et al.* again takes up the challenge of very low supply voltage and the resulting difficulty of implementing a functional switched-capacitor circuit. The solution, a switched resistor branch, is very simple and elegant.

The next paper, by Yu *et al.*, also presents a delta-sigma converter. Here the converter is implemented in 90-nm technology and thus offers new tradeoffs between analog and digital complexity. The focus is on the reduction of the DAC complexity in the feedback path by putting more truncation estimation into the digital domain.

The paper by Doerrer *et al.*, on the other hand, addresses the reduction of complexity in the ADC stage of a multibit delta-sigma. By analyzing the usage of the comparators in the ADC over time, it is derived that only three comparators are necessary

as long as their thresholds are moved as the signal moves. This sliding comparator window reduces hardware complexity.

The paper by McNeill *et al.* shows a surprisingly simple background calibration technique. An algorithmic ADC is split in two. The conversion result is derived from the sum of the conversions whereas the calibration result is derived from the difference. This technique seems applicable also outside the specific application chosen.

The paper by Ahmed and Johns demonstrates an interesting experiment in scalability of converters. The pipeline converter shown can convert at different speeds and power levels as the application requires. Key is that power management techniques are applied that allow an enormous slowing down with sufficient power scaling to still have acceptable performance, such as rapid power-on and power-off opamps.

Finally, the paper by Choe *et al.* gives a performance benchmark for a high-speed DAC implemented in a GaAs technology that presents constraints to the designer that are quite different to those encountered in state-of-the-art CMOS. The result is a state-of-the-art performance DAC with fairly low complexity and attention to detail to the behavior of each individual device.

The large variety of circuits and applications demonstrates yet again that analog design is thriving under the challenges and opportunities provided by today's technologies in terms of voltage scaling and integration. But a few papers also demonstrate that certain functions are best implemented by staying with a technology that may not be the latest, but simply the best for the task.

II. WIRELESS COMMUNICATION

This year's wireless communication section of the JOURNAL reflects many of the common themes found in the RF IC community for the past two decades: higher levels of system integration, and the ability to operate on higher carrier frequencies for a given semiconductor technology, as well as a number of papers which introduce new techniques to address some of the classic challenges of mixed-signal communication integrated systems and circuits. In addition, there are a collection of papers which highlight new wireless standards and applications which have recently evolved such as ultra-wideband transceivers and digital video broadcasting (DVB) receivers for mobile applications.

The "holy grail" for mobile communication devices, since the early 1990s, has been the realization of a true single-chip radio, with all-analog RF, mixed-signal baseband, and the necessary digital electronics integrated onto a single CMOS die. The communication section of this issue begins with three papers that report the first ever monolithic CMOS wireless transceivers. The first paper, by Staszewski *et al.*, demonstrates a single-chip GSM/EDGE transmitter integrated on a die with

the remainder of the transceiver. As the title implies, "All-Digital PLL and Transmitter for Mobile Phones," this device, integrated in a 90-nm process, utilizes an all-digital PLL with a digitally controlled oscillator (DCO) to realize a wide-bandwidth loop allowing direct modulation of an I/Q digital baseband signals in transmitter mode while acting as frequency synthesizer when necessary. Next, two papers detail the implementation of fully integrated 802.11 (WLAN) transceivers. The first paper, by Mehta *et al.*, is titled "An 802.11g WLAN SoC." The chip described in this paper contains all the radio components including the RF, analog, and mixed-signal baseband, as well as the digital components necessary to realize all of the PHY and MAC functions for a complete 802.11g transceiver, and is implemented in 0.18- μm CMOS. The IC transmits 0 dBm with EVM-compliant output power for a 64 QAM OFDM signal with a receive sensitivity as high as -92 dBm. The second paper, by Khorram *et al.*, is entitled "A Fully Integrated SOC for 802.11b in 0.18- μm CMOS." This paper describes a fully integrated system-on-a-chip intended for use in 802.11b applications, built in a 0.18- μm CMOS process. All the radio building blocks including the power amplifier (PA), the PLL loop filter, the antenna switch, and the complete baseband physical and MAC layers are integrated on a single chip.

This special issue presents two papers which illustrate the possibilities of integrating MIMO and phased-array systems in silicon. The first such paper presents "A Fully Integrated 24-GHz Phased-Array Transmitter in CMOS" by Natarajan *et al.* and demonstrates the capabilities of modern CMOS devices to operate on exceptional high carrier frequencies in the 24-GHz band. This device is the first fully integrated 24-GHz transmitter in CMOS and utilizes a two-step quadrature heterodyne transmitter which is able to operate on a carrier of 24 GHz, while achieving data rates up to 500 Mb/s. The four-element array includes CMOS PAs, which can deliver up to 14.5 dBm output power, and achieves a peak-to-null ratio of 23 dB with 7° of beam-steering resolution. The next paper, "A Four-Antenna Receiver in 90-nm CMOS for Beamforming and Spatial Diversity," by Paramesh *et al.*, utilizes a novel front-end architecture. A Cartesian combiner is used to simplify the signal path, eliminating a set of mixers and the associated LOs to greatly reduce both die area and power consumption. The device, which was implemented in a 90-nm CMOS process, is capable of attenuating adjacent channel interferers while providing 12 dB of array gain with four channels.

Commensurate with the advent of new DVB standards is an interest in realizing high-integration TV tuner systems for mobile applications. This was evidenced by several papers at the 2005 ISSCC, one of which, by Heng *et al.*, presented "A CMOS TV Tuner/Demodulator IC With Digital Image Rejection." This device uses a low-IF architecture with an adaptive digital-image rejection system to facilitate a multistandard TV tuner capable of tuning to bands from 48–860 MHz. This chip uses a 0.25- μm CMOS process and consumes 1 W with a 2.5-V supply. Antoine *et al.* present the next paper on DVB, "A Direct-Conversion Receiver for DVB-H." This TV tuner was implemented in a BiCMOS process, utilizes four VCOs and an integer PLL, and is capable of tuning to multiple bands through the use of a variable bandwidth baseband filter.

Similar to DVB, this year's ISSCC saw a number of papers which attempted to realize transceiver solutions for very high data rate and short-range standards and applications. The introduction of the ultra-wideband standard has motivated several groups around the world to explore transceiver architectures and circuits for the 2.4–10-GHz bands. Although the first paper in this section is outside the bound of the UWB standard, the paper introduces a new communications protocol that is tailored for a more efficient and highly integrated hardware solution. Verma *et al.* present "A 17-mW 0.66- mm^2 Direct-Conversion Receiver for 1-Mb/s Cable Replacement." This transceiver uses a new coding scheme which permits the integration of a high-pass filter to mitigate low-frequency noise. The die area is smaller than any reported Bluetooth-class radio to date. Next, Razavi *et al.* present a direct-conversion UWB transceiver for Mode 1 OFDM applications. This paper, "A UWB CMOS Transceiver," uses a common-gate input stage to allow direct sharing of the receiver antenna with the transmitter. The device is designed in a 0.13- μm CMOS technology with a receive noise figure (NF) of 6.5–8.4 dB across three bands with a transmitter 1-dB compression point of -10 dBm. Next, Roovers *et al.* present "An Interference-Robust Receiver for Ultra-Wideband Radio in SiGe BiCMOS Technology," which is implemented in a 0.25- μm BiCMOS technology. This paper introduces an ultra-fast, low spurious content, frequency-hopping synthesizer, which, when used with their highly linear RF circuits, realizes an interference-robust receiver. The final UWB paper is "A 3.1- to 8.2-GHz Zero-IF Receiver and Direct Frequency Synthesizer in 0.18- μm SiGe BiCMOS for Mode-2 MB-OFDM UWB Communication" by Ismail and Abidi. The chip described in this paper has an RF receive chain and direct frequency synthesizer which generates seven carrier frequencies in the 3.4–7.9-GHz range. The receiver has a NF of 3.3–4.1 dB and uses 88 mA from a 2.7-V supply.

The final group of papers is a collection of RF blocks and subsystems which present new techniques to further current state-of-the-art performance. Two PA papers begin this section with "A 21–26-GHz SiGe Bipolar Power Amplifier MMIC" by Cheung and Long. The paper describes a 21–26-GHz three-stage SiGe PA with up to 20% PAE and 15 dB of gain, delivering +21 dBm in a SiGe technology. This paper describes techniques to design magnetically coupled Class-AB stages for use in either automotive radar or WLAN applications. This is followed by a paper by Reynaert and Steyaert which describes a PA for use in a polar modulator. The paper, "A 1.75-GHz Polar Modulated CMOS RF Power Amplifier for GSM-EDGE," presents a CMOS PA with a peak output power of 27 dBm and a PAE as high as 34%. Because the PA operates inside a polar modulator transmit system, the transmitter may operate on both constant and nonconstant envelope modulation signals. The next paper, " G_m -Boosted Common-Gate LNA and Differential Colpitts VCO/QVCO in 0.18- μm CMOS" by X. Li *et al.*, presents a couple of RF circuit techniques which help to reduce the overall power consumption of an LNA and improve the close-in and far-out phase noise characteristics of a Colpitts oscillator. Guermandi *et al.* present a new synthesizer implementation in "A 0.83–2.5-GHz Continuously Tunable Quadrature VCO," which greatly extends the frequency cov-

erage of a single VCO, thus eliminating the need for multiple VCOs and reducing the die area when used in multiband applications. The final paper is a "A Noise Cancellation Technique in Active RF-CMOS Mixers" by Darabi and Chiu. A circuit technique to reduce the $1/f$ noise contribution of the switching core in a Gilbert-type mixer is described. By significantly reducing the mixer flicker noise generated by a CMOS current commutating mixer, direct-conversion architectures become more attractive for narrowband low-noise applications.

III. WIRELINE COMMUNICATION

The papers on wireline communication circuits fall under the following categories: high-end backplane transceivers, optical communication and CDR circuits, digitally controlled low phase noise crystal oscillator (DCXO), and 80-Gb/s high integration level SiGe BiCMOS circuits.

Backplane papers represent a new page in 6.25-Gb/s backplane NRZ transceivers CMOS circuits designed to operate over lower speed (1–3 Gb/s) legacy backplanes. Their requirements originate to Common Electrical I/O (CEI)–Electrical and Jitter Interoperability agreements for 6G+ b/s and 11G+ b/s I/O [OIF-CEI-02.0, finalized by Optical Internetworking Forum (OIF) in February 2005].

To tackle channel performance degradation such as frequency-dependent loss, reflections, and crosstalk, these transceivers employ multi-tap feed-forward equalization (FFE) in the transmitter and decision feedback equalization (DFE) in the receiver. While these equalization techniques are well known in digital communication, these papers are dealing with analog-reach circuit details specific to multi-gigabit-range operation. In essence, each paper represents an algorithmic variation for DFE implementation. Another design challenge is to address low bit-error-rate (BER) requirements of 10^{-15} or less.

The 4.9–6.4-Gb/s transceiver core of the first paper, by Beukema *et al.*, uses a 4-tap FFE in the transmitter, a two-path VGA, and a peaking amplifier followed by a 5-tap DFE in the receiver. The IC enables operation on ISI channels with over 30 dB loss at 3.2 GHz. It achieves a power efficiency of 45 mW/Gb/s.

The 6.25-Gb/s transceiver presented in the paper by Payne *et al.* employs a 4-tap DFE receiver architecture that uses fast direct feedback of the first-tap output to cancel post-cursor ISI and a 4-tap FFE in the transmitter. It operates at a BER $< 10^{-15}$ over legacy 1-Gb/s backplane channels.

The last backplane paper, by Krishna *et al.*, describes a power-efficient transceiver core operating from 0.6 to 9.6 Gb/s using adaptive receiver equalization with a 1-tap unrolled-type DFE preceded by a linear equalizer. The transmitter employs an FFE equalizer with asymmetrically configured post-cursor and pre-cursor taps. The core dissipates 150 mW at 6.25 Gb/s.

Advances in optical communication circuits are presented in the next three papers.

A low-power 4×10 -Gb/s transceiver, presented in the paper by Kromer *et al.*, demonstrates an unprecedented level of integration and performance in 80-nm CMOS. A 1.25-Gb/s burst-mode receiver, designed by Nakamura *et al.*, achieves an acquisition time of fewer than 20-bit intervals and -30 -dBm

sensitivity suitable for optical access networks. Finally, the paper on a 10-Gb/s two-dimensional eye-opening monitor, by Analui *et al.*, describes original architecture and circuit implementation aimed for automatic adaptation in equalizers for optical links.

The paper on CDR by Toifl *et al.* presents a novel architecture for clock phase interpolation at 2.5 GHz. A phase interpolator of 2.5-GHz clocks is replaced with an interpolator of low-speed signals at the outputs of an array of phase detectors configured in the PLL. The resulting phase resolution is better than 3 ps with 0.94-ps-rms jitter. This technique further enables area-efficient 10-Gb/s CDR design.

A 12.5 Mb/s–2.7 Gb/s continuous-rate CDR is the subject of the paper by Dalton *et al.* The circuit detects an input data rate and acquires a lock to new frequency without an external reference clock. In tracking mode, it uses a dual-loop DLL/PLL to provide superior jitter performance compared to a conventional PLL.

The DCXO-based link synchronization is a relatively new and promising technology in digital communications. A 0.004 ppm/step digitally controlled 26-MHz crystal oscillator (DCXO) with extremely low phase noise is presented in the paper by Lin. The key factor enabling high-phase-noise performance is a Colpitts-type crystal oscillator controlled by a highly linear switched-capacitor DAC. The proposed sliding sigma-delta modulation, applied to the last active thermometer element in the DAC, provides the final required frequency resolution and linearity. The DCXO's superior phase noise performance makes it ideally suitable for GSM applications, as well as for clock synthesis and synchronization in wireline communications links.

The final paper in wireline section, by Dickson *et al.*, presents an 80-Gb/s pseudo-random binary sequence generator in SiGe BiCMOS technology. The IC represents the highest integration level achieved for the circuits operating at such a high speed. Circuit employs BiCMOS digital cells biased at maximum f_t current, with inductive peaking (total 100 spiral inductors) and transmission-line style interconnects.

IV. DISPLAYS, SENSORS AND IMAGERS

A total of eight papers from the Imagers, MEMS, and Displays section of the 2005 ISSCC have been selected for this issue. They highlight not only state-of-the-art circuit design techniques, but, maybe more importantly for the reader to understand and appreciate, the constraints and restrictions within these diverse applications, whether imposed by the physical array format, the environment, or the sensitivity required. The three imaging papers selected this year show a design technique to reduce *KTC* noise, a compact column-based ADC within an extended dynamic range sensor, and an application-specific tracking use of a sensor. The display community has contributed two very different papers, a microdisplay CMOS backplane that itself emits light and a highly compact linear array of switched-capacitor DACs for LCD driving. The three final papers show the diversity and application-specific nature of this section of the ISSCC, a neural *in vitro* recording device, a detector of heavy metals, and an extremely accurate

temperature sensor that is one of the best demonstrations of combining virtually every known high-performance analog technique within one application.

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Axel Thomsen (M'93) was born on January 16, 1965, in Hamburg, Germany. He received his undergraduate education in electrical engineering at the Polytechnic University of Braunschweig, Germany. In 1988, he transferred to the Georgia Institute of Technology, Atlanta, where he received the Ph.D. degree in 1992. His areas of research were analog integrated circuits, parallel circuit architectures, and floating-gate devices.

In 1993, he joined the faculty of the University of Alabama, Huntsville, where he worked on electro-optic circuit applications and analog circuits for telecommunications. In 1995, he joined Cirrus Logic, Austin, TX, where he worked on high-precision low-power data-acquisition circuits for seismic and industrial measurement applications. In 2001, he joined Silicon Laboratories Inc., Austin, where he is currently a Design Manager working on timing circuits and PLLs. Occasionally, he teaches at the University of Texas in Austin. He has published ten journal papers and holds 30 patents.



Jacques C. Rudell (M'98) received the B.S. degree in electrical engineering from the University of Michigan, Ann Arbor. He later received the M.S.E.E. degree from the University of California, Berkeley, where he focused on high-speed, low-power digital-adaptive equalization techniques for magnetic disk-drive channels employing partial response signaling. He went on to receive the Ph.D. degree from University of California, Berkeley, completing his thesis and research on wireless transceiver architectures and systems suitable for high levels of integration in CMOS with multi-standard/modal operation capabilities.

From 1989 to 1991, he was an IC Designer and Project Manager with Delco Electronics (now Delphi), where his work focused mainly on bipolar analog circuits for automotive applications. From late 2000 to 2001, he was a Postdoctoral Researcher at the University of California, Berkeley, in addition to holding consulting positions in several Silicon Valley firms. In early 2002, he joined Berkana Wireless, San Jose, CA, as an Analog/RF IC Design Engineer, and later became the Design Manager of Advanced IC Development exploring new transceivers systems

in CMOS for a number of wireless applications. In September 2005, he joined Intel Corporation as the Manager of the Advanced Radio Circuits and Architecture Research Group.

Dr. Rudell is a member of Tau Beta Pi and Eta Kappa Nu. He was designated a James B. Angell Scholar at the University of Michigan. He received the 1998 ISSCC Jack Kilby Best Student Paper Award and was a co-recipient of the 2001 ISSCC Lewis Best Paper Award. In 1999, he received the UC Berkeley EECS Demetri Angelakos Memorial Achievement Award. In addition, he is on the technical program committees for both the International Solid-State Circuits Conference (ISSCC) and the Radio Frequency Integrated Circuits (RFIC) Symposium.



Yuriy Greshishchev (M'95–SM'02) received the M.S.E.E. degree from Odessa Electrotechnical Institute of Communications, Odessa, Ukraine, in 1974 and the Ph.D. degree in electrical and computer engineering from V. M. Glushkov Institute of Cybernetics, Microelectronics Division, Kyiv, Ukraine, in 1984.

From 1976 to 1994, he worked with research and development organizations and academia on high-speed silicon bipolar and GaAs MESFET ADC and DAC integrated circuits. In 1994, he joined the Department of Electrical and Computer Engineering, University of Toronto, where he conducted research on GaAs MESFET linear transmitter design for digital wireless communication. He was with Nortel Networks, Ottawa, Ontario, from 1996 to 2002, where he was a principal contributor to the industry first highly integrated 10 Gb/s–40 Gb/s SiGe and INP ICs for optical communications. He specializes in Gigabit transceivers and SerDes circuits for telecom, datacom, and storage applications.

Dr. Greshishchev has served as a member of the ISSCC Technical Program Committee, Wireline Subcommittee, since 2001.



J. E. D. Hurwitz (M'91) received the B.Eng. in electrical and electronic engineering from Nottingham University, Nottingham, U.K., in 1987.

After graduation, he joined GEC Plessey Semiconductors, where he worked on mixed-signal CMOS telecommunication circuits and on design-related process issues. In 1990, he moved to Matra MHS, France, where he worked on circuits for videotelephony, before becoming an independent consultant in the field of analog video and sensor design. In 1995, he joined VLSI Vision Limited (which was later acquired by ST Microelectronics), Edinburgh, U.K., as Principal Technologist, a company which successfully became one of the pioneers of CMOS imaging. In recent years, he has worked on all aspects of the architecture, design, development, and manufacturability of CMOS image sensor systems (from photons to bytes) and their optimization for the mobile cellular applications, including the publication of an open industry standard for camera modules. For several years, he has been an active participant of the technical committees of the ISSCC and the IEEE workshop on AIS and CCDs, and has provided consultancy in the fields of

displays and biosensors. In 2005, he left ST Microelectronics to co-found a start-up company, Gige Semiconductor Limited.