Check for updates

Research Article | Vol. 32, No. 16 / 29 Jul 2024 / Optics Express 27552

Optics EXPRESS

Post-processing of phase change material in a zero-change commercial silicon photonic process

UTHKARSH ADYA,[1] DANIEL STURM,[1] RUI CHEN,[1] CHANGMING WU,[1] ARKA MAJUMDAR,[1,2] MO LI,[1,2] AND SAJJAD MOAZENI[1,*]

[1] *Department of Electrical and Computer Engineering, University of Washington, Seattle, USA*
[2] *Department of Physics, University of Washington, Seattle, USA*
[*] *smoazeni@uw.edu*

Abstract: Integration of phase change material (PCM) with photonic integrated circuits can transform large-scale photonic systems by providing non-volatile control over phase and amplitude. The next generation of commercial silicon photonic processes can benefit from the addition of PCM to enable ultra-low power, highly reconfigurable, and compact photonic integrated circuits for large-scale applications. Despite all the advantages of PCM-based photonics, today's commercial foundries do not provide them in their silicon photonic processes yet. We demonstrate the first-ever electrically programmable PCM device that is monolithically post-processed in a commercial foundry silicon photonics process using a few fabrication steps and coarse-resolution photolithography. These devices achieved 1.4 dB/µm of amplitude switching contrast using a thin layer of 12.5 nm GeSbTe in this work. We have also characterized the reconfiguration speed as well as repeatability of these devices over 20,000 switching cycles. Our solution enables non-volatile photonic VLSI systems that can be fabricated at low cost and high reliability in a commercial foundry process, paving the way for the development of non-volatile programmable photonic integrated circuits for a variety of emerging applications.

© 2024 Optica Publishing Group under the terms of the Optica Open Access Publishing Agreement

1. Introduction

Silicon photonics has proven to be a reliable technology platform for the commercial wafer-scale fabrication of large-scale photonic integrated circuits (PIC). These PICs have a variety of applications such as high-speed optical I/O and co-packaged optics (CPO) [1,2], LiDAR for 3D sensing and imaging [3,4], optical neural networks [5,6] and quantum information processing [7]. Many of these applications require hundreds or even thousands of photonic devices including phase shifters and switches [8]. Further scaling of programmable PIC [9], that leverage the large-scale commercial foundry processes [10,11], is crucial to enable these applications.

Electrically programmable devices such as phase-shifters and modulators can be realized in silicon photonics foundry platforms by utilizing the thermo-optical effect [12,13] and free-carrier plasma dispersion [14], respectively. The carrier plasma effect is a relatively weak electro-optical effect but it is widely used for high-bandwidth phase or amplitude modulation due to its compatibility with silicon photonic processes and high-speed operation. On the other hand, the thermo-optic effect is slow but is stronger because of the large thermo-optical coefficient of silicon ($dn/dT \approx 10^{-4}$), which makes it suitable for DC or low-speed phase shifters and switches. However, its thermal nature normally results in power-hungry photonic devices (around $10mW$ for π phase-shift [15]). Thus, there is a need for alternative programming techniques that provide large modulation depth, low-power operation, and have a small footprint. Nonvolatile programming techniques [16] are promising candidates for creating such power-efficient programmable devices with zero static power. Today, non-volatile memories such as memristors and flash memories, among others [17] are commercially available, and some

#526141 https://doi.org/10.1364/OE.526141
Journal © 2024 Received 12 Apr 2024; revised 2 Jun 2024; accepted 21 Jun 2024; published 16 Jul 2024

Optics EXPRESS

of CMOS foundries are now offering these non-volatile memory technologies. Integration of non-volatile devices in CMOS technologies is a major step towards the post-Moore era. While photonics is in its early days of silicon photonics Moore's law [18], the integration of emerging and novel materials with commercial silicon photonics can pave the path toward scalable non-volatile programmable photonics.

Phase change materials (PCM) such as GeSbTe (GST) [19–21], SbS [22–24], and SbSe [25–28] alloys can be particularly promising solutions to provide non-volatile programmability for photonic devices. There were several demonstrations of photonic switches using these materials [23,29]. GST in particular exhibits a large contrast in refractive index between the crystalline (n = 6.63, k = 1.08) and amorphous (n = 3.88, k = 0.024) states [19]. Furthermore, GST is already widely used in re-writable optical data storage technologies [30,31] and can retain the data for over ten years [32], making it an attractive material choice for non-volatile photonic switches. The state of the material can be programmed by applying a tailored heat pulse. To achieve electrical programming, a tunable micro-heater structure can be designed in a silicon photonic process using either a doped waveguide [33,34] or a PIN diode structure [20,35,36], this type of diode has an undoped intrinsic region between the n-type and p-type doped regions.

The next generation of commercial silicon photonics can benefit from the addition of PCM to enable ultra-low power, highly reconfigurable, and compact PIC for large-scale applications. However, PCM does not exist in any of today's commercial foundry silicon photonic processes. Therefore, initial monolithic integration with these processes using post-processing is crucial to build proof-of-concept PCM-based PICs at this stage [37–40]. Some of the previous attempts to embed PCM in silicon photonics at a foundry always required a custom run or requests for existing technology fabrication flows [25]. These methods can impact the reliability and yield of the process as well as risk the performance of existing devices/materials. To overcome these issues, we report a post-processing methodology for back-end-of-line (BEOL) monolithic integration of GST in the Advanced Micro Foundry (AMF) commercial silicon photonic process where GST can be electrically programmed using process-compatible PIN micro-heaters. While the initial results are based on GST, other PCM materials can also be integrated by the same methodology.

This paper is organized as follows. We discuss the design considerations for PCM micro-heater design in the AMF silicon photonics process with no custom changes ("zero-change") and our proposed PCM post-processing methodology in Section 2. Section 3 describes the experimental results. Finally, we summarize the results and discuss possible future directions in Section 4.

2. PCM microheater design in AMF silicon photonics

Micro-heater structures can electrically reconfigure the device by inducing a micro-structural phase change from amorphous (a-GST) to crystalline (c-GST) state (called "SET" process) and vice versa (called "RESET" process) for GST [41]. The SET process occurs when GST is maintained at a temperature above its crystallization temperature ($T_c \sim 150°$ C assuming $\sim 10°$C/min heating rate characterizations [42–44]) and below the melting temperature ($T_m \sim 650°$ C [29]). The RESET process occurs when GST is heated above T_m and cooled down rapidly. We used a multi-project wafer (MPW) program to design our chip in this process. We designed a PIN micro-heater device using the features of the AMF process to enable the SET and RESET processes. Rib waveguides were used which are intended to operate in a single-mode regime in the O-band (Fig. 1(b)). In order to access the silicon optical layer, we exploited an existing feature of the process that opens an oxide window down to the silicon layer which exposes the waveguides, as illustrated in Fig. 1(c), typically utilized for sensing applications. The schematic of the PIN micro-heater is illustrated in Fig. 1(b), showing the 2 μm opening on top of the waveguide. The desired thickness of GST was deposited into the oxide window through deposition methods such as sputtering. All non-silicon layers including metal and via layers were kept at least 5 μm away from the oxide opening area to avoid damaging the metal routings during the oxide etch

Optics EXPRESS

process at the foundry, which incurred a higher resistance of our micro-heater parasitic junctions. The slab sections close to the waveguide have low doping (n+/p+) to avoid excess carrier optical loss, and regions farther from the waveguide have high doping (n++/p++) to lower the overall resistance of the device and also to achieve low contact resistance at the vias.

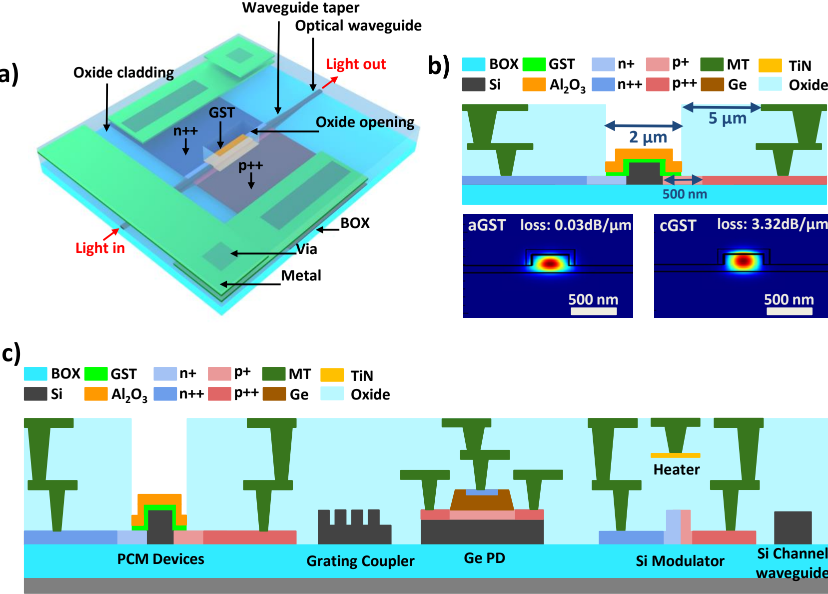

Fig. 1. (a) Illustration of the electrically programmable PIN micro-heater. (b) Cross-section of the PIN micro-heater, and mode profile simulations with GST (10 *nm*) film on the waveguide in the amorphous state (a-GST) and the crystalline state (c-GST). (c) Cross-sectional view of AMF silicon photonic process including the post-processed GST.

Post-processing Methodology for GST Integration. The monolithic integration of GST with the AMF silicon photonic process was demonstrated by a few simple post-processing steps at the die ($3mm \times 3mm$) level in the Washington Nanofabrication Facility (WNF). Figure 2 illustrates our simple post-processing scheme, which has a minimal amount of steps and utilizes coarse-resolution photolithography. Once the dies were received, we first mounted them onto a larger dummy Si carrier chip, using AZ10XT, for ease of handling, and we then spin-coated them with a photoresist (AZ1512) and patterned them using the Heidelberg DWL66+ laser writer. Patterning was performed to block the metal pads and grating couplers from the GST and oxide capping layer deposition. Edge bead formation was observed during spin coating because of the small size of the chip, which was mitigated by surrounding the chip edges with dummy chips of the same thickness. This reduced the edge bead size by a certain extent and we also adjusted the laser writing power to account for the edge beads. The nominal thickness of the AZ1512 photoresist here is 1 μm. The laser wavelength used during writing was 405nm and the exposure parameters used for the operation include a laser power of 295 mW, intensity of 80 %, and a transmission of 25. After a post-bake, the resist was developed in AZ MIF developer for around 1 minute 45 seconds. After performing development in AZ MIF developer we then sputtered a 10 nm thick film of GST, followed by a 60 nm thick Al_2O_3 through atomic layer deposition (ALD) at 50° C, which is lower than the crystallization temperature of GST (~ 150° C). ALD is an excellent choice for encapsulation layer deposition due to its conformal nature. Thermal ALD, performed at 150° C, can provide a good quality encapsulation layer as well. During this process, GST would switch to a partial or a full crystalline state, which could be switched back to

Optics EXPRESS

an amorphous state using the micro-heater. But in our case, we utilized AZ10XT photoresist to mount our die on a larger silicon chip and we wanted to avoid any risk of potential outgassing in AZ10XT [45]), occurring at temperatures higher than the baking temperature of 110° C. We did not want to take the risk so we performed plasma ALD at 50° C. In addition, GST remained in the amorphous state after the oxide capping layer deposition. Before this, we had also tried to deposit PECVD SiO_2 at 125° C as an encapsulation layer instead of Al_2O_3 and we observed that deposition over the AZ10XT photoresist was improper. The encapsulation is necessary to prevent the GST from oxidation and thermal reflow during the programming of GST (i.e. switching the state of GST) [29,41]. Finally, lift-off was performed in acetone to remove the residual photoresist, sonication was also included here as it facilitates the lift-off process.

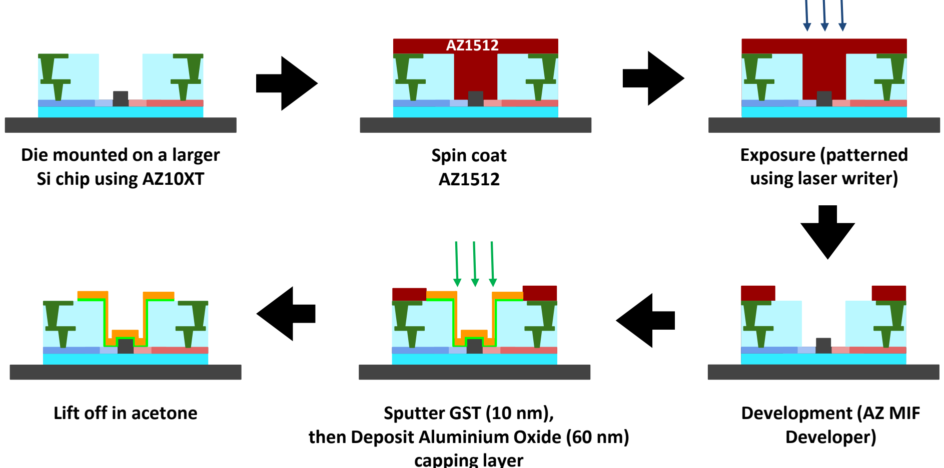

Fig. 2. The BEOL post-processing method for monolithic integration of PCM with commercial silicon photonics chip at the die-level.

Figure 3(a) shows the post-processed PIC with an area of $3mm \times 2mm$, this is the section of the chip dedicated for PCM-based PICs. This chip is composed of multiple blocks of GST-based devices for the characterization of various device configurations and GST (oxide opening) lengths. Each block such as the one shown in Fig. 3(b) was laid out such that we prevented any deposition of GST and alumina on top of the grating couplers and the metal pads with only a coarse lithography overlay. Note that we deposited a blanket of GST over a batch of PCM micro-heaters, illustrating the scalability of this post-processing methodology. The blanket deposition of GST makes it suitable for GST integration with large-scale programmable circuits. During our layout design we placed many batches of devices in a grid fashion, as seen in Fig. 3(a). Cross-shape alignment marks were placed in each grid for mask alignment during the post-processing. Figure 3(c) shows a zoomed-in microscope image of a single device with 8 μm long oxide window opening. The SEM image (Fig. 3(d)) provides a close estimate of the actual dimensions of the oxide window opening over the rib waveguide with the deposited GST and alumina. We notice that the fabricated width of the opening was 1.5 μm and the length of the opening was 7 μm, which are slightly smaller than the intended design values. However, the opening is still large enough to support a reliable GST switching operation, with a large amplitude switching contrast between the two GST states. These results will be discussed in detail in the next section.

Optics EXPRESS

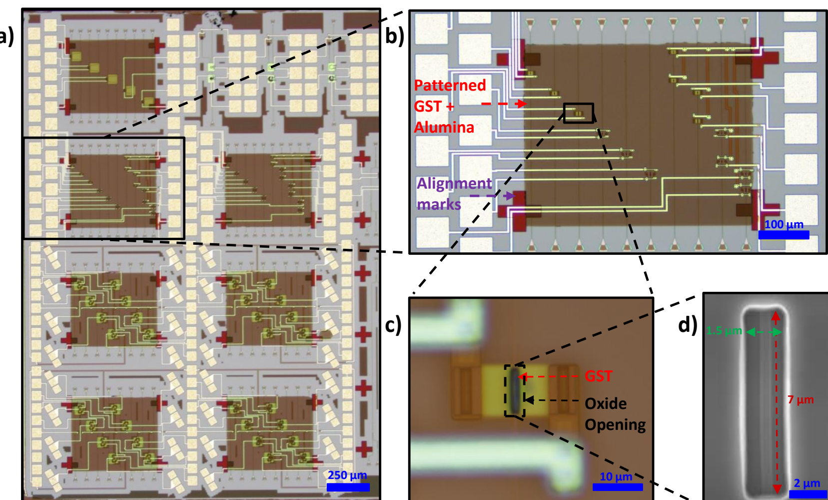

Fig. 3. (a) Microscopic image of post-processed sections of the silicon photonic chip. (b) Microscope image of a single post-processed section. (c) Micrograph image of a PIN micro-heater device with 8 μm long oxide opening. (d) SEM image of the GST deposited oxide opening region.

3. Experimental results

The optical measurements were performed on PIN micro-heater variants with an 8 μm long oxide window opening and two different thicknesses, 10 nm and 12.5 nm, of GST thin film. Figure 4(a) shows the measured I-V characteristics of the PIN micro-heater which follows a rectified diode behavior. The estimated parasitic resistance of wirings is 5 Ω for each device. The effective resistance from the linear section of the IV characteristic plot is 256 Ω, which is around 50 times the calculated wiring resistance. Grating couplers coupled the light from fiber to chip with an optical loss of 4 dB per coupler. Our test devices and PICs are designed and optimized for the O-band (1310nm) operation, but we emphasize that GST provides broadband non-volatility and can also be used for C-band (1550nm). We have verified that our post-processing steps did not affect the coupling loss of the grating couplers. Additionally, we measured an insertion loss of about 1.5 dB across the micro-heater device. The SET operation was performed by applying a lower voltage pulse with a longer width and falling edge (60 % of the pulse width [20]) to the PIN micro-heater, whereas the RESET operation was performed by applying a high voltage pulse with a short pulse width. The SET and RESET parameters were optimized separately for different lengths and thicknesses of GST. In the case of 10 nm thick GST, the applied pulse for RESET operation is 10 V and 500 ns (switching energy of 108.35 nJ), and for SET operation it is 4.5 V and 60 μs with 36 μs falling edge (switching energy of $4.07{\times}10^3$ nJ). Figure 4(c) shows the optical transmission in the O-band and it can be observed that there is a higher insertion loss in the crystalline state of GST coming from the higher absorption coefficient of crystalline GST (c-GST). The transmission plots were normalized to a waveguide with a-GST and grating couplers. The switching is repeatable, non-volatile and on average the total extinction ratio for an 8 μm long opening is 2.4 dB ($\approx$ 0.35 $dB/\mu m$), between a-GST and c-GST. The observed extinction ratio is lower compared to the simulations and that can be caused by the partial amorphization and crystallization processes, as well as a reduction in the actual length of the oxide opening. Furthermore, we have employed a 50°C plasma process for encapsulation layer deposition and the plasma process can also lead to a slight reduction in GST film thickness. Hence, we deposited a 12.5 nm thick GST film for the next device iteration. The applied pulse for RESET operation is

Optics EXPRESS

12 V and 350 *ns* (switching energy of 103 *nJ*), and for SET operation it is 4.5 V and 50 μs with 30 μs falling edge (switching energy of 3.38×10^3 *nJ*). In this case, the measured switching energies are lower for the 12.5 *nm* thick GST film because a shorter pulse was employed with a higher voltage. Figure 4(d) shows the optical transmission in the O-band for GST in both states and we observe a much higher extinction ratio for this thickness of GST, with an 8 μm long opening extinction ratio is 8 *dB* ($\approx$ 1.14 $dB/\mu m$). Figure 4(b) shows the non-volatile and repeatable binary switching between the amorphous and crystalline GST states for both thicknesses of GST (10 *nm* and 12.5 *nm*) with the same length of oxide opening.

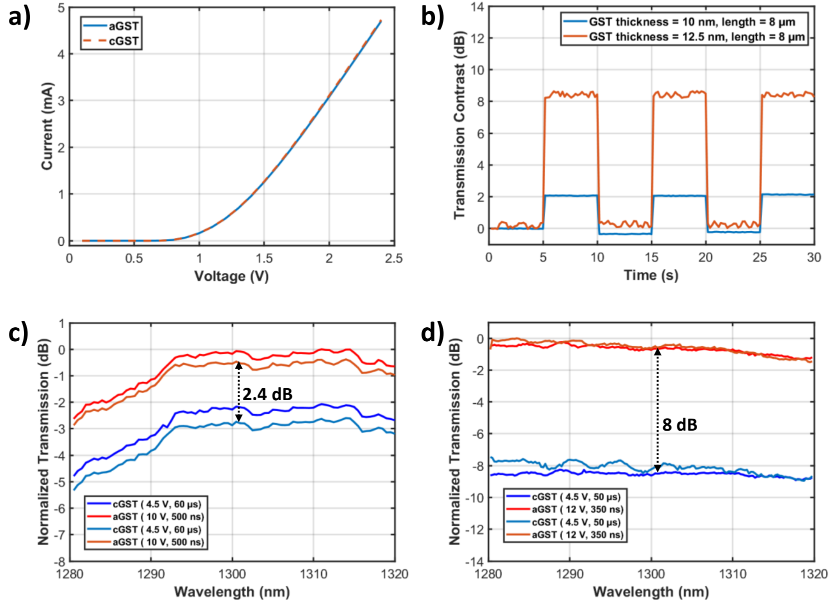

Fig. 4. (a) I-V characteristics of a PIN micro-heater. (b) Change in transmission for consecutive switching events over time. (c) Normalized transmission plots for a device with an 8 μm long and 10 *nm* thick GST film, and (d) 8 μm long and 12.5 *nm* thick GST film, over 2 switching cycles.

We characterize the total switching time by the temporal transient response measurement of optical transmission for the device variant with 8 μm long opening and 12.5 *nm* thick GST film. For amorphization (Fig. 5(a)), the transmission starts to rise at the falling edge of the amorphization pulse, with a response time of 1 μs which makes the total amorphization time around 1.5 μs. Here, the total switching time is dominated by the response time, of the quenching process, which is the critical parameter in the case of amorphization. Only during the quenching i.e. end of the pulse, we saw a rise in the optical response as it switches to the amorphous state. The delayed rise in optical transmission was because of the long carrier lifetime in the PIN diode. In the case of crystallization (Fig. 5(b)), it is critical to have a uniform temperature profile throughout the GST volume and gradual cooling ramp($\approx$ 30 μs) to ensure full crystallization [29,46]. The transmission starts to drop immediately at the rising edge of the crystallization pulse, and it reaches its minimum value within 5 μs. However, we are still required to hold GST in this state for a long period so that the full volume of GST switches to the crystalline state. Since the GST volume is relatively large, we needed to provide a sufficiently long pulse to ensure thermal diffusion throughout the entire volume, allowing the complete switching of the GST. We also tried shorter pulses but that led to partial crystallization of GST, which could be attributed to

Optics EXPRESS

switching of only a fraction of the full volume. Here, the total switching time is dominated by the crystallization pulse width (≈ 50 μs).

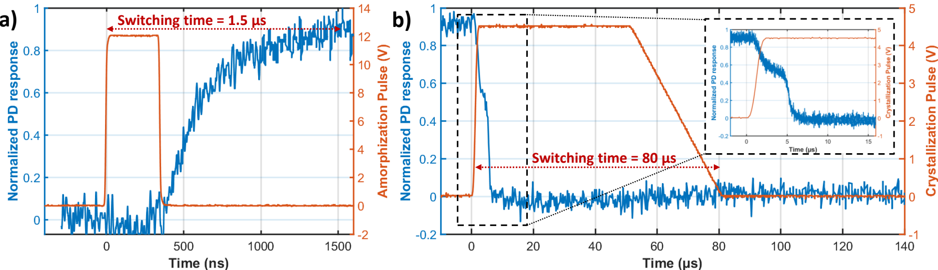

Fig. 5. (a) Temporal response of the optical transmission to the amorphization pulse, and (b) crystallization pulse, measured for a device variant with 8 μm long opening and 12.5 nm thick GST film.

Further, we verified that the GST micro-heater can be programmed for over 10,000 cycles (20,000 switching events), as seen in Fig. 6. The drop in transmission was due to gradual fiber misalignment drift at the grating couplers, and the device was realigned once every 2500 switching events depending on the extent of misalignment. The average extinction ratio in Fig. 6 is annotated section-wise for every 2500 switching events. The average extinction ratio (ER) measured over all of the 20,000 switching events is $9.91 \pm 0.53\, dB$ ($\approx 1.4\, dB/\mu m$). While each switching can happen faster, as fast as $\sim 80\mu s$, we have added a $5s$ delay between the switching events in this experiment. This is to incorporate some of the instrument delays in the experiment setup and in addition, it also provides enough time for the device to cool down to room temperature. The proposed post-processing methodology provides us with a remarkable GST lifetime, and it can be further improved by performing a patterned GST deposition only on the waveguide and then creating a full enclosure using an alumina encapsulation layer, to prevent any melted GST from reflowing.

Next, we demonstrate a four-level (2-bit) switching operation by employing two cascaded PIN micro-heaters as seen in Fig. 7(a). In this case, the two PIN microheaters represent the most significant bit (MSB) and the least significant bit (LSB) in the 2-bit switching operation. The length of the oxide opening in the MSB micro-heater is twice the length of the oxide opening in the LSB micro-heater. This device allows us to show the uniformity of fabricated microheaters and GST deposition across multiple device variants. Here, the LSB oxide opening is 4.5 μm which makes the MSB oxide opening 9 μm long and the thickness of deposited GST film is 10 nm. Here, the applied pulse parameters to program both PIN micro-heaters are the same, RESET operation is 12 V and 350 ns, and for SET operation it is 4.5 V and 50 μs with 30 μs falling edge. Figure 7(b) shows the multilevel switching operation by programming the LSB and MSB micro-heaters sequentially. The "00" state is obtained when both MSB and LSB switches are in the crystalline state. The "01" state is obtained when the LSB switch is programmed to the amorphous state and the MSB switch remains in the crystalline state. Similarly, the "10" state is obtained when the MSB switch is programmed to the amorphous state and the LSB switch remains in the crystalline state. Finally, the "11" state is obtained when both MSB and LSB switches are programmed to the amorphous state. The observed extinction ratio between the "00" and "01" states was around 1.5 dB, between '01" and "10" states the extinction ratio was around 2.5 dB, and between "10" and "11" states the extinction ratio was around 1.25 dB. It was previously observed that the actual length of the oxide openings is smaller than the intended design values and that causes the four levels to not be equally spaced. The error between measured and estimated levels can be due to partial amorphization/crystallization processes and thermal reflow in the previously measured extinction ratios.

Optics EXPRESS

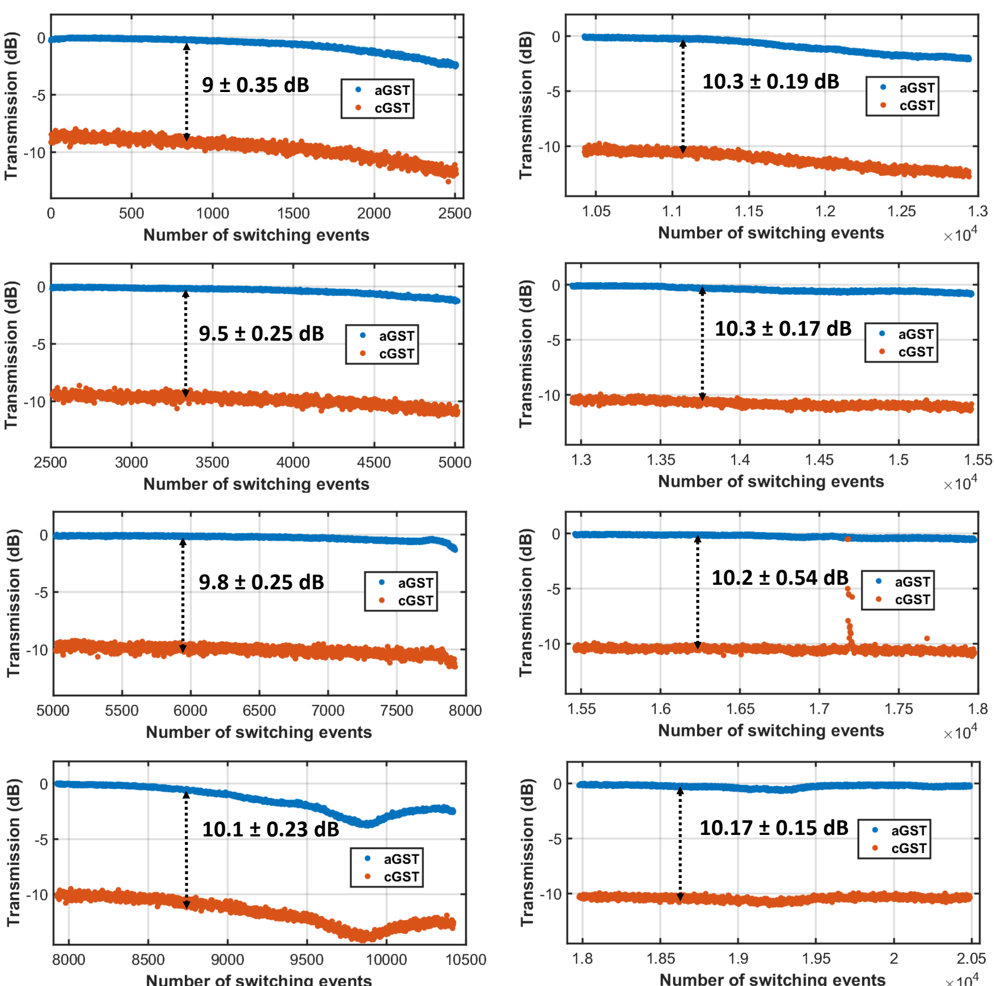

Fig. 6. Endurance test results of the electrically programmable GST switch, with 8 μm long opening and 12.5 nm thick GST film, for over 20,000 switching events.

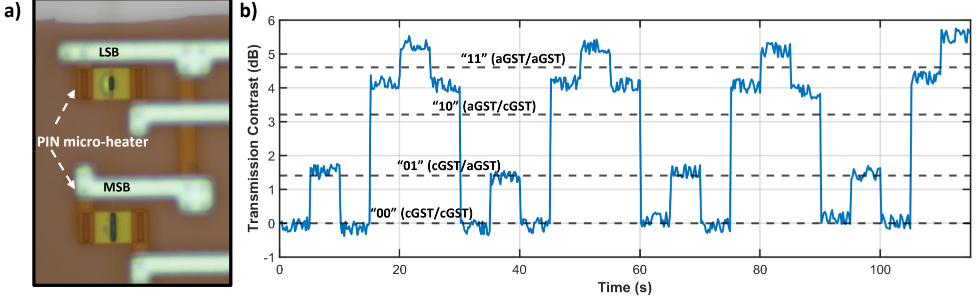

Fig. 7. (a) Microscope image of cascaded MSB and LSB PIN micro-heaters. (b) Change in transmission for multilevel switching events (dashed lines show estimated levels based on previously measured 0.4 $dB/\mu m$ contrast results).

Optics EXPRESS

4. Conclusion and discussion

We have successfully demonstrated a simple post-processing methodology for the integration of GST in a zero-change commercially available silicon photonics foundry process. The functionality of non-volatile switching is verified by measuring a transmission contrast of 1.4 $dB/\mu m$ between the amorphous and crystalline GST states for a device with 8 μm long oxide opening and 12.5 nm thick GST film. In Table 1, we compare our device to the latest reported electrically programmable PCM switches. Device structures include a directional coupler (DC), Mach-Zehnder interferometer (MZI), multi-mode interferometer (MMI), or a single waveguide (WG). Our switch performance is on par with the best-reported values when it comes to extinction ratio (ER) and footprint. The switching energy and insertion loss (IL) of our switch is slightly on the higher side. The switching energy is limited as all non-silicon layers in the PCM micro-heater including metal and via layers were kept at least 5 μm away from the oxide opening to avoid damaging the metal routings during the oxide etch process at the foundry, leading to a higher resistance of our micro-heater. The efficiency of the device can be further improved by reducing the resistance of the device by bringing the metal vias closer to PIN micro-heater with better process control during device fabrication.

Table 1. Table of comparison for electrically programmable PCM devices (+: cross state/bar state, N/R: Not Reported, *: These devices were fabricated in R&D foundry processes with custom changes to the process, **: with custom changes in the commercial foundry process).

Reference	PCM	Device Structure	Extinction Ratio ($dB/\mu m$)	Insertion Loss (dB)	Energy per Switch amf. / crys. (nJ)	Footprint (μm)	Switching Events	Commercial Foundry Process
Kato, K. et al. [47]	GST	WG 1×1	1.2	4.8	20 / 7.2×10^6	1	20	no*
Zhang, H. et al. [48]	GST	MMI 1×1	6.5	7.5	N/R	1	3000	no
Chen, R. et al. [21]	GST	DC 2×2	0.2	2	380 / 6.8×10^3	50	5600	no
Zheng, J. et al. [20]	GST	WG 1×1	1	1.6	13 / 715	5	1000	no
Rios, C. et al. [25]	Sb_2Se_3	MZI 2×2	1.08/2.5$^+$	0.3	176 / 3.8×10^3	100	250	no*
Chen, R. et al. [40]	SbS	DC 2×2	0.14/0.18$^+$	0.98	1216.8 / 7.2 x 10^7	70	1000	yes**
Wei, M. et al. [39]	GSST	WG 1×1	2.46	2.91	N/R	16	3000	yes**
This work	GST	WG 1×1	1.4	1.5	103 / 3.38×10^3	8	20,000	yes

Further, we were able to program the device more than 20,000 times showing a record level of endurance compared with previously reported works, demonstrating the reliability of our post-processing methodology. Our foundry-processed PCM micro-heaters can act as a building block for non-volatile programmable photonics. While we focused on the amplitude switching of the signal, PCM-based devices have been shown as phase shifters by utilizing low-loss PCMs such as SbS, and SbSe [24,25,28]. The demonstrated approach can also be adopted for the integration of different types of PCMs, and emerging electro-optical materials such as non-linear polymers. The introduction of novel modulation schemes in commercial foundry silicon photonics can unlock the potential of programmable photonics across a spectrum of emerging applications.

Funding. National Science Foundation (CCF-2105972, DMR-2329089, NNCI-1542101, NNCI-2025489); U.S. Department of Energy (DE-SC0024729); Office of Naval Research (N00014-17-1-2661).

Optics EXPRESS

Acknowledgments. We would like to acknowledge CMC Microsystems for providing MPW fabrication services for AMF Silicon Photonics technology. Post-processing steps were conducted at the Washington Nanofabrication Facility (WNF), a National Nanotechnology Coordinated Infrastructure (NNCI) site at the University of Washington, with partial support from the National Science Foundation via awards NNCI-1542101 and NNCI-2025489.

Disclosures. The authors declare no conflicts of interest.

Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

References

1. C. Sun, M. T. Wade, Y. Lee, *et al.*, "Single-chip microprocessor that communicates directly using light," Nature **528**(7583), 534–538 (2015).
2. A. H. Atabaki, S. Moazeni, F. Pavanello, *et al.*, "Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip," Nature **556**(7701), 349–354 (2018).
3. A. Z. Subramanian, E. Ryckeboer, A. Dhakal, *et al.*, "Silicon and silicon nitride photonic circuits for spectroscopic sensing on-a-chip," Photonics Res. **3**(5), B47–B59 (2015).
4. J. Sun, E. Timurdogan, A. Yaacobi, *et al.*, "Large-scale nanophotonic phased array," Nature **493**(7431), 195–199 (2013).
5. Y. Shen, N. C. Harris, S. Skirlo, *et al.*, "Deep learning with coherent nanophotonic circuits," Nat. Photonics **11**(7), 441–446 (2017).
6. A. N. Tait, T. F. De Lima, E. Zhou, *et al.*, "Neuromorphic photonic networks using silicon photonic weight banks," Sci. Rep. **7**(1), 7430 (2017).
7. N. C. Harris, G. R. Steinbrecher, M. Prabhu, *et al.*, "Quantum transport simulations in a programmable nanophotonic processor," Nat. Photonics **11**(7), 447–452 (2017).
8. S. Shekhar, W. Bogaerts, L. Chrostowski, *et al.*, "Roadmapping the next generation of silicon photonics," Nat. Commun. **15**(1), 751 (2024).
9. W. Bogaerts, D. Pérez, J. Capmany, *et al.*, "Programmable photonic circuits," Nature **586**(7828), 207–216 (2020).
10. S. Y. Siew, B. Li, F. Gao, *et al.*, "Review of silicon photonics technology and platform development," J. Lightwave Technol. **39**(13), 4374–4389 (2021).
11. J. S. Orcutt, B. Moss, C. Sun, *et al.*, "Open foundry platform for high-performance electronic-photonic integration," Opt. Express **20**(11), 12222–12232 (2012).
12. M. R. Watts, J. Sun, C. DeRose, *et al.*, "Adiabatic thermo-optic mach–zehnder switch," Opt. Lett. **38**(5), 733–735 (2013).
13. K. Padmaraju, J. Chan, L. Chen, *et al.*, "Thermal stabilization of a microring modulator using feedback control," Opt. Express **20**(27), 27999–28008 (2012).
14. G. T. Reed, G. Mashanovich, F. Y. Gardes, *et al.*, "Silicon optical modulators," Nat. Photonics **4**(8), 518–526 (2010).
15. M. Jacques, A. Samani, E. El-Fiky, *et al.*, "Optimization of thermo-optic phase-shifter design and mitigation of thermal crosstalk on the soi platform," Opt. Express **27**(8), 10456–10471 (2019).
16. Z. Fang, R. Chen, B. Tossoun, *et al.*, "Non-volatile materials for programmable photonics," APL Mater. **11**(10), 100603 (2023).
17. A. Chen, "A review of emerging non-volatile memory (nvm) technologies and applications," Solid-State Electron. **125**, 25–38 (2016).
18. C. Xiang, S. M. Bowers, A. Bjorlin, *et al.et al.*, "Perspective on the future of silicon photonics and electronics," Appl. Phys. Lett. **118**(22), 220501 (2021).
19. J. Zheng, A. Khanolkar, P. Xu, *et al.*, "Gst-on-silicon hybrid nanophotonic integrated circuits: a non-volatile quasi-continuously reprogrammable platform," Opt. Mater. Express **8**(6), 1551–1561 (2018).
20. J. Zheng, Z. Fang, C. Wu, *et al.*, "Nonvolatile electrically reconfigurable integrated photonic switch enabled by a silicon pin diode heater," Adv. Mater. **32**(31), 2001218 (2020).
21. R. Chen, Z. Fang, J. E. Fröch, *et al.*, "Broadband nonvolatile electrically controlled programmable units in silicon photonics," ACS Photonics **9**(6), 2142–2150 (2022).
22. M. Delaney, I. Zeimpekis, D. Lawson, *et al.*, "A new family of ultralow loss reversible phase-change materials for photonic integrated circuits: Sb_2s_3 and sb_2se_3," Adv. Funct. Mater. **30**(36), 2002447 (2020).
23. Z. Fang, J. Zheng, A. Saxena, *et al.*, "Non-volatile reconfigurable integrated photonics enabled by broadband low-loss phase change material," Adv. Opt. Mater. **9**(9), 2002049 (2021).
24. R. Chen, Z. Fang, C. Perez, *et al.*, "Non-volatile electrically programmable integrated photonics with a 5-bit operation," Nat. Commun. **14**(1), 3465 (2023).
25. C. Ríos, Q. Du, Y. Zhang, *et al.*, "Ultra-compact nonvolatile phase shifter based on electrically reprogrammable transparent phase change materials," PhotoniX **3**(1), 26 (2022).
26. C. Wu, H. Deng, Y.-S. Huang, *et al.*, "Freeform direct-write and rewritable photonic integrated circuits in phase-change thin films," Sci. Adv. **10**(1), eadk1361 (2024).
27. Z. Fang, B. Mills, R. Chen, *et al.*, "Arbitrary programming of racetrack resonators using low-loss phase-change material sb_2se_3," Nano Lett. **24**(1), 97–103 (2024).

Optics EXPRESS

28. Z. Fang, R. Chen, J. Zheng, *et al.*, "Ultra-low-energy programmable non-volatile silicon photonics based on phase-change materials with graphene heaters," Nat. Nanotechnol. **17**(8), 842–848 (2022).
29. R. Chen, Z. Fang, F. Miller, *et al.*, "Opportunities and challenges for large-scale phase-change material integrated electro-photonics," ACS Photonics **9**(10), 3181–3195 (2022).
30. M. Wuttig and N. Yamada, "Phase-change materials for rewriteable data storage," Nat. Mater. **6**(11), 824–832 (2007).
31. N. Yamada and T. Matsunaga, "Structure of laser-crystallized ge_2 sb_2+ x te_5 sputtered thin films for use in optical memory," J. Appl. Phys. **88**(12), 7020–7028 (2000).
32. S.-H. Lee, Y. Jung, and R. Agarwal, "Highly scalable non-volatile and ultra-low-power phase-change nanowire memory," Nat. Nanotechnol. **2**(10), 626–630 (2007).
33. N. Farmakidis, N. Youngblood, X. Li, *et al.*, "Plasmonic nanogap enhanced phase-change devices with dual electrical-optical functionality," Sci. Adv. **5**(11), eaaw2687 (2019).
34. W. Zhou, B. Dong, N. Farmakidis, *et al.*, "In-memory photonic dot-product engine with electrically programmable weight banks," Nat. Commun. **14**(1), 2887 (2023).
35. J. R. Erickson, V. Shah, Q. Wan, *et al.*, "Designing fast and efficient electrically driven phase change photonics using foundry compatible waveguide-integrated microheaters," Opt. Express **30**(8), 13673–13689 (2022).
36. J. R. Erickson, N. A. Nobile, D. Vaz, *et al.*, "Comparing the thermal performance and endurance of resistive and pin silicon microheaters for phase-change photonic applications," Opt. Mater. Express **13**(6), 1677–1688 (2023).
37. C. Wu, D. Sturm, U. Adya, *et al.et al.*, "Integration of phase change material with commercial 45nm monolithic silicon photonics," in *CLEO: Science and Innovations* (Optica Publishing Group, 2023), paper SF3E–5.
38. D. Onural, H. Gevorgyan, C. Eschenbaum, *et al.et al.*, "Toward hybrid integration of exotic materials in an electronic-photonic cmos platform via substrate removal," in *CLEO: Science and Innovations* (Optica Publishing Group, 2023), paper STh3H–4.
39. M. Wei, K. Xu, B. Tang, *et al.*, "Monolithic back-end-of-line integration of phase change materials into foundry-manufactured silicon photonics," Nat. Commun. **15**(1), 2786 (2024).
40. R. Chen, V. Tara, M. Choi, *et al.et al.*, "Deterministic quasi-continuous tuning of phase-change material integrated on a high-volume 300-mm silicon photonics platform," Research Square (2023).
41. M. Wuttig, H. Bhaskaran, and T. Taubner, "Phase-change materials for non-volatile photonic applications," Nat. Photonics **11**(8), 465–476 (2017).
42. J. Park, M. R. Kim, W. S. Choi, *et al.*, "Characterization of amorphous phases of $ge_2sb_2te_5$ phase-change optical recording material on their crystallization behavior," Jpn. J. Appl. Phys. **38**(8R), 4775 (1999).
43. E. Morales-Sanchez, E. Prokhorov, A. Mendoza-Galván, *et al.*, "Determination of the glass transition and nucleation temperatures in ge_2 sb_2 te_5 sputtered films," J. Appl. Phys. **91**(2), 697–702 (2002).
44. J. Orava, A. á. Greer, B. Gholipour, *et al.*, "Characterization of supercooled liquid $ge_2sb_2te_5$ and its crystallization by ultrafast-heating calorimetry," Nat. Mater. **11**(4), 279–283 (2012).
45. M. Biercuk, D. Monsma, C. Marcus, *et al.*, "Low-temperature atomic-layer-deposition lift-off method for microelectronic and nanoelectronic applications," Appl. Phys. Lett. **83**(12), 2405–2407 (2003).
46. P. Prabhathan, K. V. Sreekanth, J. Teng, *et al.*, "Roadmap for phase change materials in photonics and beyond," iScience **26**(10), 107946 (2023).
47. K. Kato, M. Kuwahara, H. Kawashima, *et al.*, "Current-driven phase-change optical gate switch using indium–tin-oxide heater," Appl. Phys. Express **10**(7), 072201 (2017).
48. H. Zhang, L. Zhou, J. Xu, *et al.*, "Nonvolatile waveguide transmission tuning with electrically-driven ultra-small gst phase-change material," Sci. Bull. **64**(11), 782–789 (2019).

205.175.118.132 {ts '2025-01-01 00:25:52'}